



Reliability Assessment of Advanced Flip-Chip
Interconnect Electronic Package Assemblies Under Extreme
Cold Temperatures Down to -190°C and -120°C

Final Report
(JPL D-27617)

Dr. Rajeshuni Ramesham

Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Tel.: 818 354 7190, *Fax:* 818 393 4382,
e-mail: Rajeshuni.ramesham@jpl.nasa.gov

Structure of this final report

- 1.0 Abstract
- 2.0 Introduction
- 3.0 Underfill materials
- 4.0 Testing for overstress interconnect fracture
- 5.0 Flip-Chip Test Boards
- 6.0 Temperature profile.
- 7.0 Electrical Resistance Measurements
 - 7.1 X-ray imaging and surface acoustic microscopy
- 8.0 FB500 Flip Chip Board
 - 8.1 Bare chip inspection prior to thermal cycling
 - 8.2 Solder wetting after reflow
 - 8.3 Underfill
- 9.0 FB250 Flip Chip Board
 - 9.1 underfill
- 10.0 Potential failure mechanisms associated with the flip-chip technology
- 11.0 Conclusions and Future Activities
 - 11.1. Conclusions
 - 11.2 Future Activities
- 12.0 References
- 13.0 Short Biography of the Author
 - 13.1 Rajeshuni Ramesham
- 14.0 Acknowledgements

1.0 Abstract

Flip-chip interconnect electronic package boards have been assembled, underfilled, non-destructively evaluated and subsequently subjected to extreme temperature thermal cycling to assess the reliability of this advanced packaging interconnect technology for future deep space long term extreme temperature missions. In this very preliminary study, the employed temperature range that covers military specifications (-55°C to 100°C) and the extreme cold Martian (-120°C to 115°C) and asteroid Nereus (-180°C to 25°C) environment. The resistance of the daisy-chained flip-chip interconnects has been measured at room temperature and at various intervals as a function of extreme temperature thermal cycling. Very preliminary electrical resistance measurements have been reported; and the tests to date have not shown significant change in resistance as a function of extreme temperature thermal cycling. However, the greater the number of thermal cycles, the change in the daisy chained flip chips' interconnect resistance is noticeable. Further research work is needed to understand the reliability of flip-chip interconnect packages under extreme temperature applications via continuously monitoring the daisy chain resistance for any intermittent failures at the temperature extremes and adapt suitable diagnostic techniques to identify the failure mechanisms.

2.0 Introduction

Flip-chip interconnect technology is an advanced electrical interconnection approach where the silicon die or chip is electrically connected face down to the substrate by reflowing solder bumps on area-array metallized terminals on the die to matching footprints of solder-wettable pads on the chosen substrate. This advanced flip-chip interconnect technology will significantly improve the performance of high-speed systems, the productivity enhancement over manual wire bonding, self alignment during die joining, low lead inductances, and reduced need for precious attachment of metals, etc. The failure mechanisms of advanced flip-chip interconnects are dependent on the structures and materials of ball limiting metallurgy (BLM) associated with the die and top surface metallurgy associated with the substrate and the solder joint and solder reflow temperature, and the solder materials. The most predominant failure mechanisms are solder joint fatigue, interdiffusion, creep, underfill delamination, and electrochemical corrosion. Any thermal expansion co-efficient mismatches between the silicon die, underfill (with filler and without filler) and the substrate causes shear displacement at each solder joint interconnect, which may lead to low-cycle thermal fatigue failure during thermal or power cycling. Reliability may be significantly increased by matching/tailoring the coefficient of thermal expansion (CTE) of the substrate material and the silicon die or chip and also the underfill materials. The CTE is defined as change in length of the material per degree centigrade often expressed in parts per million/°C or ppm/°C. The key contributing factors to solder joint fatigue failure are interdiffusion at the chip/solder and substrate/solder interfaces, the solder material, dimensions of the contact area, and CTE of the die and substrate, and finally the environment where they are going to be employed or used. Growth of intermetallics occurs due to interdiffusion processes lead to chemical, physical, and microstructural changes via dissolution of base metals into the solder and their precipitation into the solder, which probably weaken the strength of the materials at the interface. Intermetallics may possibly reduce the fatigue life of the solder joints in the flip-chip advanced interconnect electronic packages. [1-5]

The use of underfill materials is necessary with flip-chip interconnect technology to redistribute stresses due to mismatching coefficient of thermal expansions between dissimilar

materials in the over all assembly. Underfills are in general being formulated using organic polymers and possibly with inorganic filler materials. There are a few ways to apply the underfills with flip-chip technology. Traditional capillary flow underfill materials now possess high flow speed and reduced time to cure, they still require additional processing steps beyond the typical surface mount technology (SMT) assembly process. The use of newly developed no-flow fluxing underfills provides a means of reducing the processing steps employed in the traditional capillary flow methods to enhance SMT compatibility notably. The eventual goal of each process step and the entire process is to produce components with 100% interconnect and satisfying the reliability requirements. [6-10] NASA's long duration deep space missions, severe launch operations, etc., demand highly shock resistant electronic device and package reliability. Underfill materials, in general, may possibly meet demanding end use requirements such as low warpage, low stress, fine pitch, high reliability and high adhesion.

3.0 Underfill materials

The advanced flip-chip interconnect solder joints are generally referred to as controlled collapse chip connections (C4), which have exhibited remarkable reliability observed by International Business Machines (IBM). [11] The improvement of C4 reliability has been achieved by filling the gap between silicon chip and the substrate material or board material using a suitable polymer material. These polymers are called as underfill materials. Underfill is an organic material or a polymeric material that may be mixed/filled with inorganic material (ex. fused silica, etc.), which will be used to fill the space between the die and the substrate. Fused silica is a suitable candidate filler material due to its compatibility with silicon die, coefficient of thermal expansion, chemically inert/corrosion resistant, thermally conducting, and also its favorable dielectric properties. The filler provides the strength in the composite polymer, and the resin bonds the die and the substrate. [8] Paralynes, silicones, silica filled epoxy resins may be used as underfills. [12-15] These underfills may be tailored to a desired glass transition temperature, elastic modulus, and coefficient of thermal expansion (CTE) match to the solder materials. The improvement was attributed to enhancing the chip constraint, matching the elastic modulus to the solder, and the solder essentially sealed from the ambient or the environment. Underfilling of advanced flip-chips is now widespread in a variety of applications in commercial industries. The possible drawback of this technology is non-reworkability of the underfill materials. [1]

The reliability studies using underfills were reported in the literature in a temperature range of -50°C to 150°C , which resulted in an increase of reliability by one to two orders of magnitude.[9] Thermal shock of the flip-chip test articles were designed to induce failures at the interconnect sites (-40°C to 100°C). [1]The study on the reliability of flip chips using underfills in the extreme temperature region is of significant use for space applications. This technology is considered as an enabling technology for future space applications. Therefore, this study has been under taken to assess the reliability of advanced flip-chip interconnect technologies with underfill polymeric/composites under extreme temperatures.

4.0 Testing for overstress interconnect fracture

Several tests may be employed to assess the advanced flip-chip interconnect technology designs based on the potential failure mechanisms. The key failure mechanism addressed in thermal cycling is bond fracture or interfacial deadhesion due to overstress at the interfaces of die/solder and solder/substrate. The temperature cycling may result in a thermal fatigue of the

solder bump and interdiffusion at the die/solder or substrate/solder interface. The stress depends on the magnitude of the temperature either on the high temperature side or low temperature side, rate of temperature change, and range (ΔT) of temperature and also CTE of the materials combination. High rate of change of temperature (Change in temperature/minute) could lead to thermal shock of the advanced flip-chip interconnect packages. Therefore, low rate of change of temperature ($5^{\circ}\text{C}/\text{minute}$) has been employed in this study. [16,17]

5.0 Flip-Chip Test Boards

With an increasing number of input/output (I/Os) on integrated circuits (IC) and accompanying requirements for high performance, flip-chip type components have become a compelling technology to be pursued, characterized, and employed. NASA could be one of the users, especially in the context of wide extreme temperature ranges towards deep space and long term missions to enhance the electronic package reliability and subsequently to enhance the mission assurance of the respective project. Test chips on the board are daisy chained for electrical resistance continuity monitoring purposes. Figure 1 show the optical photographs of the FB250 and FB500 test boards: High temperature FR4 (Glass transition temperature, $T_g = 176^{\circ}\text{C}$) 0.031" thickness, copper conductor, Taiyo PSR-400 solder mask, FB250 board (10: 250 x 250 mil² sites, pitch 18 mil, minimum line 6 mil, and maximum space 12 mil), and FB500 board (10: 500 x 500 mil² sites, pitch 18 mil, minimum line 6 mil, and maximum space 12 mil). Glass transition temperature is defined as a phase transition that occurs at a specific temperature in hardened polymer from the hard glassy state to the rubbery state. Most materials have lower strength and exhibit a higher coefficient of thermal expansion above the glass transition temperature.

6.0 Temperature profile

Figure 2 shows the temperature profiles employed in this preliminary study to perform the extreme temperature thermal cycling of the daisy chained FB250 and FB500 flip-chip interconnect test boards.

1. Base line temperature: 25°C (room temperature)
2. TC1 cover two ranges (Mars mission environments)
 - a. 281 cycles in a temperature range of (X) -120°C to $+115^{\circ}\text{C}$; Y: ramp rate of $5^{\circ}\text{C}/\text{minute}$
 - b. 200 cycles in a temperature range of (X) -120°C to $+85^{\circ}\text{C}$; Y: ramp rate of $5^{\circ}\text{C}/\text{minute}$
3. TC2 range: 200 cycles in a temperature range of (X) -55°C to $+100^{\circ}\text{C}$; Y: ramp rate of $5^{\circ}\text{C}/\text{minute}$ (military environments)
4. TC3 range: 311 cycles in a temperature range of (X) -120°C to $+85^{\circ}\text{C}$; Y: ramp rate of $5^{\circ}\text{C}/\text{minute}$ (Mars mission environments)
5. TC4 range: 88 thermal cycles in a temperature range of (X) -190°C to $+25^{\circ}\text{C}$; Y: ramp rate of $5^{\circ}\text{C}/\text{minute}$ (asteroid Nereus encounter/landing)

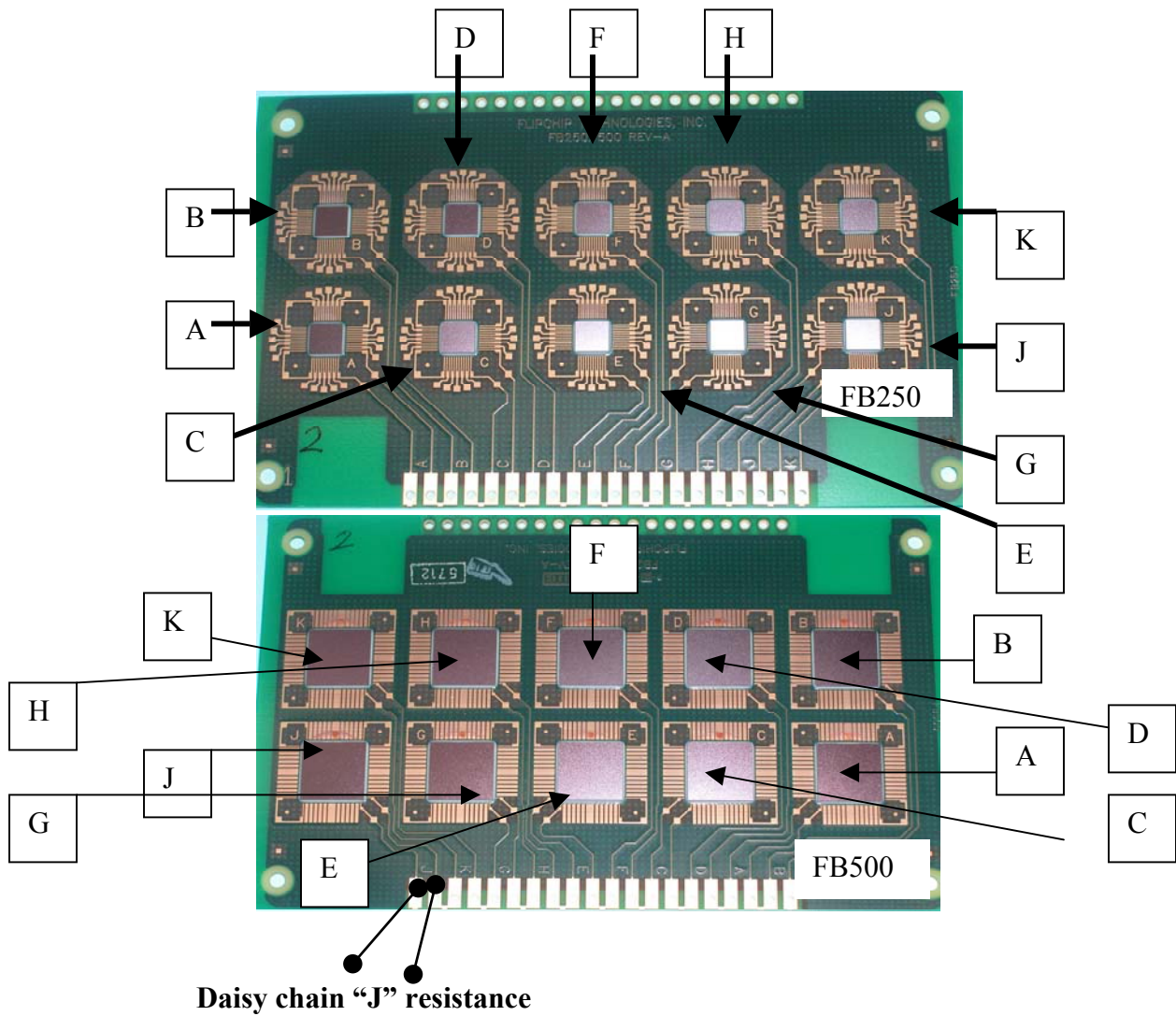
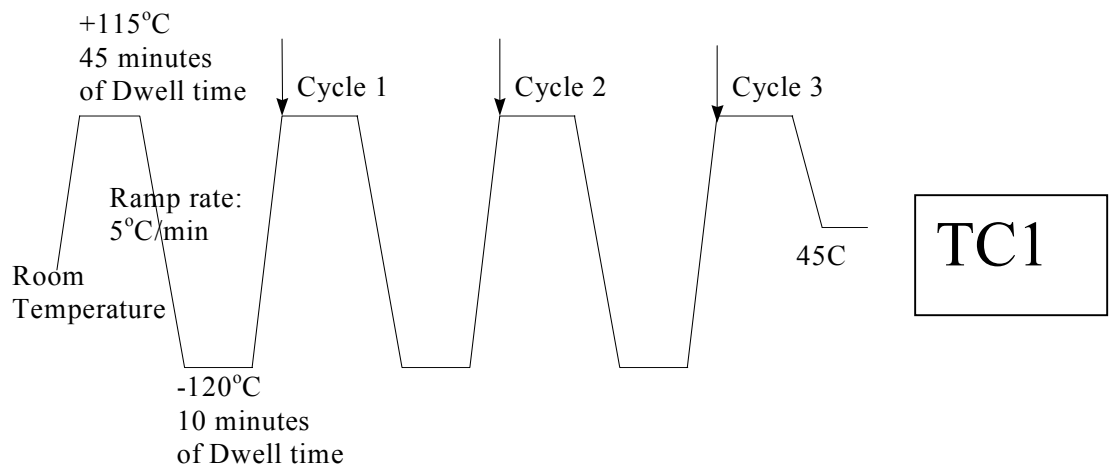


Figure 1: Optical photographs of the assembled advanced flip-chip Interconnect test boards of FB250 and FB500



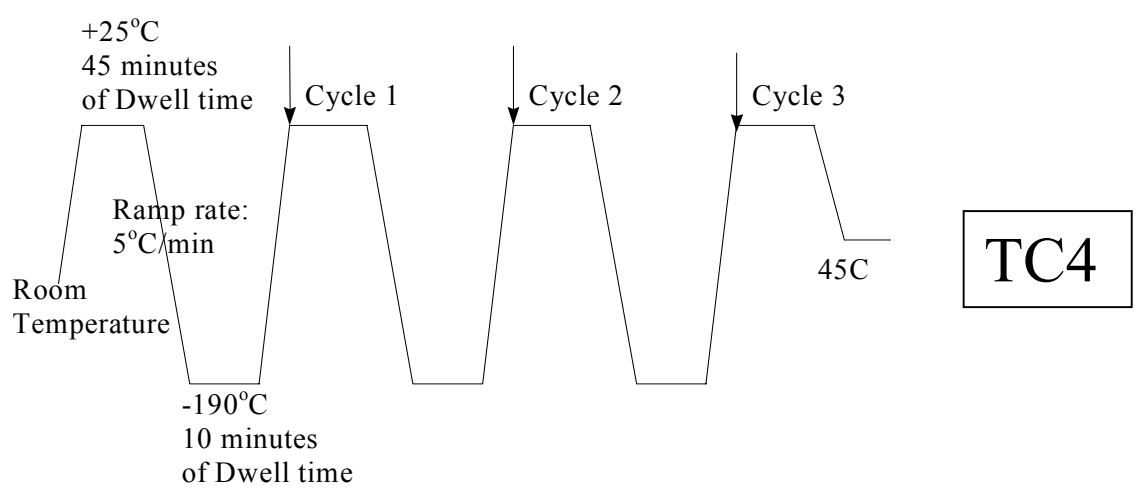
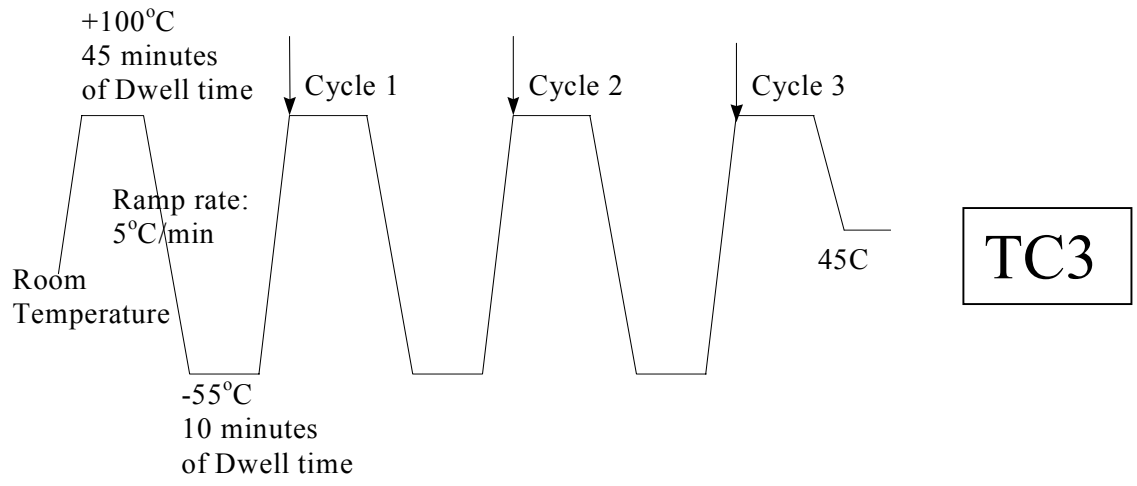
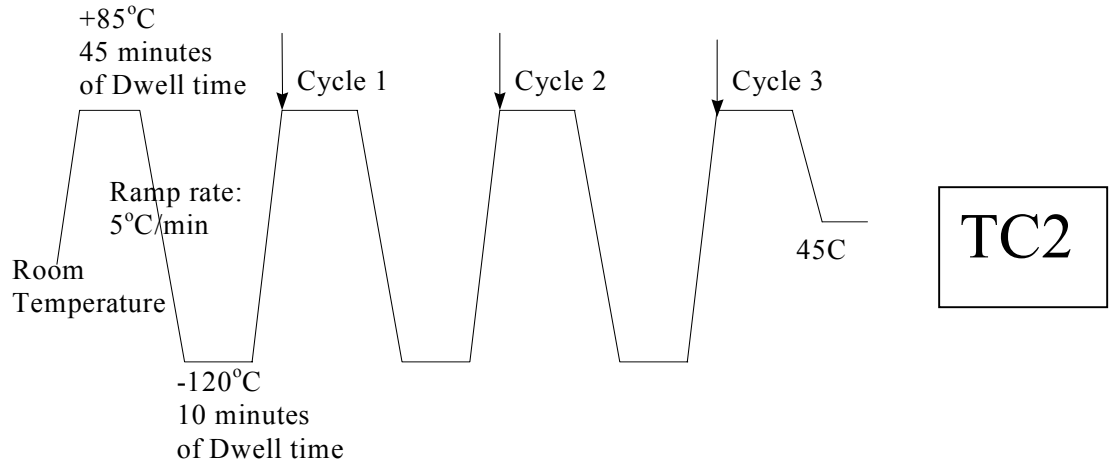


Figure 2: Thermal cycle test profiles employed for various temperature ranges of thermal cycling of flip-chip interconnect test boards

7.0 Electrical Resistance Measurements

The resistance of the daisy chains such as A,B,C,D,E,F,G,H,J,K of FB250 and daisy chains such as J,K,G,H,E,F,C,D,A,B of FB500 test boards as identified in Figure 1 was measured as a function of thermal cycling performed in various temperature ranges as described above in the temperature profile section. The schematic of temperature profiles are described in figure 2. Dwell time was maintained for 10 minutes on cold side and for 45 minutes on the hot side of the temperature profile. The ramp rate of 5°C/minute was used in this study. [16] Figures 3 to 6 show the experimental electrical resistance test data of daisy chains in FB250 and FB500 flip chip boards, which was measured at room temperature after various intervals of thermal cycling. In this experimental test data resistance was not monitored during the thermal cycling. The test on monitoring the resistance while thermal cycling is performed will be conducted in the future studies. The tests performed in this report do not provide the clues for any intermittent failure (instantaneous failure) that usually occurs under thermal cycling particularly at the solder joints such as chip/solder and board or substrate/solder interfaces during extreme temperature thermal cycling. Intermittent failures such as open circuits or very high resistance may be revealed if continuous resistance monitoring is performed while such failures will not be detected if the resistance measurements are made at room temperature. This may lead to poor understanding of the flip chip reliability. However, the present studies at least provides the physical integrity of the chip, underfill, and the substrate via appropriate diagnostic techniques.

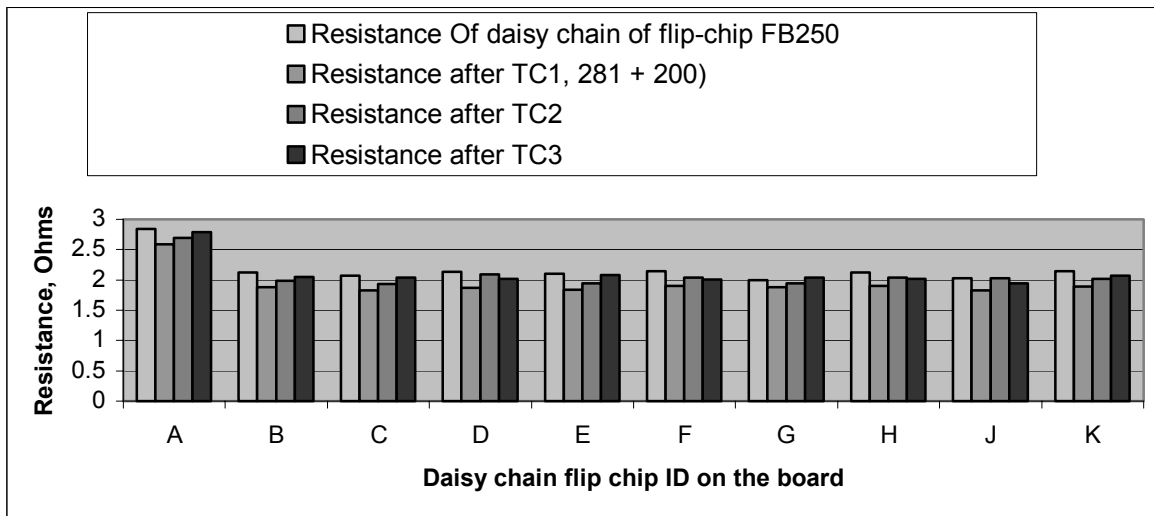


Figure 3: Resistance of daisy chains such as A,B,C,D,E,F,G,H,J,K of flip-chip FB250 test board. A. Measured resistance at room temperature, b. resistance measured after 481 thermal cycles -120°C to 115°C and -120°C to 85°C (TC1), c. Resistance measured after 200 thermal cycles -55°C to 100°C (TC2), and d. Resistance measured after 311 thermal cycles -125°C to 85°C (TC3).

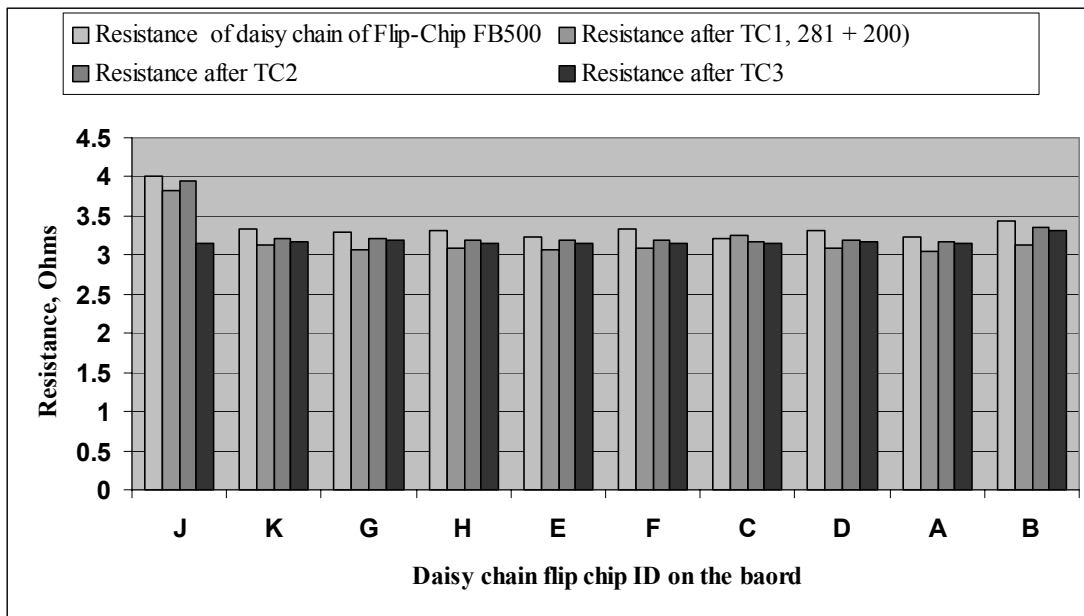


Figure 4: Resistance of the daisy chains such as J,K,G,H,E,F,C,D,A,B of flip-chip FB500 test board. A. Resistance of the pair at room temperature, b. resistance of the pairs measured after 481 thermal cycles -120°C to 115°C and -120°C to 85°C (TC1), and c. Resistance of the pairs measured after 200 thermal cycles -55°C to 100°C (TC2) and d. Resistance of the pairs measured after 311 thermal cycles -125°C to 85°C (TC3).

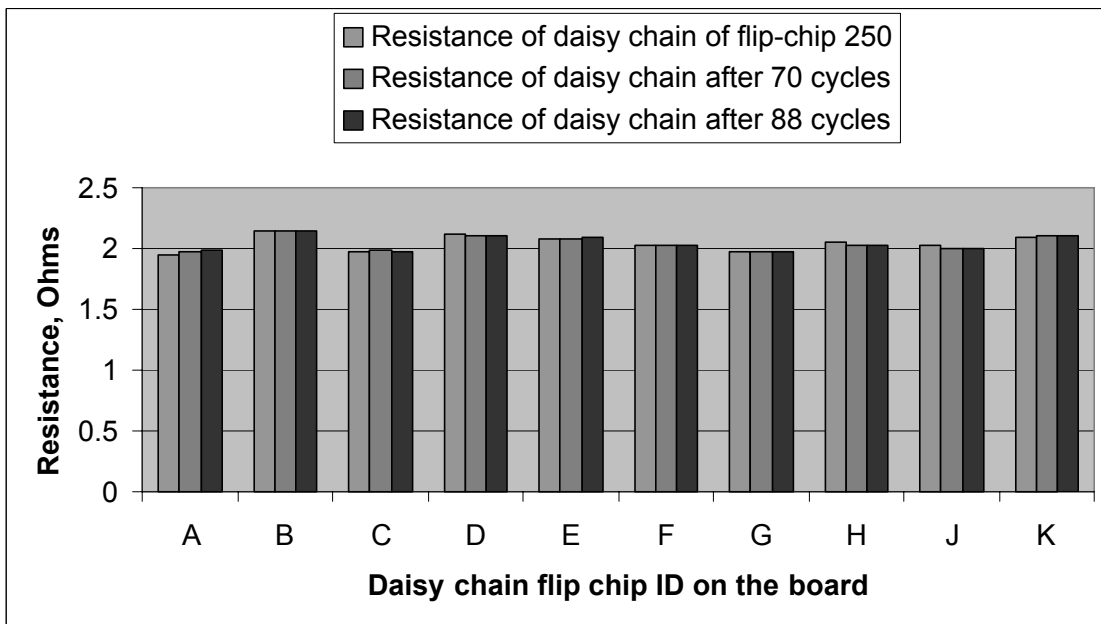


Figure 5: Resistance of the daisy chains such as A,B,C,D,E,F,G,H,J,K of flip-chip FB250 test board. a. Resistance of the daisy chains at room temperature, b. resistance of the daisy chains

measured after 70 thermal cycles (-190°C to 25°C) and c. Resistance of the daisy chains measured after 88 thermal cycles (-190°C to 25°C).

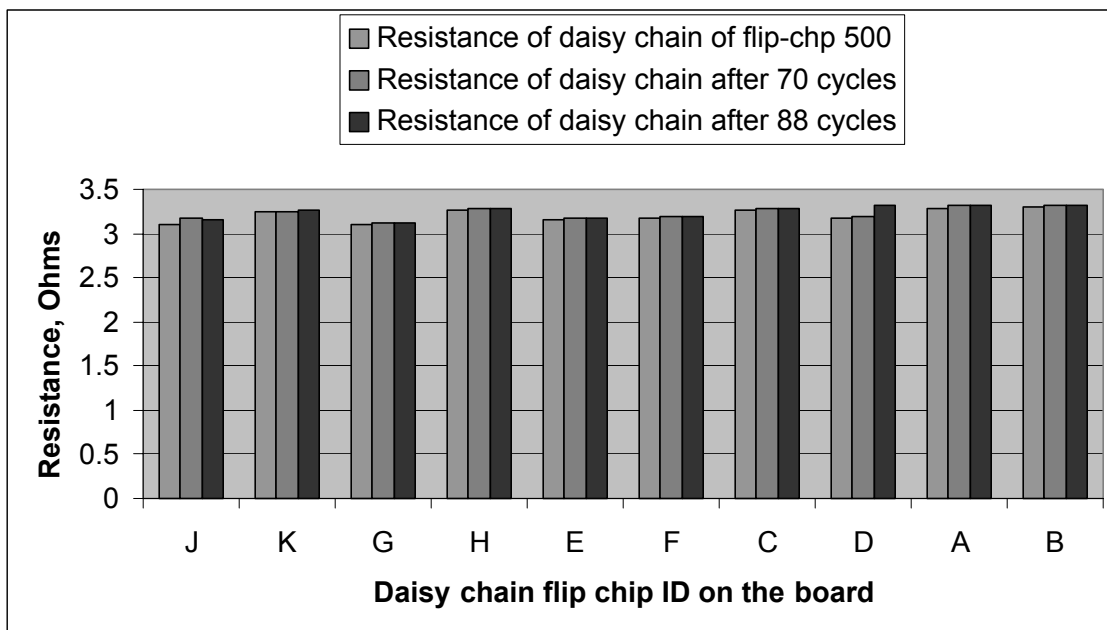


Figure 6: Resistance of daisy chains such as J,K,G,H,E,F,C,D,A,B of flip-chip FB500 test board. A. Resistance of the daisy chains at room temperature, b. resistance of the daisy chains measured after 70 thermal cycles (-190°C to 25°C) and c. Resistance of the daisy chains measured after 88 thermal cycles (-190°C to 25°C).

7.1 X-ray imaging and surface acoustic microscopy

This work will be performed shortly to identify the failures in the advanced flip-chip interconnects as a function of thermal cycling in various extreme temperature ranges. Electrical test results show that there is not a significant change in resistance as a function of conventional and extreme temperature thermal cycling.

8.0 FB500 Flip Chip Board

8.1 Bare chip inspection prior to thermal cycling

The nondestructive X-Ray image of one of the flip chips on the test board is shown in Figure 7. They are the image of two opposite corner at the same magnification, which shows non-uniform solder bumping.

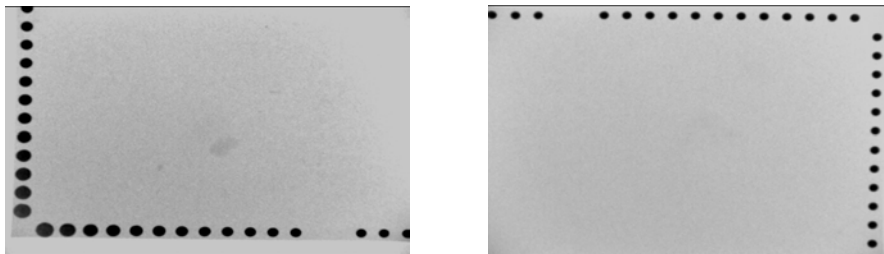


Figure 7. X-Ray image of bare chip at two opposite corner

8.2 Solder wetting after reflow

Kester 6502 tacky flux with a shim of 35 μ m thickness was used for this to build. The X-ray image of solder joint after reflow is shown in Figure 8. They are also the image of two opposite corner at the same magnification, which show different wetting result. The cross section images of the two adjacent edge corresponding to Figure 8(b) are shown in Figure 9.

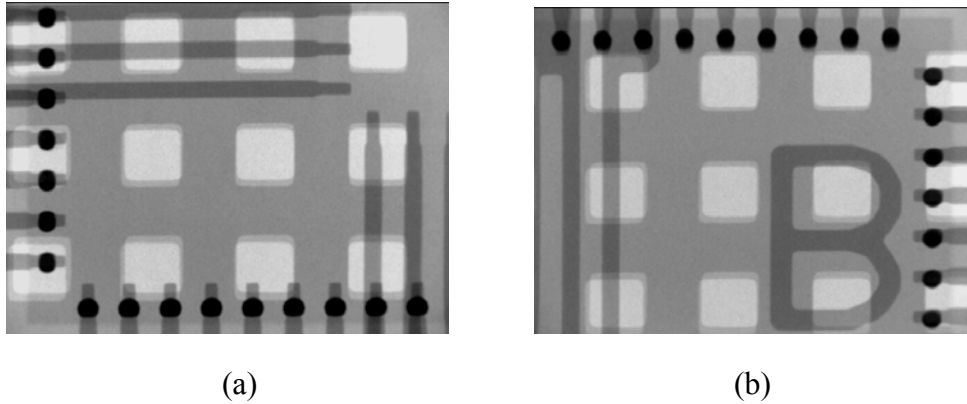


Figure 8. X-Ray image of solder wetting after reflow

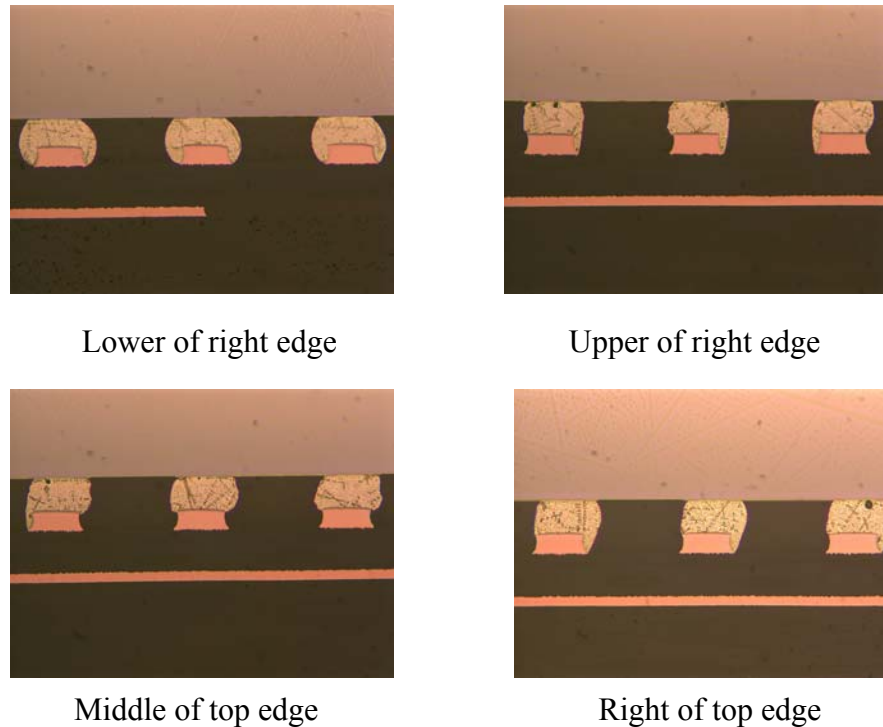


Figure 9. Cross section images of top right corner viewing from chip side

8.3 Underfill

The parameters for underfill process are shown in Table 1. The CSAM images were obtained after underfill cure. One out of forty chips was found with void, which is shown in Figure 10. The middle line pattern with one-third length of the edge was used for dispensing.

The void occurred close to the opposite edge. The RDP stands for Research and Development product of Loctite. This product was supplied to Auburn University (Dr. Wayne Johnson) to evaluate the underfill characteristics by Loctite Electronic division. RDP-960 is the proprietary composition formulated by Loctite. The technical data sheet may be corresponding to a Product 3595 of Loctite. Loctite product 3595 snap cure underfill is a rapid curing, fast flowing, liquid epoxy designed for use as a capillary flow underfill for flip chip devices.

Underfill	Stage temp. (°C)	Air pressure (psi)	Needle gauge	RPM	Line speed (in/sec)
RDP-960	80	6	#23	250	0.08

Table1. Parameters for underfill component FB500

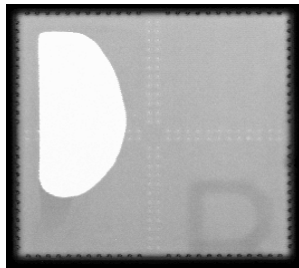


Figure 10. CSAM image of underfill with void (Board 3 die C)

9.0 FB250 Flip Chip Board

9.1 Solder wetting after reflow

Kester 6502 tacky flux with a shim of 35µm thickness was used to build. The nondestructive X-Ray image of solder joint after reflow is shown in Figure 11. It shows good wetting by viewing the shape of solder joint.

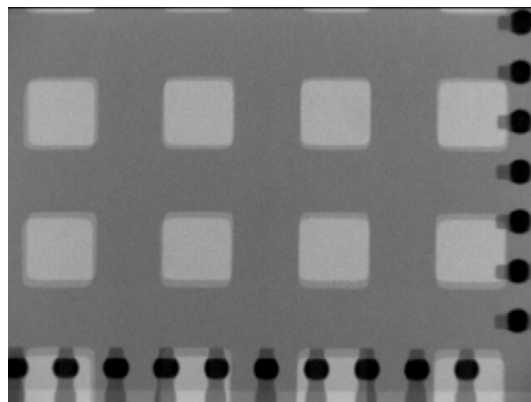


Figure 11. X-Ray image of solder wetting after reflow

9.1 Underfill

The parameters for underfill process are shown in Table 2. The CSAM images were obtained after underfill cure. Four out of seventy chips were found with void, which are shown in Figure 12. The middle line pattern with one-third length of the edge was used for dispensing. The void occurred close to the opposite edge. RDP: Research Development Product of Loctite. (Loctite Product 3595)

Underfill	Stage temp. (°C)	Air pressure (psi)	Needle gauge	RPM	Line speed (in/sec)
RDP-960	100	6	#23	250	0.08

Table 2. Parameters for underfill component FB250

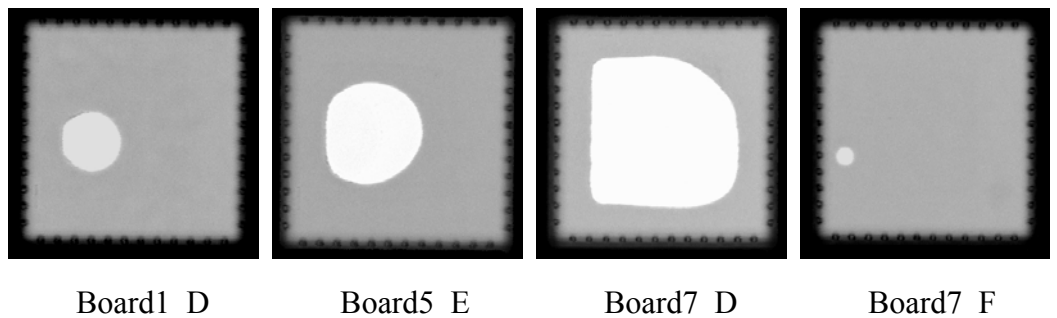


Figure 12. CSAM images of underfill with voids

11.0 Potential failure mechanisms associated with the flip-chip technology

Probable potential failure mechanisms include underfill delamination, solder fatigue, creep, corrosion, intermetallic formation, die fracture, etc., which may occur or to be revealed during various test methods such as thermal cycling, thermal shock, etc. employed during flip chip evaluation.

11.0 Conclusions and Future Activities

11.1. Conclusions

Advanced packaging interconnect technology such as flip-chip interconnect test boards (FB250 and FB500) have been subjected to various extreme temperature ranges that cover military specifications and extreme Mars and an asteroid (Nereus) environments. Higher the number of thermal cycles the change in resistance of the daisy chained flip chip interconnects was measured as a function of increasing number of thermal cycles. No catastrophic failures were observed yet even after 481 extreme temperature thermal cycles as per electrical resistance measurements and repeated the test for 311 thermal cycles to corroborate the test result. Process qualification and assembly is required to optimize the flip-chip assembly, [16,17] which is very

clear from the x-ray and C-SAM studies. X-Ray and C-SAM studies have not been made after thermal cycling, which will be done shortly as the funds available.

11.2 Future Activities

Several test vehicles/articles/boards (*ref.* IPC 9701, [16]) may be assembled to assess the reliability using various types of underfill applying methods such as capillary underfills, fluxing underfills, and advanced underfills applied to the wafer/die and also the variation of the underfill thickness (space between the die and the substrate). Reliability assessment of flip chip assemblies with various underfills that consists of fillers with various dimensions. Tailoring or matching of the coefficient of thermal expansion of the underfill with filler and the substrate, the die is a significant step to improve the reliability. Understanding the glass transition temperature of the underfills and reflow processes in the assembly of flip chips will also play a vital role in their performance for high reliability applications. Effect of solder ball configuration (staggered or irregular, single row perimeter, and/or area array flip chip) on the reliability should be evaluated. Thickness of the die and the substrate are also important in designing the experiments to assess the reliability. The effect of voids in the solder balls and underfill regions is to be assessed for their reliability. AC impedance technique is one of the most commonly used technique to address the corrosion issues, which may be used to address the underfill integrity, corrosion at the interfaces and intermetallic formation, effect of moisture and temperature, power cycling on the impedance characteristics of the interfaces, etc. Assessment of reworkable underfills in the flip chip technology for the deep space missions is also vital importance to the space applications. Identification of compliant interconnects and underfill with more fatigue resistant interconnects is vital to our applications. Reliability assessment of lead based and lead-free solders based flip-chips is also very important for long-term space applications. Thermal shock and highly accelerated techniques may be used to rapid screen the over all flip chip assemblies for their reliability. Reliability assessment of flip chip assemblies may be assessed systematically using IPC 9701 [16] with suitable modifications appropriate to space applications based on the respective project.

12.0 References

1. R. W. Johnson, "Flip-chip assembly and underfilling" Chapter 19, Preprint
2. R. W. Johnson, Q. Wang, R. Zhao, L. Crane, M. Konarski, E. Yaeger, R. Tiskoff, P. Krug, S. Bauman, M. Chason, J. Danvir, N. Yala, J. Qi, P. Kulakarani, "Wafer applied underfills for flip chip assembly", Preprint
3. M. Pecht, A. Dasgupta, J.W. Evans, J. Y. Evans, "Quality conformance and qualification of microelectronics packages and interconnects" Chapter 8, page 207, John Wiley & Science, Inc., 1994.
4. M. Pecht, "Integrated circuit, hybrid, and multichip module package design guidelines, A focus on reliability", Chapter 7, page 183, John Wiley & Science, Inc., 1994.
5. R. R. Tummala, E. J. Rymaszewski, A.G. Klopfenstein, Microelectronic Packaging Handbook, Volumes I, II, III, Chapman and Hall, 1997.
6. D. Katze (Emersion and Cuming) "No flux underfill material and process considerations" HDI 2000.
7. D. Katze, "No-Flow fluxing underfill process characterization." Proceedings of the APEX technical program, San Diego, CA January 16-18, 2001, pp. MT2-21 – MT2-29.

8. K. Gilleo, "The chemistry and physics of underfills" Alpha Metals, Cranston, RI (USA), e-mail: gilleo@compuserve.com, Preprint.
9. D. Patterson, "Solder alloy development for next generation flip chip applications," <http://www.kns.com/connections/solder-alloy/asp>
10. Loctite-Electronics underfills website. <http://www.loctite.com> and <http://www.loctite.fi/int>
11. P.A. Totta and R.P. Sopher, "SLT (Solid Logic Technology) device metallurgy and its monolithic extension," IBM Journal of Research and Development, pp. 226 – 238, 1969 (May).
12. H.M. Tong, L. Mok, K.R. Grebe, H.L. Yeh, K.K. Srivastava, and J.T. Griffin, "Paralene encapsulation of ceramic packages for liquid nitrogen applications" Proc. 1990, ECTC, pp. 345-350, 1990.
13. D. Suryanarayana, R. Hsaio, T.P. Gall, J.M. McCreary, "Enhancement of flip chip fatigue life by encapsulation," IEEE Trans. Components Hybrids Manuf. Tech. CHMT-14(1): pp. 218-223, 1991.
14. D.W. Wang and K.I. Papathomas, "Encapsulant for fatigue life enhancement of controlled-collapse chip connection (C4)," IEEE Trans. Components Hybrids Manf. Tech., CHMT-16(8), pp. 863-867, 1993.
15. J. Clementi, J. McCreary, T.M. Niu, J. Palomaki, J. Varcoe and G. Hill, "Flip-chip encapsulation on ceramic substrates," Proc 1993 ECTC, pp. 175-181, 1993.
16. IPC-9701, "Performance test methods and qualification requirements for surface mount solder attachments" Jan 2002 (IPC: Association connecting electronics industries).
17. R. Ghaffarian, "Qualification approaches and thermal cycle test results for CSP/BGA/FCBGA" Microelectronics Reliability, 43, 695-706, 2003.

13.0 Short Biography of the Author

13.1 Dr. Rajeshuni Ramesham has been working in quality assurance section of Office of Safety and Mission Success at the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California for over 6 years. His present research work focus on the reliability of packaging and interconnects associated with the microelectromechanical systems (MEMS) applications and advanced adhesion and bonding issues in microelectronics, and photonics packaging under extreme temperatures. He also works on the application of polycrystalline synthetic diamond for MEMS, electrochemical, electroanalytical, and corrosion resistant coating applications. Before joining JPL, Dr. Ramesham spent over 9.5 years at Auburn University, Auburn, Alabama. His research work at Auburn University addressed the fundamental issues involved in diamond processing techniques, heat dissipation techniques, and electrochemical applications of diamond.

Dr. Ramesham has received many awards for his work. These include an outstanding research performance award from the Electrical Engineering Department of Auburn University and 7 awards from NASA for the research work he performed. He has published over 100 refereed journal and proceedings articles and has made over 82 national and international conference presentations. He has given invited presentations at the national and international conferences. He received the best research paper award from the IEEE Alabama Section. He is a chair for Microelectromechanical activities at the SPIE's Micromachining and Microfabrication Conference and International Conference on Mechanics in Medicine and Biology. and committee member CANEUS micro-nano technology conference. Dr. Ramesham received his Ph.D from the Indian Institute of Science, Bangalore, India.

14.0 Acknowledgements

This progress report has been put together by Dr. Rajeshuni Ramesham of Jet propulsion Laboratory (JPL), California Institute of Technology (Caltech) towards Cold Electronics Interconnect Reliability Task funded through Electronics Packaging Project (EPAC) under a contract with National Aeronautics and Space Administration's Electronic Parts and Packaging (NEPP) Program. The research work described in this report was carried out by the Jet Propulsion Laboratory (JPL), California Institute of Technology, Pasadena, CA sponsored by the NEPP Program through Advanced Technology Program Office (ATPO) of the Office of Safety and Mission Success (OSMS) Directorate at JPL.

I would like to sincerely and particularly thank Dr. Reza Ghaffarian for allowing me to work in this task and accomplish the reported results. Mr. Phillip Zulueta, Project Manager, Electronic Packaging (EPAC) Project and Dr. Charles Barnes, Program Manager (NASA Electronic Parts and Packaging Program) is acknowledged for their funding support to this task. Mr. Carl De Silveira (Section Manager) for his support in the Quality Assurance Engineering Office of OSMS to carry out the reported research work in this report. The report represents the up to date results on "Reliability Assessment of Advanced Flip-Chip Interconnect Electronics Package Assemblies Under Extreme Cold Temperatures Down to -190°C and -120°C ". Thanks to Debbie Goodwin of Practical Components for all the necessary components to build the FB250 and FB500 flip-chip boards and Dr. Wayne Johnson of Auburn University in assembling the flip-chip interconnect boards employed in this study using the Loctite's Research and Development underfill product.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA.