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Latchup Test Considerations for Analog-to-Digital Converters†

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I. BASIC CONSIDERATIONS

Many CMOS circuits are sensitive to latchup from heavy ions, and latchup is one of the major considerations when CMOS devices are evaluated for space applications. Radiation-induced latchup has been studied for many years [1-8], but it remains a difficult problem in actual circuits because latchup sensitivity inherently depends on the layout and distribution of contacts, power and ground within complex circuits [9,10]. The gain of the parasitic bipolar transistors that form potential latchup paths is nearly always high enough so that latchup can potentially occur. However, the key factor in latchup sensitivity is the external resistance across the base-emitter junctions of the two parasitic transistors, not the transistor gain [11].

A diagram of a four-region device in a typical n-well CMOS circuit is shown in Figure 1. This device has a bulk substrate. As discussed in references 6, 7, 12 and 13, the triggering process is initiated by a heavy ion strike in the well-substrate junction (the region with the largest charge collection depth). If the voltage drop within the n-well due to the heavy-ion strike is above approximately 0.6 V, then it is possible for the vertical parasitic transistor to turn on. The amplified current from the vertical transistor then flows through the substrate region, making it possible to turn on the second transistor and initiate latchup.

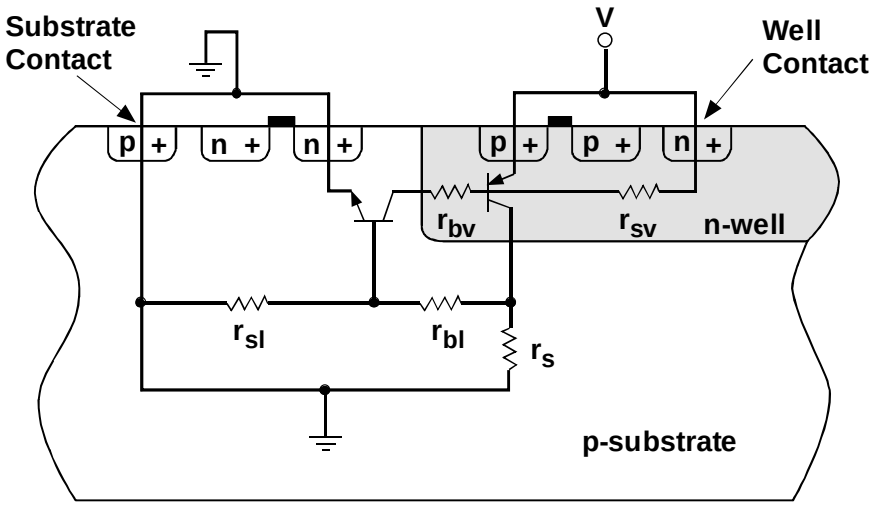

Figure 1. Latchup path in a CMOS structure. The bipolar transistors are parasitic elements that are not directly related to the properties of the MOS transistors used in the design.

Commercial CMOS devices are designed to withstand electrically induced latchup from transients or start-up conditions at the input, output and power supply connections, but generally do not consider triggering from *internal* transients such as those caused by heavy ions. Many CMOS devices are fabricated on so-called epitaxial substrates where a relatively thin lightly doped epitaxial region is grown over a highly doped, low resistivity substrate. The purpose is to provide a low substrate resistance that requires higher current to forward bias the substrate. All things being equal, CMOS devices that use epitaxial substrates are more resistant to latchup than devices with bulk

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substrates. However, most commercial designs reduce the interelement spacing on devices with epitaxial substrates (taking advantage of the improved latchup characteristics) and in many cases radiation-induced latchup can occur quite readily on devices with epitaxial substrates. For example, one type of modern microprocessor exhibits destructive latchup [14] even with protons even though it uses a very thin epitaxial substrate (about 2.5 μm).

Latchup depends on temperature, as shown by several studies of electrically induced latchup [15,16]. The triggering current for electrically induced latchup decreases more than a factor of two as the temperature of latchup test structures is increased from 300 to 400 K. The main reason for this dependence is the increase in well resistance (it approximately doubles), with some additional contribution from the decreased forward voltage at high temperature. Most data on radiation-induced latchup has found that the threshold LET is reduced at high temperature [17,18], paralleling the temperature dependence of triggering current for electrically induced latchup.

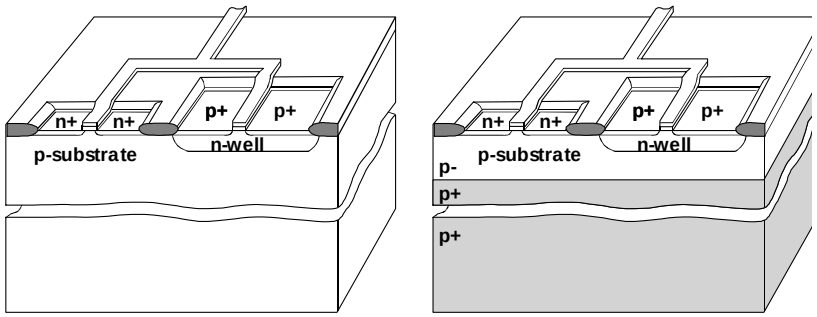

Figure 2. Comparison of bulk and epitaxial substrates.

One earlier paper argued that the temperature dependence of transistor gain was the mechanism for latchup temperature dependence [3]. Although their analysis of the temperature dependence of gain was correct, the model that they used for latchup did not recognize that the base-emitter junctions of the parasitic transistors are effectively shorted by the well and substrate resistances. Although transistor gain does indeed increase with temperature, the gain of the two transistors involved in latchup is well above the minimum gain required for latchup. The body of work in the electron device community on latchup [9-11, 15, 16] along with later work on single-event latchup verified that triggering is due to turn on of the parasitic vertical transistor formed by the isolation well [6, 7]. Nearly all work on radiation-induced latchup has found that the threshold LET decreases more than a factor of two at elevated temperature and that the cross section is substantially higher -- in some cases more than an order of magnitude -- at elevated temperature. Work with test structures has shown this conclusively, although circuit results can be more complicated. Figure 3 shows a typical result.

II. Experimental Approach

The Analog Devices AD9240 is a successive-approximation 14-bit analog-to-digital converter that incorporates three different power supplies (all are 5 V). The maximum conversion rate is 10 Mb/s. One supply is used for the analog section of the part, and it has the highest power consumption during normal operating (nominally 50 mA). A second power supply connection is used for digital circuitry in the interior regions, and it typically requires about 7 mA during normal operation. A third power supply is used to provide power to the output drivers. The nominal current is only a few mA, depending on duty cycle.

The AD9240 is produced in a plastic package. A special acid delidding system was used to etch away the plastic at the top surface, thereby allowing direct access to the top of the die for heavy ion testing. The device was powered and tested in a development board, provided as a standard item by the manufacturer for evaluation purposes. The development board is designed to minimize electrical noise and interference between the digital and analog sections of the device, and is considerably less costly than development of a custom test fixture for this high-resolution part.

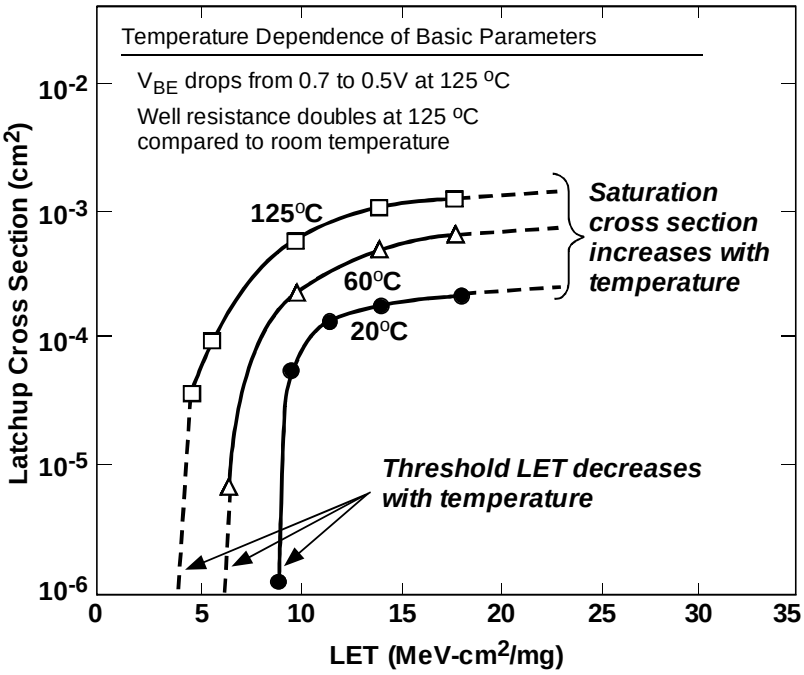

Figure 3. Typical dependence of threshold LET on temperature. The cross section also increases at high temperature, but the magnitude of the increase varies widely for different circuit types, possibly because additional latchup paths can be triggered at elevated temperature.

Radiation testing was done by irradiating the device in the test board, monitoring functional operation and the currents in each power supply. Devices from three different date codes were tested, 9722, 9910 and 9930. All devices appeared to behave in about the same way and had identical surface topology. A special power supply was used that could shut down power within about 100 ms after a high-current condition was found in any of the power supplies. The current trigger conditions and current limit could be programmed separately. Rapid shutdown prevented destructive burnout and minimized heating during the time that latchup occurred.

III. LATCHUP CHARACTERIZATION OF THE AD9240

A. Heavy Ion Test Results

The cross section for latchup of the AD9240 is shown in Figure 4. Data were obtained from several different experiments, some of which were done at angle to increase the effective LET. The effective range (taking the incident angle into account) is shown for each data point. Counting statistics are nominally 5-8%. Note that the cross section is substantially higher for ions with longer range; in particular the cross section for the last data point with 23 μm range is about a factor of three lower than that of the next-to-last data point that was taken with a 160 μm range ion. The threshold LET was above 15 MeV-cm²/mg.

The cross section increases somewhat gradually over a wide range of LET values. All of the tests with heavy ions were done using somewhat conservative current limit values for the three power supplies to avoid destroying the device, and allow a series of tests to be done on a small number of devices. The current limit values were 30 mA for the two digital power supplies (with nominal operating values of 2 to 7 mA) and 100 mA for the analog power supply (with nominal operating current 50 mA). The equilibrium current condition approximately 100 ms after latchup occurred was monitored for each latchup event. Although many of the events corresponded to full current limit for the analog power supply (100 mA), about 25% of the events resulted in an equilibrium current below that limit.

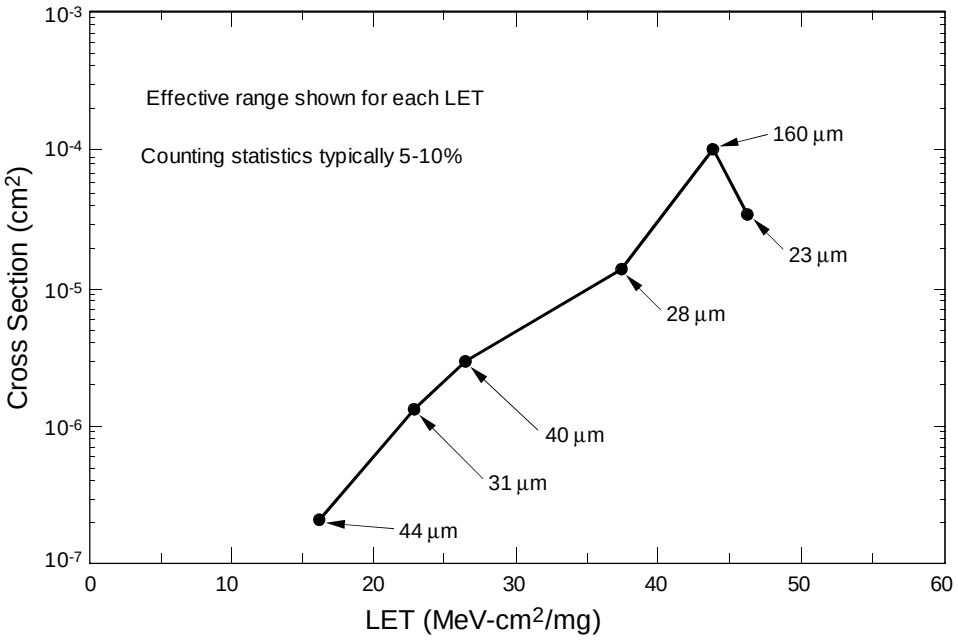

Figure 4. Latchup cross section of the Analog Devices AD9240 obtained after several different radiation tests. Note the different ranges for various points on this curve.

Later tests were done using californium ions in our laboratory with the current limit of all three power supplies extended to 2 A. Those tests showed a very wide range of latchup equilibrium currents for the digital power supply, ranging from about 45 to more than 300 mA. A histogram of the currents obtained during the tests with californium is shown in Figure 5. Similar variability occurred for currents in the analog power supply for latchup events that caused current to increase in the analog circuitry.

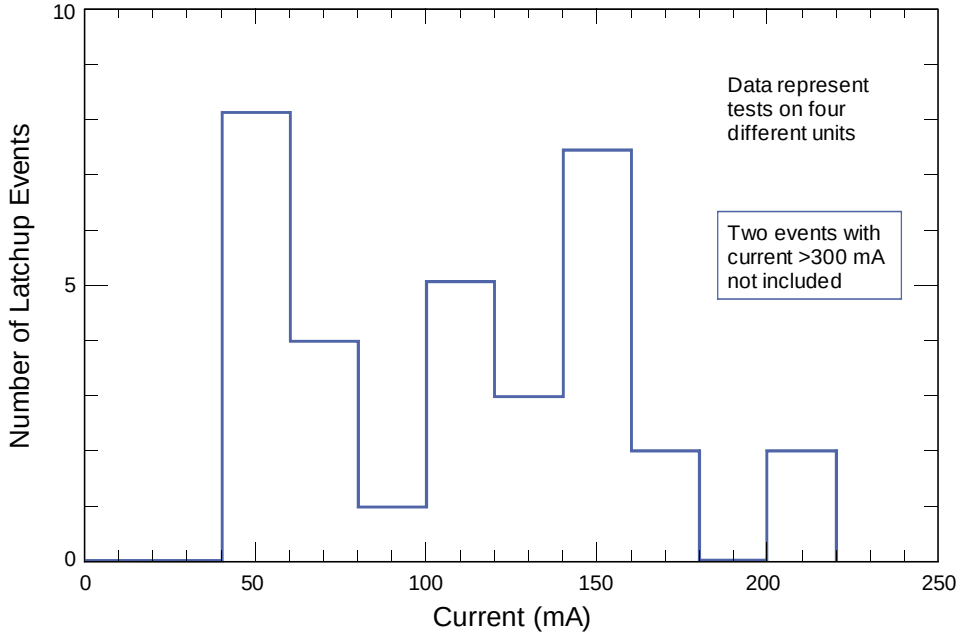

Figure 5. Histogram of many different latchup events showing the wide range of equilibrium currents in the analog power supply when the devices were irradiated (and latched) with californium. Power supply current limiting (2 A) was well above the highest latchup current

The latchup events with californium were of two types, as determined by monitoring the power supply currents. Latchup occurred either in the interior digital regions or the analog section, but never in the output drivers. Most of the latchups did not result in device destruction, even though the current limit was 2 A. Note however that the californium is not necessarily capable of triggering events that correspond to LET above about 25 MeV-cm^2/mg because of the limited range of the californium fission fragments.

Some tests were done by leaving the device in a latched state, allowing subsequent latchup events to occur. Substantial heating of the device occurred after the first latchup event, allowing later latchup events to be more easily triggered. Figure 6 shows a representative test of this type in which four latchup events were observed. Note that the current drops slightly after each current "step," probably because the metallization resistance and well resistance increase due to localized heating. The last event resulted in destructive failure of the device.

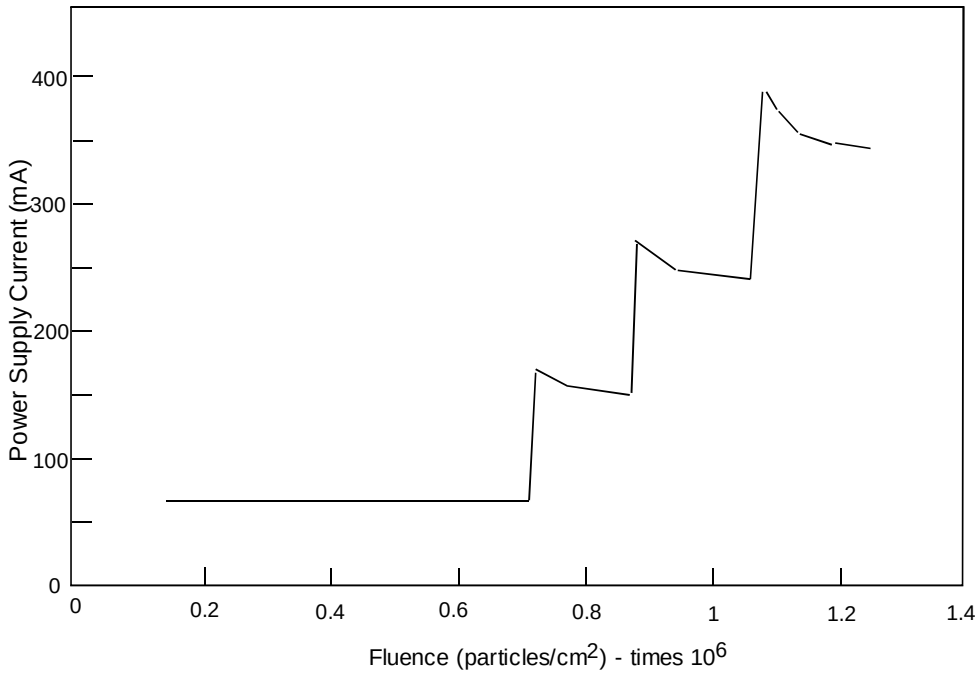

Figure 6. Sequence of latchup events during tests with continual irradiation with californium fission fragments. Each current step corresponds to an additional latchup event in a different region of the device.

B. Thermal Imaging of Latched Regions

It is very difficult to determine which internal regions of complex devices are actually involved in the latchup path. One way to do this is to use a thermal imaging system to examine the surface topology before and after latchup. Thermal imaging systems rely on an infrared-sensitive cooled detector system, coupled through a microscope with an optical system that transmits in the infrared region. Such systems are commercially available that contain software for automated analysis of the temperature distribution. However, the calibration is limited by the variation in thermal emissivity in different regions. Areas covered by metallization have a much lower emissivity than silicon regions of the chip. Nominal "normalization" of differences in emissivity can be obtained by storing thermal images of the device surface before and after latchup, and that approach is satisfactory for identifying latchup-sensitive regions even though the temperature increase cannot be precisely measured.

Higher sensitivity (and better thermal accuracy) can be obtained by coating the device after latchup has occurred with a thin layer of black paint to provide more uniform emissivity. After the initial image (with the device latched), power was momentarily interrupted and the device was allowed to come to thermal equilibrium for about two minutes. At that time a second thermal image was taken.

The difference between those two images can then be used to measure the actual surface temperature of the device, assuming an emissivity near one. The thermal imaging system provides software to determine differences on a pixel-by-pixel basis, along with a calibration. Surface temperatures of about 130 C were determined in this way.

Latchup was observed in many different interior regions of the AD9240. Figure 7 shows an outline of the die, along with regions where latchup was observed during several different irradiations with californium. After each latchup event, the device was removed from the vacuum chamber (retaining power to keep the device in a latched condition) so that the thermal imaging results correspond to equilibrium conditions with the device in air. The size of the heated regions was on the order of 15 to 30 μm in diameter.

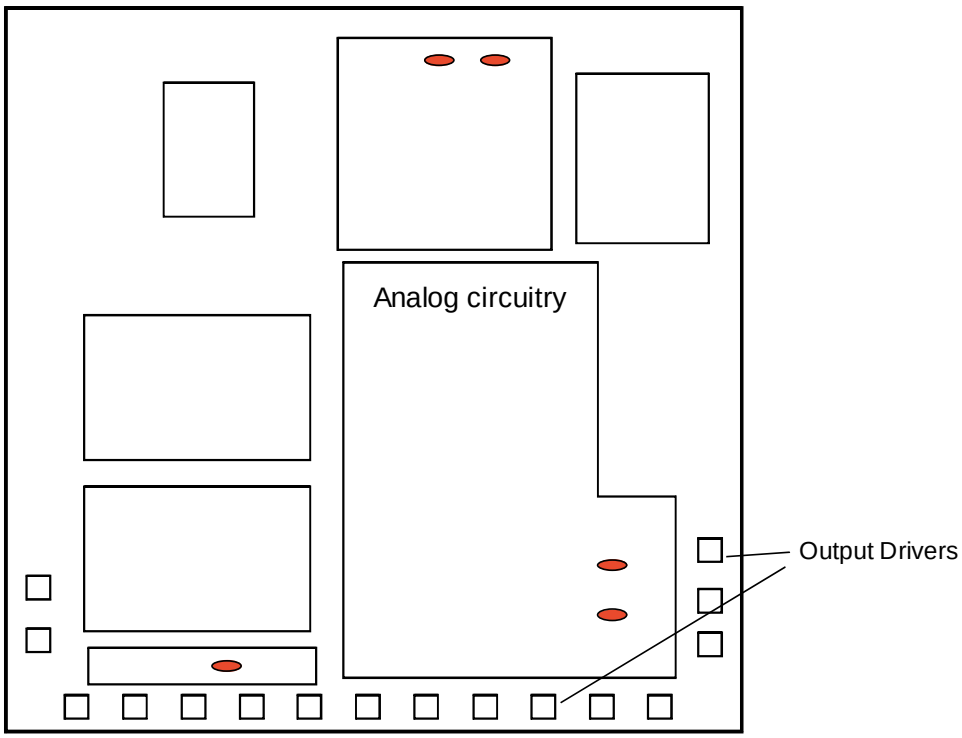

Figure 7. Latchup regions in the AD9240 as determined by thermal imaging after several different tests with californium. Thermal imaging was not done during tests at the accelerators because of the cost for the "dead" time required to continually interrupt radiation testing to do the thermal imaging.

Although other mechanisms such as snapback [19,20] can also cause circuit malfunctions when devices are irradiated with heavy ions, generally the current involved in snapback is much lower because it involves only current within a single parasitic transistor and does not require large currents in the substrate. The magnitude of the currents observed in our tests along with the thermal signature observed with thermal imaging support the conclusion that these events are due to latchup, not snapback.

IV. Characterization Issues for Complex Circuits

The detailed work on this device illustrates the complexity of latchup in modern devices. A number of issues have to be considered.

First, for devices with bulk substrates it is essential that the effective range of the ions used for testing is above 40 μm because charge collection occurs deep within the substrate. That requirement limits the ability to use tests on tilted devices to increase effective LET. If the beam has insufficient range, the cross section will be considerably lower when tests are done at angle.

Second, current limiting has to be used very cautiously when latchup characterization tests are done. If the current limit is too low it may prevent some latchup events from occurring, underestimating the cross section. For the AD9240, current limiting of the digital power supply caused the analog section to be loaded down when latchup occurred in the digital region, erroneously indicating that all latchup events occurred in the analog region of the circuit. Subsequent tests with higher current limits showed that latchup could occur in the digital as well as analog regions of the devices.

Third, temperature is an important consideration because the latchup cross section and threshold LET are strongly affected by temperature. Latchup testing must be done at the highest temperature that the part will encounter in applications. Even moderate temperature increases -- 30 to 40 C -- can significantly alter the threshold LET and cross section for latchup.

Fourth, the behavior of the AD9240 circuit during latchup illustrates how difficult it is to provide the necessary detailed characterization of latchup modes and currents for complex parts. There are many different regions that can latch, and it is necessary to observe very large numbers of latchup events with several different types of ions in order to get the proper picture of how latchup affects different regions of the part. Using power supply current detection and shutdown as a circumvention method is very difficult for a device of this type because of the large number of different latchup paths that are present in the circuit along with the wide range of currents that occur for different latchup paths. It is necessary to monitor all power supplies and to consider variations in nominal operating current for different units and operating conditions in order to establish detection limits.

Work on more recent devices has shown that latchup continues to be an important issue, even for advanced devices with epitaxial substrates. Although the principles of latchup are well understood, the inherent dependence on device topology and power distribution increases the difficulty of testing and characterizing devices that are sensitive to latchup. Thermal imaging is a valuable tool to determine which regions of a device are involved in latchup that is applicable to devices with extensive metallization coverage that is inconsistent with laser diagnostic methods.

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