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SUPERSEDING
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PERFORMANCE SPECIFICATION

CAPACITOR, CHIP, MULTIPLE LAYER, FIXED,
CERAMIC DIELECTRIC, ESTABLISHED RELIABILITY
AND NON-ESTABLISHED RELIABILITY,
GENERAL SPECIFICATION FOR

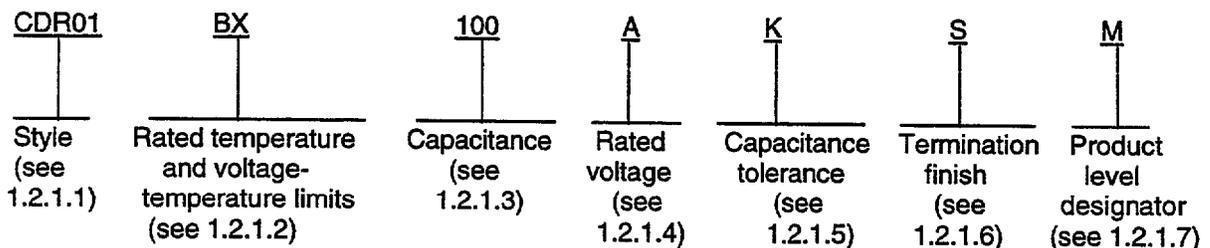
This specification is approved for use by all Departments
and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for non-established reliability (non-ER) and established reliability (ER), ceramic dielectric, multiple layer, chip capacitors. ER capacitors covered by this specification have failure rate levels (FRL) ranging from 1.0 percent to 0.001 percent per 1,000 hours. These FRLs are established at a 90-percent confidence level and maintained at a 10-percent producer's risk and are based on life tests performed at maximum rated voltage at maximum rated temperature. An acceleration factor of 8:1 has been used to relate life test data obtained at 200 percent of rated voltage at maximum rated temperature, to rated voltage at rated temperature.

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). The PIN is in the following form, and as specified (see 3.1).



Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: U.S. Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LEO-E-EP, Fort Monmouth, NJ 07703-5023, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document, or by letter.

AMSC N/A
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

FSC 5910

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1.2.1.1 Style. The style is identified by the three-letter symbol "CDR" followed by a two-digit number. The letters identify non-ER and ER, ceramic dielectric, fixed, chip capacitors.

1.2.1.2 Rated temperature and voltage-temperature limits. The rated temperature and voltage-temperature limits are identified by a two-digit symbol. The first letter "B" indicates the rated temperature of -55°C to +125°C; the second letter indicates the voltage-temperature limits as shown in table I.

TABLE I. Voltage-temperature limits.

Symbol	Capacitance change with reference to +25°C		
	Step A through step D of table XIII	Percent rated voltage	Step E through step G of table XIII
G	90 ± 20 ppm/°C	100	90 ± 20 ppm/°C
P <u>1/</u>	0 ± 30 ppm/°C	100	0 ± 30 ppm/°C
R	± 15 percent	100	+15, -40 percent
X	± 15 percent	100	+15, -25 percent
Z	± 15 percent	60	+15, -45 percent

1/ At measurement point F of table XIII, the capacitance measurement may be ± 0.1 percent or ± 0.05 pF, whichever is greater, from the +25°C reference.

1.2.1.3 Capacitance. The nominal capacitance value expressed in picofarads (pF) is identified by a three-digit number; the first two digits represent significant figures and the last digit specifies the number of zeros to follow. When the nominal value is less than 10 pF, the letter "R" is used to indicate the decimal point and the succeeding digit(s) of the group represent significant figure(s). For example, 1R0 indicates 1.0 pF and OR5 indicates 0.5 pF.

1.2.1.4 Rated voltage. The rated voltage for continuous operation at +125°C is identified by a single letter as shown in table II.

TABLE II. Rated voltage.

Symbol	Rated voltage
A	50
B	100
K	150
C	200
D	300
E	500
F	1,000
G	2,000
H	3,000
J	4,000

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1.2.1.5 Capacitance tolerance. The capacitance tolerance is identified by a single letter as shown in table III.

TABLE III. Capacitance tolerance.

Symbol ^{1/}	Capacitance tolerance (±)
B	.10 pF
C	.25 pF
D	.50 pF
F	1 percent
G	2 percent
J	5 percent
K	10 percent
M	20 percent

^{1/} Symbols B, C, and D are applicable for capacitance values of less than 10 pF only. For capacitance values of .10 pF through .50 pF, the capacitance will never be zero.

1.2.1.6 Termination finish. The termination finish is identified by a single letter as shown in table IV.

TABLE IV. Termination finish.

Symbol	Finish
M	Palladium-silver
N ^{1/}	Silver-nickel-gold
P	Silver-copper-gold
Q	Palladium-gold
S	Solder coated, final
T	Silver
U	Base metallization-barrier metal-solder coated ^{2/} ^{3/}
W ^{3/} ^{4/}	Base metallization-barrier metal-tinned (tin or tin/lead alloy)
Y ^{4/}	Base metallization-barrier metal-tin (100 percent) ^{3/}
Z	Base metallization-barrier metal-tinned (tin/lead alloy, with a minimum of 4 percent lead) ^{3/}

^{1/} See 6.4.1.

^{2/} Solder will have a melting point of +200°C or less. Solder coat thickness will be a minimum of 60 microinches.

^{3/} At the option of the user, U, W, Y, and Z termination finishes may be substituted for the other termination finishes. W and Y termination finishes are not substitutable for Z termination finish.

^{4/} See 6.11.

1.2.1.7 Product level designator. The product level designator is identified by a single letter as shown in table V.

TABLE V. Product level designator.

Symbol	Product level
C	non-ER
M	1.0
P	0.1
R	0.01
S	0.001

1/ Failure rate (FR) in percent/1,000 hours.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of the documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

DEPARTMENT OF DEFENSE

(See supplement 1 for list of associated specification sheets.)

STANDARDS

DEPARTMENT OF DEFENSE

- MIL-STD-202 - Electronic and Electrical Component Parts, Test Methods for.
- MIL-STD-690 - Failure Rate Sampling Plans and Procedures.
- MIL-STD-790 - Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications.
- MIL-STD-810 - Environmental Test Methods and Engineering Guidelines.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from Defense Printing Service Detachment Office, Building 4D (Customer Service), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

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2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation (see 6.2).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

- ANSI/J-STD-004 - Requirements for Soldering Fluxes.
- ANSI/J-STD-005 - Requirements for Soldering Pastes.
- ANSI/J-STD-006 - Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications.

(Application for copies should be addressed to the American National Standards Institute (ANSI), 11 West 42nd Street, New York, NY 10036-0609.)

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

- EIA-554-1 - Assessment of Average Outgoing Quality Levels in Parts Per Million (ppm).(DoD Adopted).
- EIA-557 - Statistical Process Control Systems. (DoD Adopted).

(Application for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated specifications, specifications sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheets. In the event of any conflict between requirements of this specification and the specification sheet, the latter shall govern (see 6.2).

3.2 Qualification. Capacitors furnished under this specification shall be products which are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award. In addition, the manufacturer shall obtain certification from the qualifying activity that the product assurance requirements of 4.2 have been met and are being maintained. Authorized distributors who are approved to MIL-STD-790 distributor requirements by the QPL manufacturer are listed in the QPL.

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-690 (ER parts only) and MIL-STD-790. In addition, the manufacturer shall establish a Statistical Process Control (SPC) and Part Per Million (ppm) system that meets the requirements specified in 3.3.1 and 3.3.2.

3.3.1 SPC system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a SPC system that meets the requirements of EIA-557. The manufacturer shall demonstrate control of the voltage-temperature limits of capacitance in the process.

3.3.2 PPM system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a ppm system for assessing the average outgoing quality of lots in accordance with EIA-554-1. Data exclusion, in accordance with EIA-554-1 may be used with approval of the qualifying activity. The ppm system shall identify the ppm rate at the end of each month and shall be based on a six month moving average. Style reporting may include both non-ER and ER style combinations.

3.4 Material. The material shall be as specified herein. However, when a definite material is not specified, a material shall be used which enables the capacitors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guarantee of the acceptance of the finished product.

3.4.1 Soldering flux. Soldering flux shall be in accordance with ANSI/J-STD-004. No acid, acid salts, or type RA fluxes shall be used in preparation for or during soldering.

3.5 Interface and physical dimension requirements. Capacitors shall meet the interface requirements and physical dimensions specified (see 3.1).

3.5.1 Terminations. The terminations shall be of solderable metals or metal alloys. Termination finishes, as identified in 1.2.1.6, shall be as specified (see 3.1).

3.5.1.1 Reprocessing of terminations for solderability enhancement. The manufacturer may reprocess the terminations of capacitors supplied to this specification for the purpose of solderability enhancement, provided the termination process has been approved by the qualifying activity.

3.5.1.1.1 Reprocessing option. If the manufacturer reprocesses the terminations of the capacitors as a part of normal production, or as a corrective action for solderability failure, the reprocessed lot shall be subjected to the group A, subgroup 1, electrical tests.

3.6 Voltage conditioning. When tested as specified in 4.8.3, capacitors shall meet the following requirements:

- a. Dielectric withstanding voltage (DWV) (at +25°C): Shall be as specified in 3.12, with the following exceptions:
 - (1) For capacitors with a voltage rating of 500 volts, 150 percent of rated voltage shall be applied.
 - (2) For capacitors with a voltage rating of 1,000 volts or greater, 120 percent of rated voltage shall be applied.
 - (3) Not applicable if the optional voltage conditioning was performed at or above 250 percent of rated voltage.
- b. Insulation resistance (IR) (at +25°C): Shall be as specified in 3.9.

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c. Capacitance (at +25°C): Shall be as specified in 3.7.

d. Dissipation factor (DF) (at +25°C): Shall be as specified in 3.8.

3.7 Capacitance. When measured as specified in 4.8.4, the capacitance shall be within the applicable tolerance specified (see 3.1).

3.8 DF. When measured as specified in 4.8.5, the DF shall not exceed 2.5 percent for the BR, BX, and BZ characteristics, 0.15 percent for the BP characteristic, and 0.05 percent for the BG characteristic.

3.9 IR. When measured as specified in 4.8.6, the IR shall be not less than the following:

a. At +25°C (except high frequency styles) (see 3.1): 100,000 megohms or 1,000 megohm-microfarads, whichever is less.

b. At +125°C (except high frequency styles) (see 3.1):

(1) BR, BX, and BZ characteristics: Shall be not less than 10,000 megohms or 100 megohm-microfarads, whichever is less (see 3.1).

(2) BP characteristic: Shall be not less than 1,000 megohms or 10 megohm-microfarads, whichever is less (see 3.1).

(3) BG characteristic: Shall be as specified (see 3.1).

3.10 Equivalent series resistance (ESR) (UHF) (when specified, see 3.1). When tested in accordance with 4.8.7, the ESR shall be less than the limits shown in appendix A, figure 3 and figure 4.

3.11 ESR (RF) (when specified, see 3.1). When tested in accordance with 4.8.8, the ESR shall be less than the limits shown in appendix A, figure 5 and figure 6.

3.12 DWV. When capacitors are tested as specified in 4.8.9, there shall be no evidence of breakdown or visible evidence of arcing or damage.

3.13 Solderability.

3.13.1 Nonleaded capacitors. Capacitors shall be tested as specified in 4.8.10. Nonbarrier metal capacitors shall utilize Pb36B solder; barrier metal capacitors (types U, W, Y, and Z) shall utilize Sn60A, Pb36B, or Sn63A solder (see 3.1) in accordance with ANSI/J-STD-006, and the immersed metallized surface shall be at least 85 percent covered with a smooth solder coating. The remaining 15 percent of the surface may contain small pinholes or exposed termination material; however, these shall not be concentrated in one area.

3.13.2 Leaded capacitors. When leaded capacitors are tested as specified in 4.8.10, the dipped surface of the leads shall be at least 90 percent covered with a new, smooth solder coating. The remaining 10 percent may contain only small pinholes or rough spots, and these shall not be concentrated in one area. Bare base metal where the solder dip failed to cover the original coating is an indication of poor solderability and shall be cause for failure. In case of dispute, the percentage of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area.

3.14 Voltage-temperature limits (not applicable to high frequency capacitors). When capacitors are tested as specified in 4.8.11, the capacitance change shall not exceed the applicable limits specified in table I.

3.15 Thermal shock and immersion. When tested as specified in 4.8.12, capacitors shall meet the following requirements:

- a. Visual examination: There shall be no mechanical damage.
- b. DWV: Shall be as specified in 3.12.
- c. IR (at +25°C): Shall be not less than 30 percent of the initial requirement (see 3.9).
- d. Capacitance change:
 - (1) BR, BX, and BZ characteristics: Shall change not more than ± 10 percent from the initial measured value.
 - (2) BG and BP characteristics: Shall change not more than 0.5 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.
- e. DF: Shall be as specified in 3.8.

3.16 Resistance to soldering heat. When tested as specified in 4.8.13, capacitors shall meet the following requirements:

- a. Visual examination: There shall be no evidence of mechanical damage or delamination or exposed electrodes. Leaching shall be a maximum of 25 percent on each edge of mounting area (see figure 1).
- b. IR (at +25°C): Shall not be less than the initial 25°C requirement.

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- c. Capacitance change:
 - (1) BR, BX, and BZ characteristics: Shall change not more than -1.0 percent to +6.0 percent from the initial measured value.
 - (2) BG characteristic: Shall change not more than 0.5 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.
 - (3) BP characteristic: Shall change not more than -1.0 percent to +2.0 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.
- d. DF: Shall not exceed the initial limits.

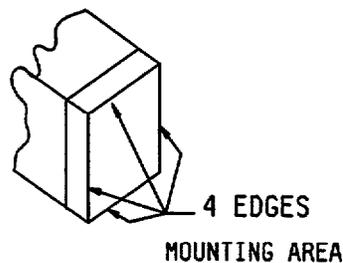


FIGURE 1. Mounting areas

3.17 Moisture resistance. When tested as specified in 4.8.14, capacitors shall meet the following requirements:

- a. Visual examination: There shall be no mechanical damage, and marking shall remain legible.
- b. DWV: Shall be as specified in 3.12.
- c. IR (at +25°C): Shall be not less than 30 percent of the initial requirement (see 3.9).
- d. Capacitance change:
 - (1) BR, BX, and BZ characteristics: Shall change not more than ± 10 percent from the initial measured value.
 - (2) BP and BG characteristics: Shall change not more than 0.5 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.

3.18 Humidity, steady state, low voltage. When tested as specified in 4.8.15, capacitors shall meet the following requirements:

- a. Visual examination: There shall be no mechanical damage, and marking shall remain legible.
- b. IR (at +25°C): Shall meet the initial 25°C requirement specified in 3.9.
- c. Capacitance change:
 - (1) BR, BX, and BZ characteristics: Shall not change more than ± 10 percent from the initial measured value.
 - (2) BP and BG characteristics: Shall not change more than 0.3 percent of the nominal value or 0.3 pF, whichever is greater, from the initial measured value.

3.19 Life (at elevated ambient temperature). When tested as specified in 4.8.16, capacitors shall meet the following requirements:

- a. Visual examination: There shall be no mechanical damage.
- b. IR:
 - (1) (At +25°C): Shall be not less than 30 percent of the initial requirement (see 3.9).
 - (2) (At maximum rated temperature): Shall be not less than 30 percent of the initial requirement (see 3.9).
- c. Capacitance change:
 - (1) BR, BX, and BZ characteristics: Less than ± 10 percent from the initial measured value.
 - (2) BP and BG characteristics: Shall change not more than 2.0 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.
- d. DF:
 - (1) BR, BX, and BZ characteristics: Less than 3.0 percent.
 - (2) BP and BG characteristics: Less than 0.2 percent.

3.20 Fungus. The manufacturer shall certify that all materials are fungus resistant or shall perform the test specified in 4.8.17. When capacitors are tested as specified in 4.8.17, examination shall not disclose evidence of fungus growth or damage.

3.21 Series resonance (when specified, see 3.1). When tested as specified in 4.8.18, capacitors shall meet or exceed the series resonance frequency as shown on figure 2.

3.22 Terminal strength (when specified, see 3.1). When capacitors are tested as specified in 4.8.19, there shall be no loosening, rupturing, or permanent damage to the terminals.

3.23 Temperature coefficient and capacitance drift (high frequency capacitors only).

3.23.1 Temperature coefficient. When capacitors are tested as specified in 4.8.20, the capacitance change shall not exceed the applicable limits specified in table I.

PPM per °C can be calculated with the following equation:

$$\text{PPM}^\circ\text{C} = \frac{C_2 - C_1}{C_1(T_2 - T_1)} \times 10^6, \text{ where: } \begin{array}{l} C_2 = \text{Capacitance at test temperature} \\ C_1 = \text{Capacitance at } 25^\circ\text{C} \\ T_2 = \text{Test temperature} \\ T_1 = 25^\circ\text{C} \end{array}$$

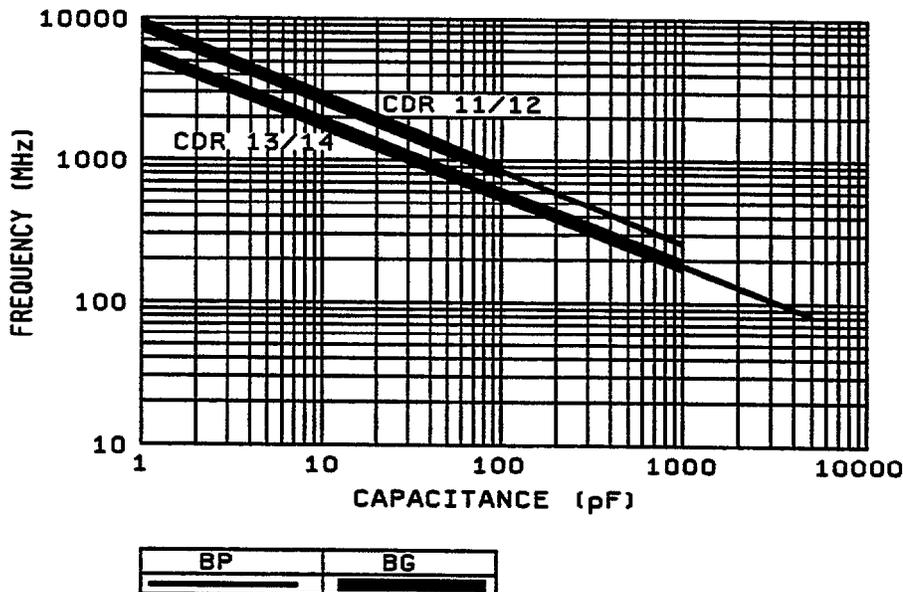


FIGURE 2. Series resonance frequency versus nominal capacitance value.

3.23.2 Capacitance drift. The capacitance drift shall be within \pm (0.2 percent or 0.05pF), whichever is greater.

3.24 Marking (all styles except high frequency). Packaging containers shall be marked with the PIN, capacitance, capacitance tolerance, voltage, "JAN" brand, lot date code, and the Commercial and Government Entity (CAGE) code. Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited. When specified in the ordering data capacitors shall be legibly marked in accordance with table VI (see 6.2). A two character marking system shall be used. The first character shall be an alphabetic symbol and shall designate the first and second significant figures. The second character shall be a numerical digit and shall designate the decimal multiplier of capacitance in pF (Examples: A1 = $1 \times 10^1 = 10$ pF; J5 = $2.2 \times 10^5 = 0.22 \times 10^6 = 0.22$ μ F).

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The marking shall appear in black or legible contrast. The size and orientation of the marking shall be at the option of the manufacturer. At the option of the manufacturer, the capacitor may be laser marked with the manufacturer's trademark or symbol and the capacitance code in accordance with table VI. Additional marking may appear provided that it does not interfere with the required marking.

TABLE VI. Marking for chip capacitors.

First character				Second character	
Alphabetic character	Significant figures	Alphabetic character	Significant figures	Numerical character	Decimal multiplier
A	1.0	T	5.1	0	10 ⁰
B	1.1	U	5.6	1	10 ¹
C	1.2	V	6.2	2	10 ²
D	1.3	W	6.8	3	10 ³
E	1.5	X	7.5	4	10 ⁴
F	1.6	Y	8.2	5	10 ⁵
G	1.8	Z	9.1	6	10 ⁶
H	2.0	a	2.5	7	10 ⁷
J	2.2	b	3.5	8	10 ⁸
K	2.4	d	4.0	9	10 ⁹
L	2.7	e	4.5		
M	3.0	f	5.0		
N	3.3	m	6.0		
P	3.6	n	7.0		
Q	3.9	t	8.0		
R	4.3	y	9.0		
S	4.7				

3.24.1 Marking (styles CDR11, CDR12, CDR13, CDR14, CDR21, CDR22, CDR23, CDR24, and CDR25). These capacitors shall be marked with a contrasting color dot placed on the side of the capacitor to indicate the vertical plate orientation to that side. When parts are laser marked, the marking shall be on the surface which is parallel to the plane of the embedded electrodes (this is the larger area which is normally the imprint area). If the capacitor is so marked, the vertical plate orientation is defined; therefore, the contrasting color dot on the capacitor to indicate the vertical plate orientation to that side may be an option.

Capacitors may be laser marked with the manufacturer's trademark or symbol, the two-digit or three-digit capacitance code, and the tolerance code as follows:

XXX
100 (or A1 for two-digit)
F

or

XXX
100F (or A1F for two-digit)

Where space does not permit, the manufacturer's trademark or symbol may be omitted.

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3.24.2 Substitutability of product levels. A manufacturer may supply to those product levels, as listed in table VII, with failure rates (FR) higher than that to which they are qualified. Parts with lower FRs are substitutable, with the acquiring agency approval, for higher FR parts, provided the lot date codes of the parts are not changed.

TABLE VII. Product level substitutability.

Parts qualified to product level	Are substitutable for product level
S (.001)	C, M, P, and R
R (.01)	C, M, and P
P (.1)	M, C
M (1)	C
C	NA

3.24.3 Substitutability of capacitance tolerance and rated voltage. Parts qualified and marked (if applicable) to tighter capacitance tolerance or qualified to a higher rated voltage are substitutable, with acquiring agency approval, for parts qualified and marked (if applicable) to looser capacitance tolerance, or qualified to a lower rated voltage, provided all other values, such as case size, characteristic, and leads or terminations remain the same. The substitutable parts shall not be remarked (if applicable) unless specified in the contract or order (see 6.2). In the event the capacitance tolerance is changed and remarked (if applicable) or the voltage rating is changed, the lot date codes of the parts shall not be changed and the workmanship criteria shall be met.

3.24.4 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to and meeting all of the criteria specified herein and in applicable specifications shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets or associated specifications, the manufacturer shall remove completely the military part number and the "JAN" or the "J" from the sample tested and also from all items represented by the sample. The "JAN" or "J" certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 504,860 for the certification mark "JAN" and Registration Number 1,586,261 for the certification mark "J".

3.25 Recycling and waste prevention. Recovered materials or environmentally preferable materials shall be used wherever possible without jeopardizing the intended use of the item.

3.26 Workmanship. Capacitors shall be so processed that when inspected under 20X to 40X magnification, they shall be uniform in quality and shall be free from pits, cracks, rough edges, adhered foreign material, and other defects which will affect life or serviceability. The capacitors shall exhibit no delamination (separation in the layers of ceramic) or demetallization (lift-off) on the terminations.

4. VERIFICATION

4.1 Classification of inspections. The inspections specified herein are classified as follows:

- a. Qualification inspection (see 4.4).
- b. Verification of qualification (see 4.5).
- c. Conformance inspection (see 4.6).
- d. Periodic group C inspection (see 4.7).

4.2 QPL system. The manufacturer shall establish and maintain a system to meet the requirements of MIL-STD-790 and the requirements herein (see 3.3). Evidence of such compliance shall be verified by the qualifying activity as a prerequisite for qualification and retention of qualification.

4.3 Inspection conditions and methods.

4.3.1 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the "GENERAL REQUIREMENTS" of MIL-STD-202.

4.3.2 Methods.

4.3.2.1 Reference measurements. When requirements are based on comparative measurements made before and after conditioning, the reference measurement shall be considered the last measurement made at $+25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ prior to conditioning. Unless reference measurements have been made within 30 days prior to the beginning of conditioning, they shall be repeated.

4.3.3 Power supply. The power supply used for life testing shall have a regulation of ± 2 percent, or less, of the applicable applied test voltage. The power supply used for dc leakage current or IR measurements shall be stabilized to at least ± 100 ppm. No voltage fluctuations shall occur during measurements that would produce a variation in the current or resistance measurement.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3) on sample units produced with equipment and procedures normally used in production.

4.4.1 Sample size. The number of sample units comprising a sample of capacitors to be submitted for qualification inspection shall be as specified in table VIII, or in appendix B to this specification. The sample shall be taken from a production run and shall be produced with equipment and procedures normally used in production.

4.4.2 Inspection routine. Sample units shall be subjected to the qualification inspection specified in table VIII, in the order shown. All sample units shall be subjected to the group I tests. These sample units shall then be divided as shown in table VIII for groups II through VIII, and subjected to the tests for their particular group.

4.4.3 Failures. Failures in excess of those allowed in table VIII shall be cause for refusal to grant qualification approval.

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TABLE VIII. Qualification inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of defectives permitted
Group I				
Voltage conditioning	3.6	4.8.3	85 <u>2/</u> <u>3/</u>	Not applicable
DWV	3.12	4.8.9		
IR (elevated temperature) <u>1/</u>	3.9	4.8.6		
Capacitance <u>1/</u>	3.7	4.8.4		
Dissipation factor <u>1/</u>	3.8	4.8.5		
IR <u>1/</u>	3.9	4.8.6		
ESR (UHF) (high frequency only) <u>4/</u>	3.10	4.8.7		
ESR (RF) (high frequency only) <u>4/</u>	3.11	4.8.8		
DWV	3.12	4.8.9		
Visual and mechanical examination	3.1, 3.4, 3.5.1, 3.24 through 3.26 inclusive	4.8.2		
Group II				
Solderability	3.13	4.8.10	6	
Group III				
Voltage-temperature limits <u>5/</u>	3.14	4.8.11	18	1
Temperature coefficient and capacitance drift (high frequency only)	3.23	4.8.20		
Thermal shock and immersion	3.15	4.8.12		
Group IV				
Resistance to soldering heat	3.16	4.8.13	9	
Moisture resistance	3.17	4.8.14	9	
Group V				
Life (at elevated ambient temperature)	3.19	4.8.16	25	1
Group VI				
Fungus <u>2/</u>	3.20	4.8.17	6	0
Group VII				
Series resonance (when specified, see 3.1)	3.21	4.8.18	18 <u>3/</u>	0
Terminal strength (when specified, see 3.1)	3.22	4.8.19		
Group VIII				
Humidity, steady state, low voltage	3.18	4.8.15	12	0

1/ Performed as part of the voltage conditioning test.

2/ Only 79 samples are needed if certification is given for fungus (see 3.20).

3/ When group VII inspection is specified, 18 additional samples will be required.

4/ Not applicable to high frequency styles below 1 pF.

5/ Not applicable to high frequency capacitors.

4.4.4 FRL and quality level verification.

4.4.4.1 FR qualification and lot conformance FR inspection. FR qualification and lot conformance FR inspection shall be in accordance with the general and detailed requirements of MIL-STD-690 and the following details:

- a. Procedure I: Qualification at the initial FR level. Level M (1.0 percent) of FRSP-90 shall apply. Sample units shall be subjected to the qualification inspection specified in group I, table VIII (see 4.4.2).
- b. Procedure II: Extension of qualification to lower FR levels. To extend qualification to the P (0.1 percent), R (0.01 percent), and S (0.001 percent) FR levels, two or more voltages within a style and of similar construction may be combined. For FR levels R and S, two or more styles of similar construction (see 4.6.1.1.1) may be combined.
- c. Procedure III: Maintenance of FR level qualification. Maintenance period B of FRSP-10 shall apply. Regardless of the number of production lots produced during this period, the specified number of unit hours shall be accumulated to maintain qualification.

4.4.4.2 Quality level verification. The manufacturer is responsible for establishing a quality system to assess the ppm defect level of lots. The ppm defect level shall be based on a 6-month moving average. The following groupings of styles shall be used for the maintenance of ppm defect level:

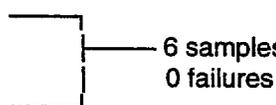
<u>Group</u>	<u>Styles</u>
1	CDR01, CDR02, CDR03, CDR04, CDR05, CDR06, CDR31, CDR32, CDR33, CDR34, CDR35
2	CDR11, CDR12, CDR13, CDR14, CDR21, CDR22, CDR23, CDR24, CDR25
3	CDR26, CDR27, CDR28, CDR29, CDR30

4.5 Verification of qualification. Every 6 months, the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification shall be based on meeting the following requirements:

- a. MIL-STD-790 program.
- b. The capacitor design has not been modified.
- c. Lot rejection for group A inspection does not exceed 10 percent or one lot, whichever is greater.
- d. Periodic group C inspection.
- e. Verification of FRLs.
- f. PPM assessment. This information shall be submitted in accordance with style groupings listed in 4.4.4.2.
- g. Continued qualification to non-ER (C level) shall be based upon continued maintenance of qualification for the ER part (FRL P).

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TABLE IX. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
<u>Subgroup 1</u> Voltage conditioning <u>1/</u>	3.6	4.8.3	100 percent inspection
<u>Subgroup 2</u> IR (elevated temperature) (+125°C) Visual and mechanical examination <u>2/</u>	3.9	4.8.6	Table X, column A
<u>Subgroup 3</u> ESR (UHF) (when specified, see 3.1) <u>3/</u> ESR (RF) (when specified, see 3.1) <u>3/</u>	3.1, 3.4, 3.5 3.5.1, 3.24 through 3.26 inclusive	4.8.2	Table X, column B
<u>Subgroup 4</u> Solderability <u>4/</u>	3.10	4.8.7	
	3.11	4.8.8	
	3.13	4.8.10	13 samples 0 failures

1/ For CDR11 through CDR14 and CDR21 through CDR25 capacitors of less than 10 pF, the DF shall not exceed 0.25 percent for the BP characteristic and 0.15 percent for the BG characteristic. A negative reading is not considered a failure.

2/ The manufacturer may request the deletion of the subgroup 2, visual and mechanical examination, provided an in-line or process control system for assessing and assuring the visual and mechanical requirements are met, can be validated and approved by the qualifying activity. Deletion of this examination does not relieve the manufacturer from meeting these requirements.

3/ Not applicable to styles CDR11 through CDR14 and CDR21 through CDR25 below 1 pF.

4/ The manufacturer may request the deletion of the subgroup 4 solderability test, provided an in-line or process control system for assessing and assuring the solderability of leads can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement.

TABLE X. Sampling plans for subgroup 2.

Lot size	Sample Size	
	A	B
1 - 13	100%	100%
14 - 125	100%	13
126 - 150	125	13
151 - 280	125	20
281 - 500	125	29
501 - 1,200	125	34
1,201 - 3,200	125	42
3,201 - 10,000	192	50
10,001 - 35,000	294	60
35,001 - 150,000	294	74
50,001 - 500,000	345	90
500,001 - up	435	102

4.6.1.2.3.1 Manufacturer's production inspection. If the manufacturer performs tests equal to or more stringent than those specified in subgroup 1, table IX, as the final step of the production process, group A, subgroup 1 inspection may be waived. Authority to waive the subgroup 1 inspection shall be granted by the qualifying activity only. The following criteria shall be complied with:

- a. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than that specified for subgroup 1. Test conditions shall be equal to or more stringent than those specified for subgroup 1 tests. (NOTE: Includes optional voltage conditioning (see 4.7.3.2)).
- b. Manufacturer subjects 100 percent of the product supplied under this specification to his production tests.
- c. The parameters measured and the failure criteria shall be the same or more stringent than those specified herein.
- d. The lot rejection criteria is the same or more stringent than that specified herein.
- e. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification and concurrence by the qualifying activity.

4.6.1.2.3.2 Rejected lots. Production lots exceeding the eight percent defective allowance (PDA) of group A, subgroup 1 inspection shall be segregated from new lots and lots that have passed inspection. Lots rejected may be offered for acceptance only if the manufacturer 100 percent retests to the requirements of subgroup 1. Resubmitted lots shall be kept separate and shall be clearly identified as resubmitted lots. If, during the 100 percent reinspection to subgroup 1, the lot exceeds 3 percent defective, the lot shall be rejected and shall not be resubmitted.

4.6.1.2.4 Subgroup 2 tests.

4.6.1.2.4.1 Sampling plans. Subgroup 2 tests shall be performed on an inspection lot basis. Samples subjected to subgroup 2 shall be selected in accordance with table X, based on the size of the inspection lot. In the event of one or more failures the lot shall be rejected.

4.6.1.2.4.2 Rejected lots. The rejected lot shall be segregated from new lots and those lots that have passed inspection. The rejected lot shall be 100 percent inspected for those quality characteristics found defective in the sample and any defectives found removed from the lot. A new sample of parts shall then be randomly selected in accordance with table X. If one or more defects are found in this second sample, the production lot shall be rejected and shall not be supplied to this specification.

4.6.1.2.5 Subgroup 3 tests. Subgroup 3 shall be performed on an inspection lot basis. The sampling procedure shall be as specified in table IX.

4.6.1.2.5.1 Rejected lots. The rejected lots shall be segregated from new lots and those lots that have passed inspection. Lots rejected because of failures in subgroup 3 shall be reinspected, using the sampling procedure specified in table IX. If one or more defects are found in the second sample, the lot shall be rejected and shall not be supplied to this specification. Resubmitted lots shall be kept separate from new lots, and shall be identified as resubmitted lots.

4.6.1.2.6 Subgroup 4 (solderability).

4.6.1.2.6.1 Sampling plan. Thirteen samples shall be selected randomly from every inspection lot and subjected to the subgroup 4 solderability test. The manufacturer may use electrical rejects from the subgroup 1 screening tests for all or part of the samples to be used for the solderability testing. If there are one or more defects, the lot shall be considered to have failed.

4.6.1.2.6.2 Rejected lots. In the event of one or more defects, the inspection lot shall be rejected. The manufacturer may use one of the following options to rework the lot:

- a. Each production lot that was used to form the failed inspection lot shall be individually submitted to the solderability test as required in 4.6.1.2.6.1. Production lots failing the solderability test can be reworked only if submitted to the reprocessing procedure in 4.6.1.2.6.2b.
- b. The manufacturer shall submit the failed production lot to 100 percent reprocessing of the terminations, using an approved process in accordance with 3.5.1.1. Following the reprocessing, the electrical measurements required in the group A, subgroup 1 test shall be repeated on 100 percent of the lot. The PDA for electrical measurements shall be as for the subgroup 1 tests. Thirteen additional samples shall then be selected and subjected to the solderability test with no defects allowed. If the lot fails this solderability test, the lot shall be considered rejected and shall not be furnished against the requirements of this specification.

4.6.1.2.6.3 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract.

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4.6.1.2.7 PPM calculations. The manufacturer shall establish a ppm system in accordance with 3.3.2 for assessing and calculating average outgoing quality of capacitors. A ppm rate combining capacitance, DF, IR (25°C), and DWV shall be assessed for lots that have passed the group A inspection. The manufacturer's ppm system shall also address rectification procedures for lots failing ppm assessment. Data from the rectification process shall not be used to calculate ppm.

4.7 Periodic group C inspection (ER only). Periodic inspection shall consist of the group C inspection tests specified in table XI, in the order shown. Group C inspection shall be performed on sample units randomly selected from inspection lots which have passed group A inspection. Except where the results of periodic inspection show noncompliance with the applicable requirements (see 4.7.2), delivery of products which have passed group A inspection shall not be delayed pending the results of this periodic inspection.

4.7.1 Sampling plan.

4.7.1.1 Subgroup 1, subgroup 2, and subgroup 5 (all FR levels). Thirty-six sample units of each voltage-temperature characteristic shall be selected from the first inspection lot produced every 6 months.

4.7.1.2 Subgroup 3 (all FR levels). A minimum of 25 sample units per style of the highest capacitance value produced shall be selected from the first inspection lot produced during a 6-month period. Permitted failures shall be as specified in MIL-STD-690. The accumulated data shall be used for maintenance and extension of FR qualification.

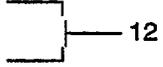
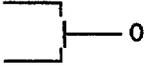
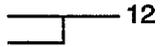
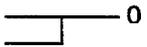
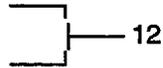
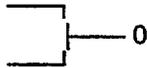
4.7.1.3 Subgroup 4 (all FR levels) (high frequency only). Twelve sample units of each voltage-temperature characteristic shall be selected from the first lot produced.

4.7.1.4 Disposition of sample units. Sample units which have been subjected to group C inspection shall not be delivered on the contract or order.

4.7.2 Noncompliance. If a sample fails to pass group C inspection, the manufacturer shall notify the qualifying activity and cognizant inspection activity of such failure and take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same materials, and which are considered subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the qualifying activity has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspection, or the inspection which the original sample failed, at the option of the qualifying activity). Group A inspection may be reinstated; however, final acceptance and shipment shall be withheld until the group C inspection has shown that the corrective action was successful.

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TABLE XI. Group C inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of defectives permitted
<u>Subgroup 1</u> Temperature coefficient and capacitance drift Voltage-temperature limits <u>1/ 2/</u> Thermal shock and immersion <u>3/</u>	3.23 3.14 3.15	4.8.20 4.8.11 4.8.12	 12	 0
<u>Subgroup 2</u> Resistance to soldering heat Moisture resistance	3.16 3.17	4.8.13 4.8.14	 12	 0
<u>Subgroup 3</u> Life (at elevated ambient temperature)	3.19	4.8.16	25 minimum	See 4.7.1.2
<u>Subgroup 4</u> Terminal strength (when specified, see 3.1) <u>3/</u> Series resonance (when specified, see 3.1)	3.22 3.21	4.8.19 4.8.18	 12	 0
<u>Subgroup 5</u> Humidity, steady state, low voltage <u>4/</u>	3.18	4.8.15	12	0

- 1/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, the frequency of this test, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, construction or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency.
- 2/ Not applicable to high frequency capacitors.
- 3/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, this test, with the approval of the qualifying activity, can be deleted. The manufacturer, however, shall perform this test every three years after the deletion as part of long term design verification. If the design, material, construction or processing of the part is changed or, if there are any quality problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.
- 4/ Not applicable to CDR26, CDR27, CDR28, CDR29, and CDR30.

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4.8 Methods of inspection.

4.8.1 Mounting for testing. When specified in the test procedures, the chip capacitors shall be mounted on a suitable substrate (e.g., 96 percent alumina or FR4 glass epoxy). The substrate and mounting process shall be such that it will not be the cause of, nor contribute to, failure of any test for which it may be used. The capacitors shall be mounted on the substrate as follows:

- a. A substrate shall be prepared with metallized surface land areas of proper spacing to permit mounting of chips by soldering the terminations of the chips to the substrate land areas. The dimensions of the test card are optional.
- b. Solder paste, type Sn60A, Pb36B, or Sn63A in accordance with ANSI/J-STD-005 and ANSI/J-STD-006, shall be used.
- c. The chip capacitor shall be soldered to the substrate using a solder reflow process. Conductive belt reflow and IR reflow processes are suggested. The temperature range of the peak reflow temperature shall be between 220°C and 260°C. Recommended ramp rates during preheating should not exceed 4°C per second. The substrates and capacitors shall be allowed to cool at room temperature.
- d. The substrate shall be cleaned to remove flux residue, if applicable. Any residue which degrades capacitor electrical performance shall be removed.

4.8.1.1 Test rack. When specified, the substrate shall be mounted on a test rack which shall be so designed as to permit readout for electrical parameters at +25°C and +125°C and to monitor each chip under test for failure. This will insure uniform and uninterrupted voltage and heat stresses.

4.8.2 Visual and mechanical inspection. Capacitors shall be examined to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5, and 3.24 through 3.26, inclusive).

4.8.3 Voltage conditioning (see 3.6). One of the voltage conditioning tests in 4.8.3.1 or 4.8.3.2 shall be performed. The lot traveler shall indicate which test is used. When the optional voltage conditioning test of 4.8.3.2 is used, the traveler shall include the specific accelerated voltage used and the test time.

4.8.3.1 Standard voltage conditioning. A minimum of twice the rated voltage shall be applied to the unit at the maximum rated temperature +4°C, -0°C for 100 hours +25 hours, -4 hours. After completion of the exposure period, the unit shall be stabilized at room temperature and the DWV (see 3.6a), IR, capacitance, and DF shall be measured as specified in 4.8.9, 4.8.6, 4.8.4, and 4.8.5, respectively. 1/

1/ Due to the deaging characteristic of ceramic, capacitance measurement may be delayed (applicable to BR, BX, and BZ characteristics only).

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4.8.3.2 Optional voltage conditioning (capacitors with voltage ratings of 200 volts or less only). The manufacturer, with approval from the qualifying activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning test of 4.8.3.1. All conditions of 4.8.3.1 apply, with the exception of the voltage applied and the test time. The minimum time duration, T(test), shall be calculated as follows:

$$T(\text{test}) = \frac{800}{(E \text{ test}/E \text{ rated})^3}$$

Where: $2 \times E \text{ rated} \leq E \text{ test} \leq 4 \times E \text{ rated}$

T(test) = Minimum test time in hours

E test = Applied voltage

E rated = Rated voltage of the capacitor

4.8.4 Capacitance (see 3.7) (for high frequency styles, see 3.1). Capacitors shall be tested in accordance with method 305 of MIL-STD-202. The following details and exception shall apply:

- a. Test frequency: 1 MHz \pm 50 kHz (for all BP and BG characteristic capacitors $\#$ 1,000 pF, and for all BX characteristic capacitors \leq 100 pF); or 1 kHz \pm 50 Hz for all other capacitors.
- b. Test voltage: 1.0 volt \pm 0.2 volt rms.

Stable capacitance standards may be used, at the option of the manufacturer, to eliminate or reduce capacitance bridge and fixturing error when measuring capacitance of less than 100 pF. The method used for making these measurements shall be included in the manufacturer's program plan in accordance with MIL-STD-790.

4.8.5 DF (see 3.8). DF shall be measured with a bridge or other suitable equipment at the frequency and voltage specified in 4.8.4.

4.8.6 IR (see 3.9). Capacitors shall be tested in accordance with method 302 of MIL-STD-202. The following details shall apply:

Precautionary note: Prior to performing this test, capacitors shall be carefully cleaned to remove any contamination including fingerprints. Care must be taken to maintain cleanliness in test chamber and while making measurements.

- a. Test conditions: Rated voltage as specified (see 3.1) applied through a series resistor sufficient to limit the charging current to a maximum of 50 milliamperes (mA).
- b. Special conditions: If a failure occurs at a relative humidity above 50 percent, the IR may be measured again at any relative humidity less than 50 percent.
- c. Points of measurement: Between the terminations (metallized ends) or leads.

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4.8.7 ESR (UHF) (when specified, see 3.1) (see 3.10). The UHF ESR shall be measured in accordance with appendix A and table XII. Leaded devices shall be characterized as having the same ESR as equivalent nonleaded devices manufactured from the same dielectric/metallization material lot.

TABLE XII. ESR (UHF) test frequency range.

Capacitance range	Frequency range	Wavelength
100 pF or less	910 MHz - 1,050 MHz	7/4
101 pF - 330 pF	640 MHz - 660 MHz	5/4
331 pF - 1,000 pF	380 MHz - 400 MHz	3/4

4.8.8 ESR (RF) (when specified, see 3.1) (see 3.11). The RF ESR shall be measured in accordance with appendix A at one quarter wavelength in a frequency range of 130 MHz to 260 MHz. Leaded devices shall be characterized as having the same ESR as equivalent nonleaded devices manufactured from the same dielectric/metallization material lot.

4.8.9 DWV (see 3.12). Unmounted capacitors shall be tested in accordance with method 301 of MIL-STD-202. The following details and exceptions shall apply:

- a. Magnitude and nature of test voltage: Unless otherwise specified (see 3.1), 250 percent of rated voltage.
- b. Duration of application of test voltage: 5 seconds \pm 1 second.
- c. Points of application of test voltage: Unless otherwise specified (see 3.1), between the capacitor-element terminals.
- d. Limiting value of surge current: Shall not exceed 50 mA.
- e. Examination after test: Capacitors shall be examined for evidence of damage and breakdown.

4.8.10 Solderability (see 3.13). Capacitors shall be tested in accordance with method 208 of MIL-STD-202. The following detail and exceptions shall apply:

- a. For capacitors without leads, each terminal shall be immersed to a depth of .020 inch \pm .010 inch, -.000 inch (0.51 mm \pm 0.25 mm, -0.00 mm), or the entire capacitor may be immersed.
- b. For capacitors with leads, each terminal shall be immersed to a distance of .030 inch \pm .020 inch (0.76 mm \pm 0.51 mm) to the capacitor body.
- c. Examination of terminations shall be in accordance with 3.13. In case of dispute, the percent coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area.

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4.8.11 Voltage-temperature limits (not applicable to high frequency capacitors)(see 3.14). The temperature of each capacitor shall be varied as specified in table XIII. Capacitance measurements shall be made at the frequency specified in 4.8.4. The dc rated voltage need only be applied to the capacitor in each of step E through step G until voltage stability is reached and the capacitance measurement made. Capacitance measurements shall be made at each step specified in table XIII and at a sufficient number of intermediate points between step B and step G to establish a true characteristic curve. Capacitance measurements at each temperature shall be taken at five-minute intervals and shall be stopped and recorded when two successive readings indicate a capacitance change of less than one percent. These measurements need be performed only on capacitors having a value of 10 pF or greater. Capacitors of less than 10 pF shall be characterized as having the same voltage-temperature limits as those of 10 pF or more manufactured from the same dielectric material lot. For voltage ratings above 200 V, an approved alternate test method based on volts/mil stress of the same dielectric lot is allowed.

TABLE XIII. Voltage-temperature limit cycle.

Step ^{1/}	Voltage	Temperature
	<u>Volts, dc</u>	<u>°C</u>
A	None	+25 ± 2
B	None	-55 ± 2
C (reference)	None	+25 ± 2
D	None	Maximum rated temperature +4, -0
E	Rated voltage (see 3.1)	Maximum rated temperature +4, -0
F	Rated voltage (see 3.1)	+25 ± 2
G	Rated voltage (see 3.1)	-55 ± 2

^{1/} Step A through step D and step F (without voltage) only for BP and BG characteristics.

4.8.12 Thermal shock and immersion (see 3.15).

4.8.12.1 Thermal shock. Capacitors shall be tested in accordance with method 107 of MIL-STD-202. The following details shall apply:

- a. Test condition: Test condition A, except that in step 3, sample units shall be tested at the maximum rated temperature (see 1.2.1.2).
- b. Measurements before and after cycling: Not applicable.

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4.8.12.2 Immersion. Following thermal shock, capacitors shall be tested in accordance with method 104 of MIL-STD-202. The following detail and exception shall apply:

- a. Test condition: Test condition B.
- b. Examinations and measurements after final cycle: Capacitors shall meet the requirements of 3.15.

4.8.13 Resistance to soldering heat (see 3.16). Capacitors shall be tested in accordance with method 210 of MIL-STD-202. The following details and exceptions shall apply:

- a. Mounting of specimens: The capacitors shall be mounted on a substrate using the methods of 4.8.1, with the following exception: The post preheat hot-plate temperature shall be $+260^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for a duration of 5 seconds ± 0.5 second. Tunnel ovens shall not be used to provide the soldering heat, since an observation is recommended during the test.
- b. Test condition: B for leaded capacitors and C for unleaded capacitors.
- c. Measurements after test: After completion of the cleaning process and following a minimum 10-minute to maximum 24-hour cooling period, the capacitance, DF, and IR shall be measured as specified in 4.8.4, 4.8.5, and 4.8.6, respectively.
- d. Examination after test: Capacitors shall be examined for evidence of mechanical damage.

4.8.14 Moisture resistance (see 3.17). Capacitors shall be tested in accordance with method 106 of MIL-STD-202. The following details and exceptions shall apply:

- a. Initial measurements: Capacitance as specified in 3.7.
- b. Number of cycles: Twenty continuous cycles except that steps 7a and 7b shall be omitted.
- c. Polarizing voltage shall be 50 V dc during the first ten cycles.
- d. Examinations and final measurements: On completion of step 6 of the final cycle, capacitors shall be conditioned at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and a maximum relative humidity of 60 percent for a period of 18 hours minimum to 24 hours maximum, and shall be visually examined for evidence of mechanical damage and obliteration of marking; capacitance, DWV, and IR shall then be measured as specified in 4.8.4, 4.8.9, and 4.8.6, respectively.

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4.8.15 Humidity, steady state, low voltage (see 3.18). Capacitors shall be tested in accordance with method 103 of MIL-STD-202, condition A. The following details and exceptions shall apply:

NOTE: At no time during test shall voltage greater than 1.55 volts be applied to any capacitor under test.

- a. Initial measurements: Capacitance shall be measured in accordance with 4.8.4.
- b. Tests: Capacitors shall be subjected to an environment of +85°C with 85 percent relative humidity for 240 hours minimum. Cycling shall not be performed. A dc potential of 1.3 volts ± 0.25 volts shall be applied continuously through a 100 kilohm resistor.
- c. Final measurements: On completion of test, remove the capacitors from the chamber and allow 3 hours, 30 minutes, ± 30 minutes for drying and stabilization at 25°C before performing IR (through a 100 kilohm resistor at 1.3 ± 0.25 volts) and capacitance in accordance with 4.8.6 and 4.8.4, respectively. The capacitors shall then be examined for evidence of mechanical damage and obliteration of marking.
- d. Leads may be attached to chip capacitors for mounting and loading purposes. Mechanical loading is acceptable.

4.8.16 Life (at elevated ambient temperature)(see 3.19). Capacitors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

- a. Capacitors shall be mounted as specified in 4.8.1 and 4.8.1.1.
- b. Test temperature and tolerance: At the maximum rated temperature, +125°C +4°C, -0°C.
- c. Operating conditions: Capacitors shall be subjected to a minimum of 200 percent of rated voltage (see 3.1). The surge current shall not exceed 50 mA. When necessary, a suitable current-limiting resistor shall be inserted into the circuit.
- d. Test condition: Test condition F (2,000 hours).
- e. Measurements during and after exposure: After 1,000 hours and at the conclusion of this test and while the capacitors are still held at the maximum rated temperature, IR shall be measured as specified in 4.8.6. The capacitors shall then be returned to the inspection conditions specified in 4.3 and shall be visually examined for evidence of mechanical damage; capacitance, DF, and IR shall be measured as specified in 4.8.4, 4.8.5, and 4.8.6, respectively.
- f. Final measurement: Capacitors shall meet the requirements of 3.19.

4.8.17 Fungus, when applicable (see 3.20). Capacitors shall be tested in accordance with method 508 of MIL-STD-810.

4.8.18 Series resonance (when specified, see 3.1)(see 3.21). Capacitors shall be mounted as specified in 4.8.1 and tested to determine minimum series resonance frequency. Measurement frequency shall be varied smoothly between 100 MHz and 10,000 MHz.

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4.8.19 Terminal strength (when specified, see 3.1) (see 3.22). Capacitors shall be tested in accordance with method 211 of MIL-STD-202. The following details and exceptions shall apply:

- a. Test condition: B (five bends).
- b. Examination after test: Visual examination for loosening, rupturing, and permanent damage to the terminals.

4.8.20 Temperature coefficient and capacitance drift (high frequency capacitors only)(see 3.23).

4.8.20.1 Temperature coefficient. Capacitance measurements shall be made as specified in 4.8.4 and at the temperatures specified in table XIII.

4.8.20.2 Capacitance drift. Capacitance drift shall be computed by dividing the greatest single difference between any two of the three capacitance values recorded at 25°C by the value determined at the reference temperature (see table XIII).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Ceramic chip capacitors are intended to be used in thin and thick film hybrid circuits where micro-circuitry is indicated for filter by-pass coupling applications, and where variation in capacitance with respect to temperature (-55°C to +125°C), voltage, frequency, and life can be tolerated. This specification also covers another ER capacitor, using ceramic dielectric, primarily intended for use in resonant circuits with high Q factor and stability of capacitance with respect to temperature (-55°C to +125°C), frequency, and life.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, and date of this specification, the applicable specification sheet, and the complete PIN (see 1.2.1 and 3.1).
- b. Issue of DoDISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).
- c. Capacitor marking (see 3.24).
- d. Packaging requirements.

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6.11 Tin plated finishes (100 percent). MIL-PRF-55681 capacitors have not historically had a problem with tin whisker growth. However, tin whisker growth could adversely effect the operation of electronic equipment systems. For additional information, see ASTM B545, "Standard Specification for Electrodeposited Coating of Tin".

6.12 Marking of comparable MIL-C-11272, non-ER parts. An ER part manufactured in accordance with this specification and MIL-PRF-55681/4 may be marked and furnished as the non-ER version in accordance with MIL-C-11272/16 and MIL-C-11272/17, and correspondingly, parts manufactured in accordance with this specification and MIL-PRF-55681/5 may be marked and furnished as the non-ER version in accordance with MIL-C-11272/18, if produced on the same assembly line or lines, and provided it is subjected to and meets all the inspection requirements of the ER part.

6.13 Subject term (key word) listing.

- Established Reliability (ER)
- Part per million (ppm)
- Statistical process control (SPC)

6.14 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX A

EQUIVALENT SERIES RESISTANCE MEASUREMENT CRITERIA
FOR HIGH FREQUENCY CAPACITOR STYLES CDR11 THROUGH CDR14
AND CDR21 THROUGH CDR25

A.1 SCOPE

A.1.1 Scope. This appendix specifies the method to determine high frequency loss as measured by equivalent series resistance (ESR). This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS

A.2.1 Other publications. The following document forms a part of the specification to the extent specified herein.

ELECTRONIC INDUSTRIES ASSOCIATION

EIA RS-483 - Standard Method of Test for Effective Series Resistance.

(Application for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

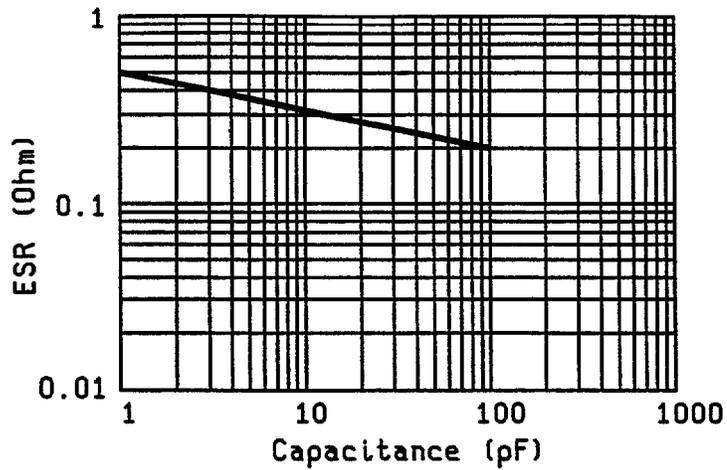
A.3 PROCEDURES FOR TEST

A.3.1 ESR. When specified, the ESR shall be measured in accordance with EIA RS-483.

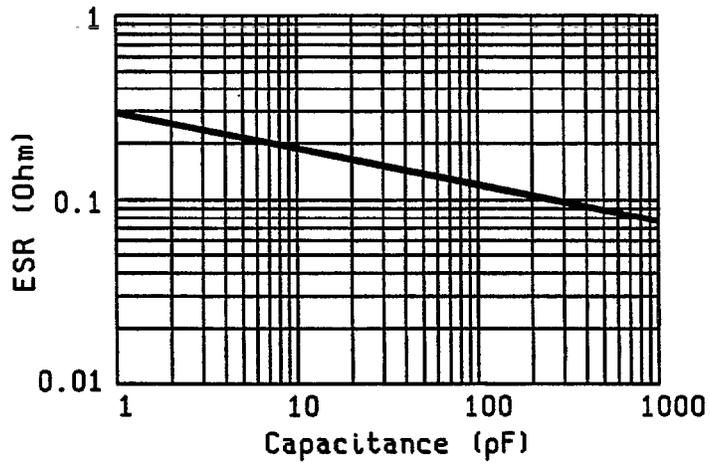
A.4 TEST CRITERIA

A.4.1 ESR. When ESR is tested in accordance with A.3.1, ESR shall be less than the limits shown on figure 3 through figure 6 at the specified measurement frequency range.

APPENDIX A



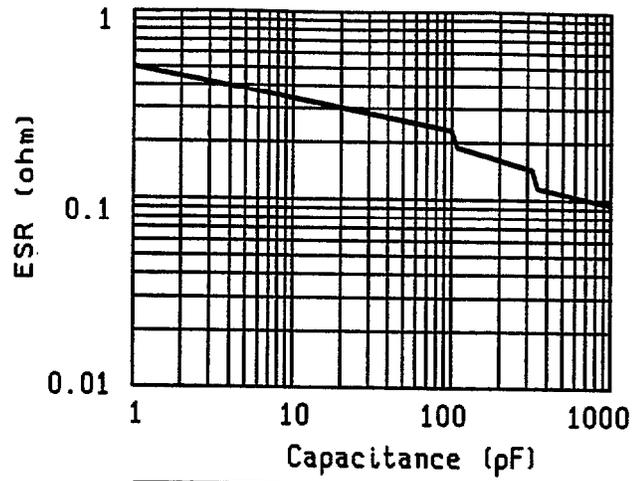
CDR 11/12



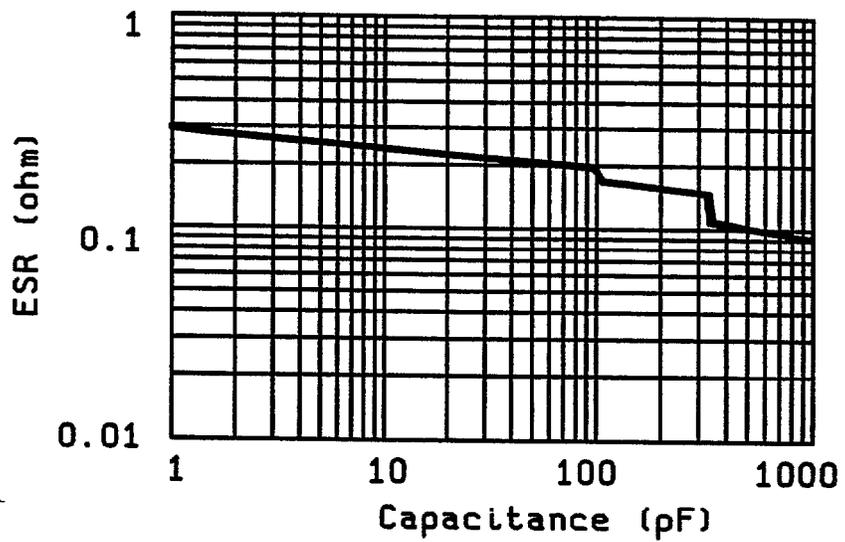
CDR 13/14 AND
CDR21 THROUGH CDR25

FIGURE 3. ESR (UHF) (BG characteristic).

APPENDIX A



CDR 11/12

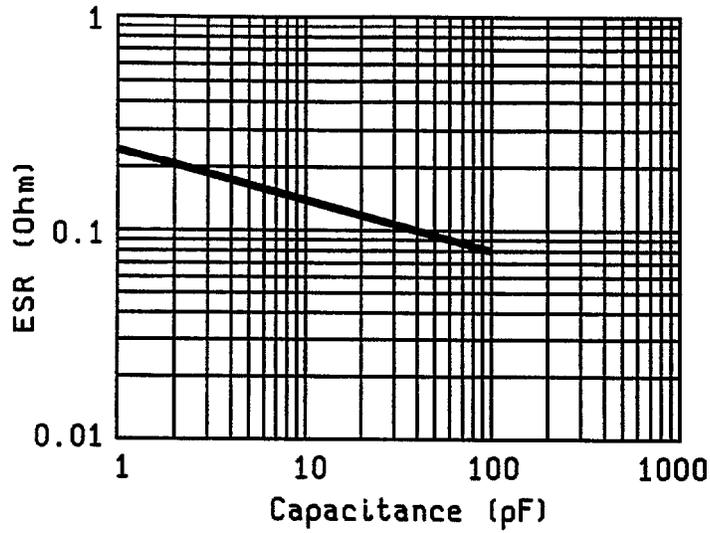


CDR 13/14 AND
CDR21 THROUGH CDR25

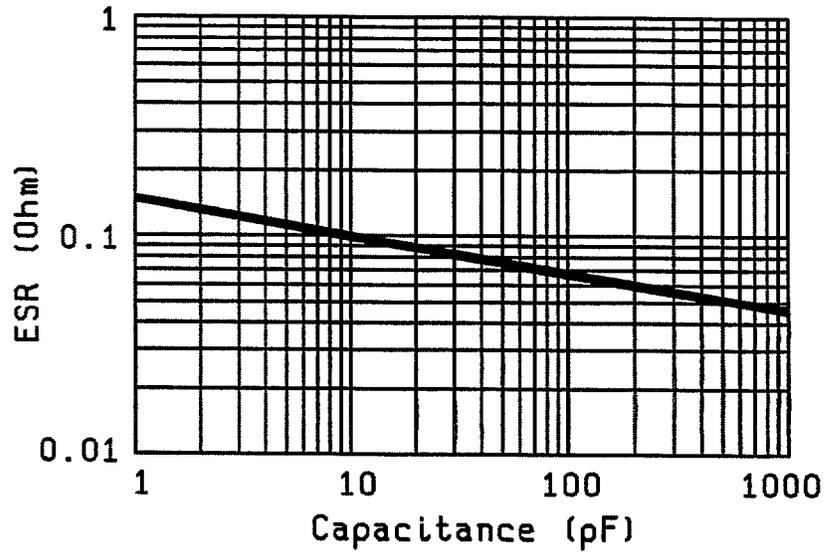
FIGURE 4. ESR (UHF) (BP characteristic).

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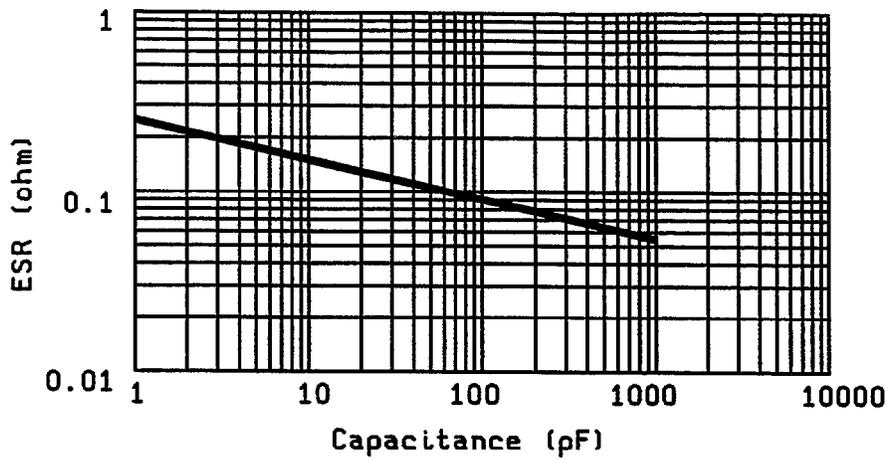
CDR 11/12



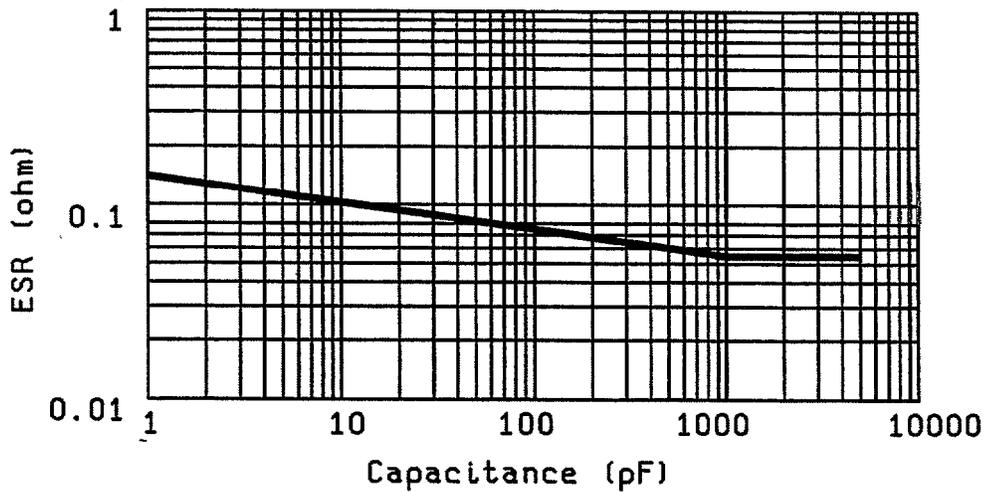
CDR 13/14 AND
CDR21 THROUGH CDR25

FIGURE 5. ESR (RF) (BG characteristic).

APPENDIX A



CDR 11/12



CDR 13/14 AND
CDR21 THROUGH CDR25

FIGURE 6. Equivalent series resistance (RF) (BP characteristic)

APPENDIX B

PROCEDURE FOR QUALIFICATION INSPECTION

B.1 SCOPE

B.1.1 Scope. This appendix details the procedure for submission of samples, with related data, for qualification inspection of capacitors covered by this specification. The procedure for extending qualification of the required sample to other capacitors covered by this specification is also outlined herein. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

B.3 SUBMISSION

B.3.1 Sample.

B.3.1.1 Single-style submission. A sample consisting of 103 sample units of the highest capacitance value in each voltage rating, in each rated temperature and voltage-temperature limits, in each style for which qualification is sought shall be submitted. After qualification has been granted, no changes shall be made in materials, design, or construction without prior notification of the qualifying activity.

B.3.1.2 Combined-voltage submission. A sample consisting of sample units of the highest capacitance value in each voltage rating, in each rated temperature and voltage-temperature limits, in each style for which qualification is sought shall be submitted (see table XIV). After qualification has been granted, no changes shall be made in materials, design, or construction without prior notification of the qualifying activity.

B.3.2 Certification of material. When submitting samples for qualification, the contractor shall submit certification, in duplicate, that the material used in his components are in accordance with the applicable specification requirements.

B.4 EXTENT OF QUALIFICATION

B.4.1 Single-style submission. Capacitance-range qualification will be restricted to values equal to and less than the capacitance value submitted. Capacitance-tolerance qualification will be restricted to tolerances equal to and wider than the tolerance submitted. Voltage rating qualification will be restricted to that submitted. Rated temperature and voltage-temperature limit qualification will be restricted to that submitted.

B.4.2 Combined-voltage submission. Capacitance-range qualification will be restricted to values equal to and less than the capacitance value submitted. Capacitance-tolerance qualification will be restricted to tolerances equal to and wider than the tolerance submitted. Voltage rating qualification will be restricted to those submitted.

B.4.3 Product levels. Qualification of the C (non-ER) level is predicated upon meeting the qualification requirements for ER FRL "P". Since the non-ER (C level) is the ER design without the mandatory conformance inspection and FRL assessment, this product is still expected to meet the environmental requirements (e.g., moisture resistance, thermal shock, shock, etc).

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APPENDIX B

TABLE XIV. Combined-voltage submission.

Style	PIN	Number of units ^{1/}	Rated voltage
CDR01	BP181BJ-M	85	100
	BX332BK-M	<u>2/</u> 43	100
	BX472AK-M	<u>2/</u> 43	50
CDR02	BX271BJ-M	85	100
	BX103BK-M	<u>2/</u> 43	100
	BX223AK-M	<u>2/</u> 43	50
CDR03	BP102BJ-M	85	100
	BX333BK-M	<u>2/</u> 43	100
	BX683AK-M	<u>2/</u> 43	50
CDR04	BP332BJ-M	85	100
	BX563BK-M	<u>2/</u> 43	100
	BX184AK-M	<u>2/</u> 43	50
CDR05	BP562BJ-M	85	100
	BX154BK-M	<u>2/</u> 43	100
	BX334AK-M	<u>2/</u> 43	50
CDR06	BP103BJ-M	85	100
	BX474AK-M	85	50
CDR11 and CDR12	B -101K--M <u>3/</u>	43	150
	BP102A--M	43	50
CDR13 and CDR14	B -101E--M <u>3/</u>	85	500
	B -201D--M <u>3/</u>	<u>2/</u> 43	300
	B -471C--M <u>3/</u>	<u>2/</u> 43	200
	B -621B--M <u>3/</u>	<u>2/</u> 43	100
	B -102A--M <u>3/</u>	<u>2/</u> 43	50
	BP512A--M	<u>2/</u> 43	50
CDR21 and CDR22	B -101E-TM <u>3/</u>	85	500
	B -201D-TM <u>3/</u>	<u>2/</u> 43	300
	B -471C-TM <u>3/</u>	<u>2/</u> 43	200
	B -621B-TM <u>3/</u>	<u>2/</u> 43	100
	B -102A-TM <u>3/</u>	<u>2/</u> 43	50
	BP512A-TM	<u>2/</u> 43	50
CDR23 and CDR24	B -101E--M <u>3/</u>	85	500
	B -201D--M <u>3/</u>	<u>2/</u> 43	300
	B -471C--M <u>3/</u>	<u>2/</u> 43	200
	B -621B--M <u>3/</u>	<u>2/</u> 43	100
	B -102A--M <u>3/</u>	<u>2/</u> 43	50
	BP512A--M	<u>2/</u> 43	50

See footnotes at end of table.

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APPENDIX B

TABLE XIV. Combined-voltage submission - Continued.

Style	PIN	Number of units 1/	Rated voltage
CDR25	B -101E-SM <u>3/</u>	85	500
	B -201D-SM <u>3/</u>	<u>2/</u> 43	300
	B -471C-SM <u>3/</u>	<u>2/</u> 43	200
	B -621B-SM <u>3/</u>	<u>2/</u> 43	100
	B -102A-SM <u>3/</u>	<u>2/</u> 43	50
	BP512A-SM <u>3/</u>	<u>2/</u> 43	50
CDR26	BP151J--M	<u>2/</u> 43	4,000
	BZ821H--M	<u>2/</u> 43	3,000
CDR27	BP331J--M	<u>2/</u> 43	4,000
	BZ182H--M	<u>2/</u> 43	3,000
CDR28	BP681J--M	<u>2/</u> 43	4,000
	BR222J--M	<u>2/</u> 43	4,000
CDR29	BP122J--M	<u>2/</u> 43	4,000
	BR392J--M	<u>2/</u> 43	4,000
CDR30	BP222J--M	<u>2/</u> 43	4,000
	BR123H--M	<u>2/</u> 43	3,000
CDR31	BP471BF-M	<u>4/</u> 40	100
	BP681AF-M	<u>4/</u> 40	50
	BX472BK-M	<u>4/</u> 40	100
	BX183AK-M	<u>4/</u> 40	50
CDR32	BP102BF-M	<u>4/</u> 40	100
	BP222AF-M	<u>4/</u> 40	50
	BX153BK-M	<u>4/</u> 40	100
	BX393AK-M	<u>4/</u> 40	50
CDR33	BP222BF-M	<u>4/</u> 40	100
	BP332AF-M	<u>4/</u> 40	50
	BX273BK-M	<u>4/</u> 40	100
	BX104AK-M	<u>4/</u> 40	50
CDR34	BP472BF-M	<u>4/</u> 40	100
	BP103AF-M	<u>4/</u> 40	50
	BX563BK-M	<u>4/</u> 40	100
	BX184AK-M	<u>4/</u> 40	50
CDR35	BP103BF-M	<u>4/</u> 40	100
	BP223AF-M	<u>4/</u> 40	50
	BX154BK-M	<u>4/</u> 40	100
	BX474AK-M	<u>4/</u> 40	50

1/ Number of samples may vary with style (see table VIII). The number of units shown shall be submitted for each termination finish.

2/ Table VIII, group V samples may be split 12-13 or 13-12.

3/ The PIN will include either a letter P or G (see 1.2.1).

4/ The number 40 is derived from the qualification inspection table: 85 total, minus 6 (for fungus test) divided by 2 and rounded off to 40.

Custodians:

Army - CR
Navy - EC
Air Force - 85

Review activities:

Army - MI
Navy - AS, MC, OS, SH
Air Force - 19, 99
DLA - CC

Preparing activity:
Army - CR

Agent:
DLA - CC

(Project 5910-1923)

AUTHORIZED ER DISTRIBUTORS: Category A unless otherwise specified

MANUFACTURER: GENICOM Corporation
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Electronics Marketing Corp. 60 Compark Centerville, OH 45459-4802	*	Jaco/QC Product 3158 S. 108th Avenue East Suite 274 Tulsa, OK 74146	*
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Jaco/Distel, Inc. 15014 N.E. 40th Street Building O, Unit 202 Redmond, WA 98052	*	Norstan Electronics 1911 E. Carnegie Avenue Santa Ana, CA 92905	
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Jaco Electronics, Inc. 1053 East Street Tewksbury, MA 01876	*		
Jaco Electronics, Inc. Rivers Center 10270 Old Columbia Road Columbia, MD 21046	*		
Jaco Electronics, Inc. Ottilio Office Complex 555 Preakness Avenue Totowa, NJ 07512	*		
Jaco Electronics, Inc. 145 Oser Avenue Hauppauge, NY 11788			
Jaco Electronics, Inc. 1209 Glenville Drive Richardson, TX 75080	*		