# 3-D Simulation of Heavy-Ion Induced Charge Collection in SiGe HBTs

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***Abstract*—This paper presents the first 3-D simulation of heavy-ion induced charge collection in a SiGe HBT, together with microbeam testing data. The charge collected by the terminals is a strong function of the ion striking position. The sensitive area of charge collection for each terminal is identified based on analysis of the device structure and simulation results. For a normal strike between the deep trench edges, most of the electrons and holes are collected by the collector and substrate terminals, respectively. For an ion strike between the shallow trench edges surrounding the emitter, the base collects appreciable amount of charge. Emitter collects negligible amount of charge. Good agreement is achieved between the experimental and simulated data. Problems encountered with mesh generation and charge collection simulation are also discussed.**

***Index Terms*—Deep trench, DESSIS, HBT, LET, mesh, polysilicon emitter, shallow trench, SIMS, SRIM, UHV/CVD.**

## I. Introduction

SiGe heterojunction bipolar transistor (HBT) technology has emerged as a strong contender for high speed digital and mixed-signal applications because of superior transistor performance and integrability with CMOS. For space applications, as fabricated SiGe HBTs were shown robust to ionization and displacement damage [1]. However, recent testing [2], [3], and quasi-3-D simulations [4] have shown that SiGe HBT logic circuits could be vulnerable to single-event effects. To understand SEU in SiGe circuits, it is necessary to investigate the charge collection behavior in the transistors, including the SEU induced transient terminal currents, as well as how the charge collection varies with ion strike position. The latter can only be obtained from true 3-D simulation and microbeam testing. This work presents the first 3-D simulation of heavy-ion induced charge collection in IBM's 5 HP SiGe HBT technology, together with microbeam testing data. The area of maximum charge collection for each terminal is identified based on analysis of the device structure and simulation results.

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## II. Device Structure

The physical layout used for device fabrication, as shown in Fig. 1, is used in constructing the 3-D structure for 3-D simulation. The layout at each fabrication step provides information of lateral doping variation and boundaries between different material regions, e.g., isolation oxide and silicon. Vertical structural information is obtained from SEM images of the same device used in the microbeam testing.

The 3-D SiGe HBT structure is generated using the software package MESH from ISE [5]. The vertical doping and Ge profiles are based on measured secondary ion mass spectrometry (SIMS) data and calibration to measured electrical characteristics. Fig. 2 shows the device in 3-D with doping level indicated by color. The structural information is better seen from the 2-D cross section shown in Fig. 3, which is the result of a 2-D cut of the simulated 3-D structure. The colors on silicon denote the doping concentration. The device has a p-type substrate, an n+ buried layer for minimizing collector resistance, a selectively implanted collector (SIC), an epitaxial SiGe base grown by UHV/CVD, and a polysilicon emitter. Deep trench (DT) isolates the HBT from nearby devices. Shallow trench (ST) isolates the collector and base. Base contact is made through the poly SiGe layer on top of the shallow trench, which is doped heavily through additional implantation to minimize base resistance.

The collector-to-substrate junction area is defined by the spacing between the inner deep trench edges, while the collector-to-base junction area is defined by the spacing between the inner edges of the shallow trench surrounding the emitter opening. The collector-base junction doping profile is nonuniform laterally, because base doping is higher in the extrinsic base than in the intrinsic base, and the collector doping is higher in the intrinsic collector than in the extrinsic collector. As detailed later, the collector-substrate junction area defines the area of maximum charge collection through the collector-substrate junction, while the collector-base junction area defines the area of maximum charge collection through the collector-base junction.

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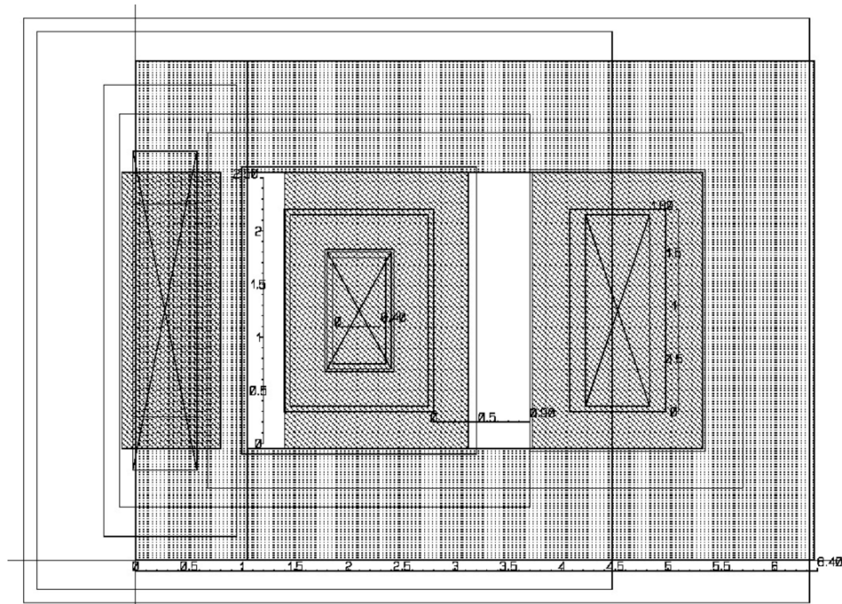

Fig. 1. Layout of the SiGe HBT used in this work. The emitter area $A_E = 0.5 \times 1.0\ \mu\mathrm{m}^2$.

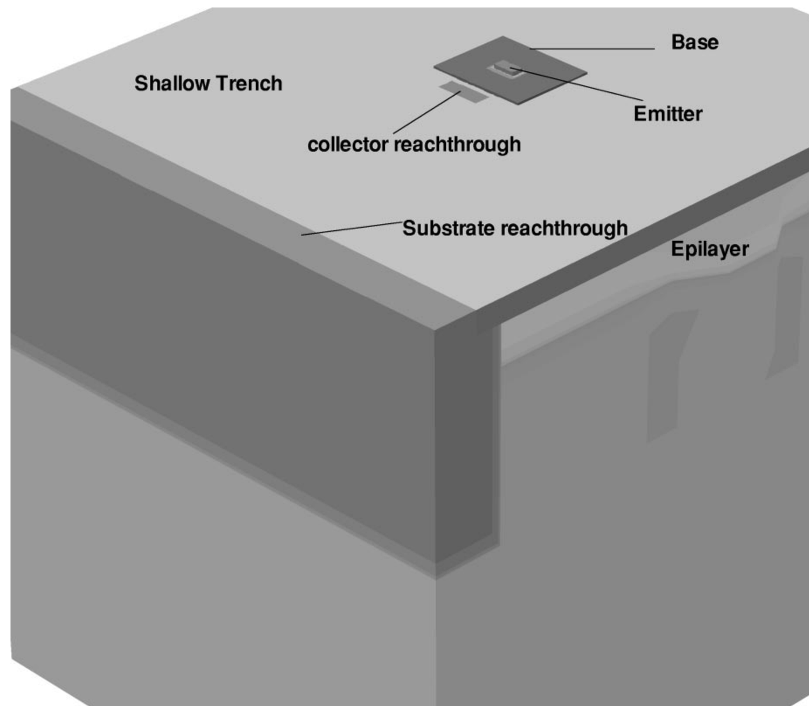


Fig. 2. 3-D view of the device. Color indicates the doping level.

## III. SEU Device Simulation

### A. Meshing and Numerical Issues

For accurate charge collection simulation, a reasonably fine grid near the ion track is critical. A manual placement of fine meshes along the ion track requires considerable efforts, and can be very time consuming. The ideal solution is to refine the mesh based on solution variables, e.g., the carrier generation rate, during device simulation. The 3-D device simulator used, DESSIS [6], however, does not support such self-adaptive meshing based on solution variables. We note that the MESH program supports automatic regridding based on solution variables, which is used here. The average number of nodes is 17 000.

The device electrical characteristics is simulated using DESSIS. In addition to fine gridding along the ion path, the numerical discretization schemes are important in obtaining accurate charge collection simulation. The default discretization method does not give correct charge collection for simple benchmark tests, such as a shallow ion strike through a planar pn junction. Close inspection of the simulation details suggests that this is caused by the *default* assumption of constant generation rate inside the control volume, basic element of 3-D equation solving.

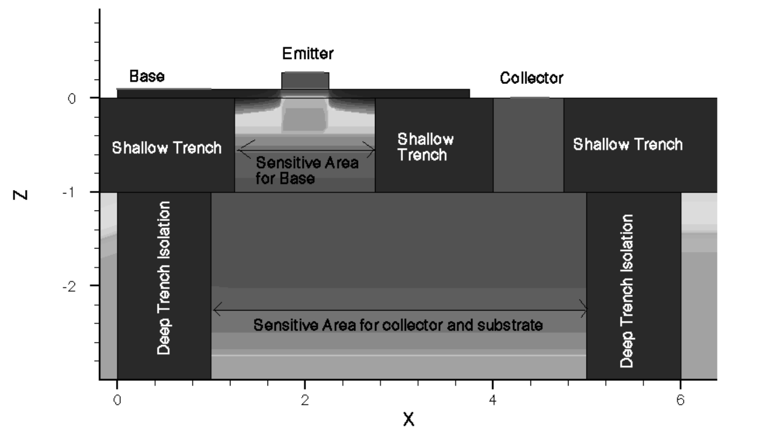


Fig. 3. 2-D cross section of the device. Color indicates the doping level.

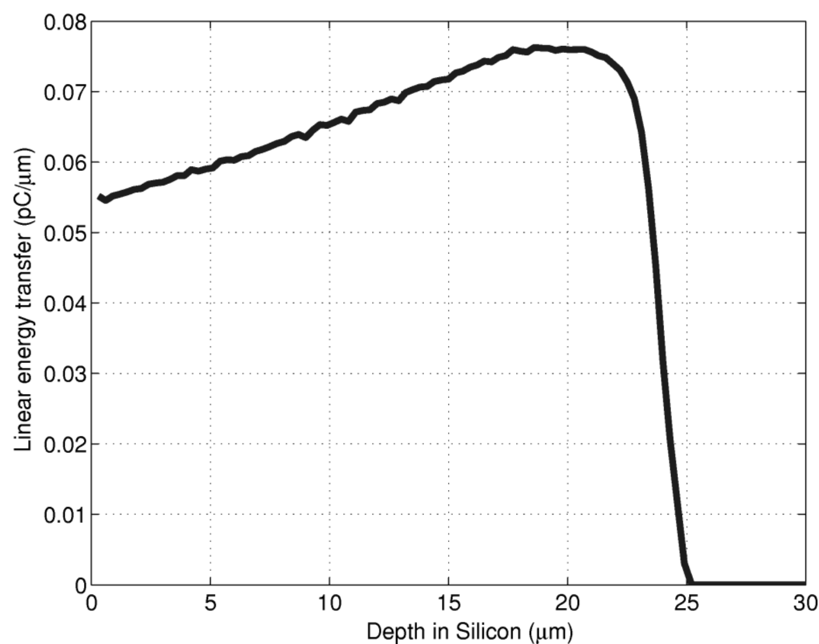


Fig. 4. LET versus depth in silicon for 36 MeV oxygen ion.

This default assumption leads to large error in the final charge collected, because of the well known highly nonuniform spatial distribution of the electron-hole generation rate. This source of numerical error can be minimized by activating an option of more accurate discretization. With this option turned on, the program further divides each 3-D control volume into a set of smaller rectangular boxes for integration of the generation rate in the control volume [6]. To test the accuracy of the discretization parameters, a simple test is made using a shallow ion strike, which should result in complete collection of the charge deposited. All of the charges deposited are collected using the option method, confirming the validity of the discretization parameters. In contrast, only 0.1 pC of the 0.8 pC deposited charge is collected using the default settings.

### *B. Charge Track Generation*

The LET versus depth in silicon was simulated using the stopping and range of ions in matter (SRIM) [7] and input into DESSIS. 36 MeV oxygen ion, which was used in the microbeam experiment, is used here. Fig. 4 shows the LET versus depth in silicon. A matlab code was written to convert the LET unit from the SRIM LET unit $eV/A^o$ to the DESSIS LET unit $\mathrm{pC}/\mu\mathrm{m}$. The average LET is $0.07\ \mathrm{pC}/\mu\mathrm{m}$ which is equivalent to $7\ \mathrm{MeV} - \mathrm{cm}^2/\mathrm{mg}$. The energy losses in the interconnection and passivation layers are accounted for.

In DESSIS, the charge track was generated over a period of 10 ps using a Gaussian waveform. The 1/e characteristic time scale is 2 ps, and the 1/e characteristic radius is $0.1\ \mu\mathrm{m}$. The peak of the Gaussian occurs at 2 ps. These constants are assumed to be independent of LET, and at present the simulator does not support varying these constants with LET.

### *C. Physical Model Selection*

The physical models selected for device simulation include doping dependant SRH recombination, Auger recombination, the phillips unified mobility model, velocity saturation, and bandgap narrowing (BGN). The phillips unified mobility model is used because it is the most accurate for bipolar devices. Due

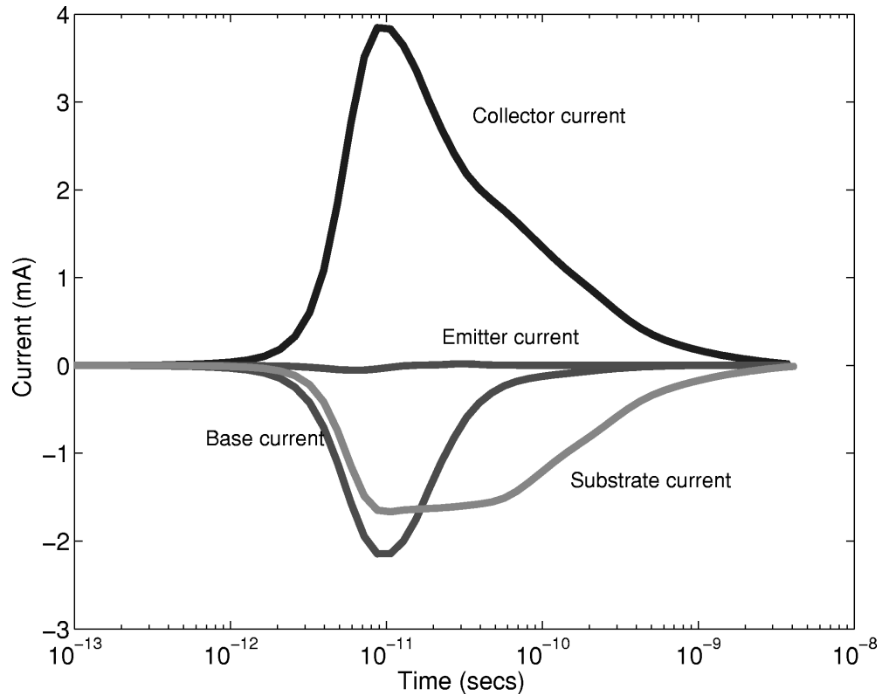


Fig. 5. Simulated terminal currents as a function of time.

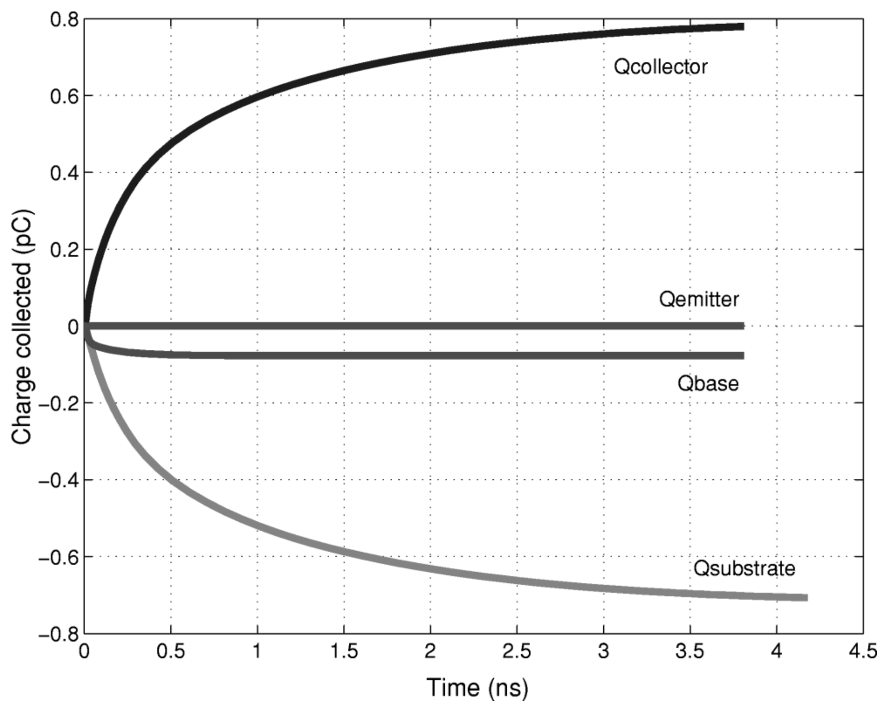


Fig. 6. Charges collected by transistor terminals as a function of time.

to the presence of high density of both carriers Auger and SRH recombinations are both accounted for. Velocity saturation is used because of the presence of high carrier density gradient in SEU simulations.

### *D. Biasing and Transient Simulation*

The emitter, base and the collector were grounded and the substrate was biased to −5.2 V. The heavy ion strike was simulated on different positions on the surface of the device. For each strike, a transient simulation is performed till the current decays to zero. Time step control parameters are carefully chosen to strike a balance between accuracy and simulation time. The use of very small time steps helps reducing simulation error, but increases simulation time. On the other hand, the use of large time steps can lead to large errors, even though it reduces simulation time. One transient simulation takes an average of 4 days on a dedicated Sun Blade 2000 workstation with 1.8 GB memory, provided that convergence problem does not occur.

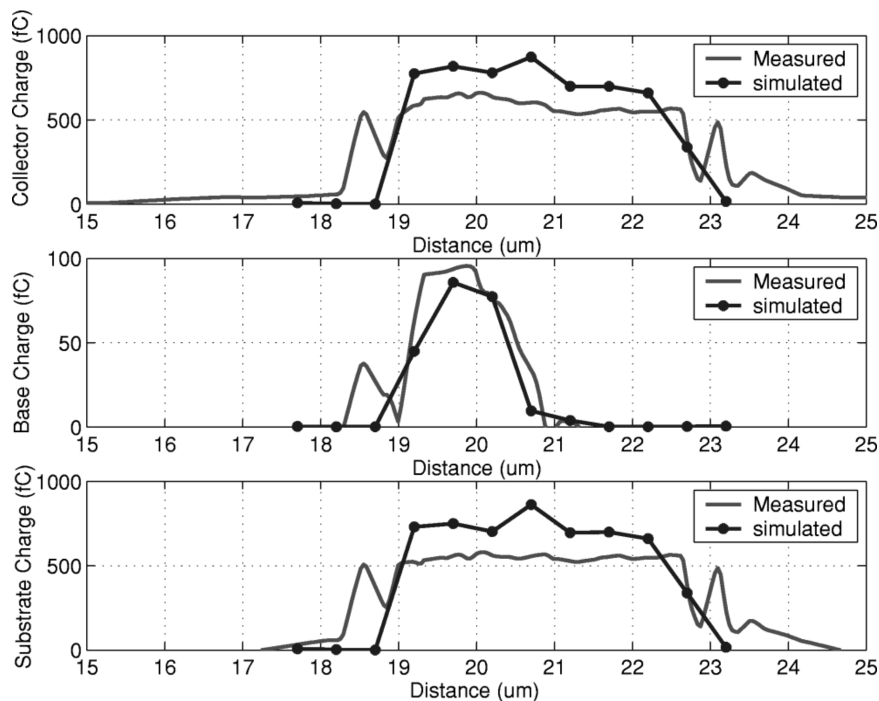


Fig. 7. Charge collected by collector, base and substrate as a function of the x$x$-coordinate of striking location. The $y$-coordinate is fixed at that of the DT center. Both measured and simulated charges are shown.

## IV. Microbeam Test

Charge collection and its sensitivity to ion strike location are experimentally investigated using Sandia Focused Heavy Ion Microprobe Facility's Ion Beam Induced Charge Collection (IBICC) technique. In this test the emitter, base and collector are grounded. Two substrate biases, 0 V and $-5.2$ V, are used. The substrate bias $-5.2$ V is used in HBT digital circuits for this technology. Hence, we focus on the $-5.2$ V substrate bias results. The worst case of charge collection is observed for a substrate bias of $-5.2$ V, as expected, because of a thicker depletion layer of the collector-substrate junction. A focused 36-MeV oxygen ion beam with a spot size of 2 $\mu\mathrm{m}^2$ is scanned over an area of 1600 $\mu\mathrm{m}^2$ containing a wire-bonded SiGe HBT. The emitter area is $0.5 \times 1.0\ \mu\mathrm{m}^2$. The step size is $0.1\ \mu\mathrm{m}$. The final charges collected by all transistor terminals are simultaneously measured for each ion strike. The charges collected by all transistor terminals are obtained as a function of the location of the ion spot, i.e., the $x$ and $y$ coordinates.

## V. Results and Discussion

### A. Transient Current and Charges

Fig. 5 shows the simulated terminal current transients for a strike at the center of the deep trench. Here current entering the device is defined as positive. Fig. 6 gives the corresponding charge collection versus time obtained by integration. The final charge collected is thus obtained, and can then be compared to ion beam testing. Note that the ion beam testing only gives the final charge collected per ion strike, and is not time resolving. Most of the charge collection occurs through the collector-substrate junction. A smaller but noticeable amount of charge is collected by the base. The emitter charge collection is negligible. These are consistent with previous quasi-3-D simulation [4]. The collector collects 0.79 pC of charge, which is equal to the total charge deposited in silicon, indicating that all charges deposited have been collected. This large amount of charge can cause an upset in HBT digital and analog circuits [2].

### B. Ion-Strike Positional Dependance

The ion strike position was stepped from the left outer DT edge to the right outer DT edge along a single line by varying the $x$-coordinate of the incident point. The $y$-coordinate is fixed at the the $y$ of the DT center. As the strike proceeds in the silicon island between the inner DT edges, the simulated collector current waveform and hence the total charge collected is approximately constant, as shown in Fig. 7. The microbeam test data are also shown in Fig. 7 for simulation validation. The simulated collector charge collection agrees reasonably well with the test data. In particular, the simulation well captures the abrupt drop of collector charge collection at the silicon/DT interface. The response of substrate current and charge collection to ion striking position is similar to that for the collector, as expected. The microbeam test agrees well with the simulation for ion strikes inside the silicon island surrounded by the DT but the simulation collects less charge compared to microbeam test for strikes outside DT. In the microbeam test, the collector collects 200 fC for ion strike at the DT outer edge and 100 fC for a strike 1 $\mu\mathrm{m}$ away from the DT outer edge, as shown in Fig. 7. In contrast the collector collects only 40 fC for a strike at the DT outer edge in simulation and 35 fC for a strike 1 $\mu\mathrm{m}$ away from DT edge. A rapid rise and fall of charge collection is seen in the outer edges of the measured curve which the simulation fails to capture. This rapid rise and fall of charge collection is a strong function of the

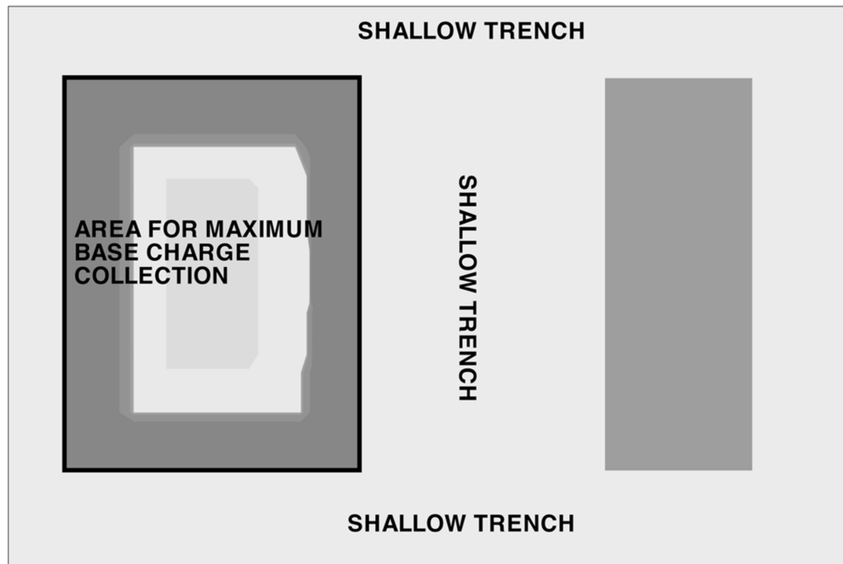


Fig. 8. Top view of the maximum base charge collection area.

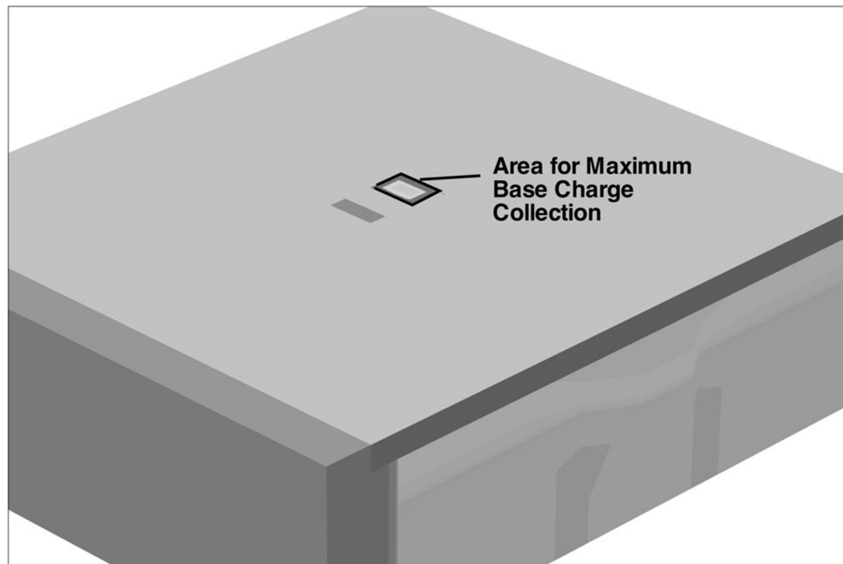


Fig. 9. 3-D view of the maximum base charge collection area.

position of cut, as will be shown later. The origins of these discrepancies are being explored.

### *C. Base Charge Collection*

The peak base current decreases from 1 mA for an ion strike at the DT center to 0.2 $\mu$A for an ion strike at the ST/silicon boundary. The base charge collection shows a similar trend, as can be seen from Fig. 7. The charge collected, however, is not laterally constant. This is in part due to the variation in the junction doping profile between intrinsic and extrinsic collector-base junctions. The base charge collection is higher for ion strikes inside the shallow trench edges surrounding the emitter. This is attributed to the presence of collector-base junctions inside the shallow trench edges, both extrinsic and intrinsic, as shown in Fig. 3.

Based on the above analysis, we identify that the area of maximum charge collection for base is the silicon island surrounded by the ST isolation, as illustrated in Fig. 8 using a top view of the simulated structure. The emitter and the base layers are "turned off" to visualize the silicon islands defined by the ST isolation. The silicon island containing and surrounding the intrinsic emitter is the volume for maximum base charge collection. A 3-D view is given in Fig. 9. Again, the emitter and base layers are "turned off" for clarity.

### *D. Collector/Substrate Charge Collection*

The peak collector current decreases from 3 mA for the ion strike at the DT center to 2.8 $\mu$A for the ion strike at the DT outer edge. The peak substrate current decreases from 2 mA for the ion strike at the DT center to 2.8 $\mu$A for the ion strike at the DT outer edge. The peak current is nearly constant for ion strikes inside the DT edges, and drops abruptly for ion strikes outside the silicon island enclosed by the DT isolation. As a result, the collector and substrate charge collection are maximum and approx-

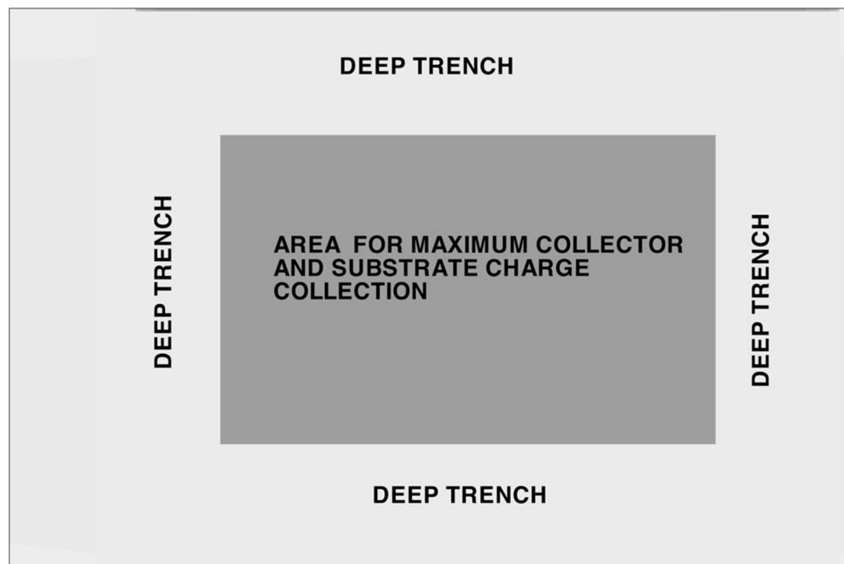


Fig. 10. Top view of the maximum collector and substrate charge collection area.

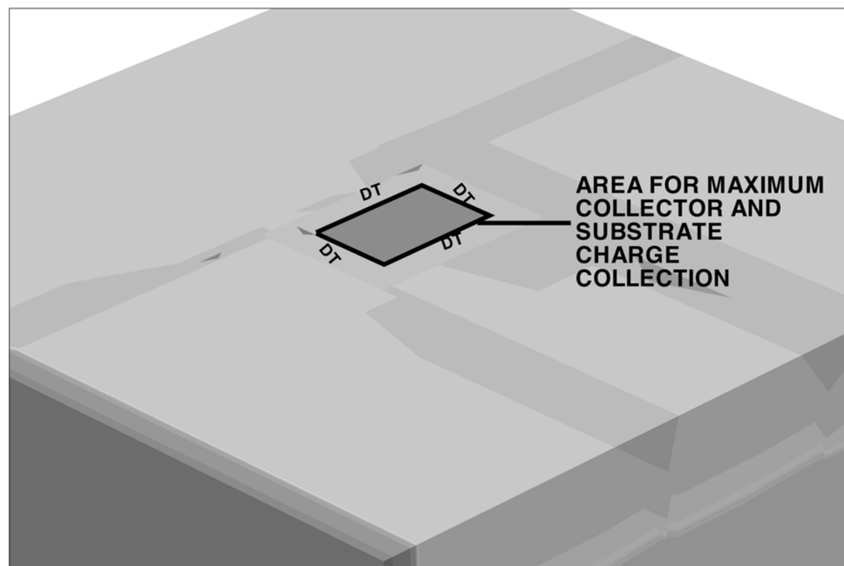


Fig. 11. 3-D view of the maximum collector and substrate charge collection area.

imately constant for strikes inside the silicon island, and drops abruptly for strikes outside the silicon island defined by the DT isolation, as can be seen from Fig. 7. Physically, this ion-strike position dependence of collector and substrate charge collection can be attributed to the presence of collector-substrate junction inside the DT isolation, as can be seen from Fig. 3. The maximum charge collection obtained from simulation differs from the experimental data by 24%. Possible sources of discrepancy include: 1) The LET profile estimated by SRIM; 2) accuracy of physical models used in device simulation, particularly for high carrier concentration as well as high concentration gradients; 3) doping profile and 3-D topology description; and 4) models of charge column generation.

Based on the above simulation results, we identify that the collector and substrate charge collection is maximum for strikes in the silicon island enclosed by the DT isolation, as shown by the top view shown in Fig. 10. Therefore, the sensitive area for collector and substrate charge collection is a rectangle enclosing the silicon island inside the DT isolation. In the microbeam test, 100 fC of charge is collected for a strike 1 $\mu\mathrm{m}$ away from DT outer edge which is sufficient to cause upset in circuits with a small critical charge [8]. The actual size of sensitive volume depends on the lateral diffusion length of carriers, since diffusion is responsible for the collection of charges deposited by outside DT ion strikes, as well as the critical charge. The ST, base, and emitter layers are "turned off" to visualize the silicon island defining the collector-substrate junction. A 3-D view is given in Fig. 11. Again, the emitter, base and the shallow trench layers are "turned off."

### E. Experimental Verification

The sensitive areas for terminal charge collection identified above agree with the charge collection map obtained from the microbeam test, as shown in Fig. 12. Contours of the total charge

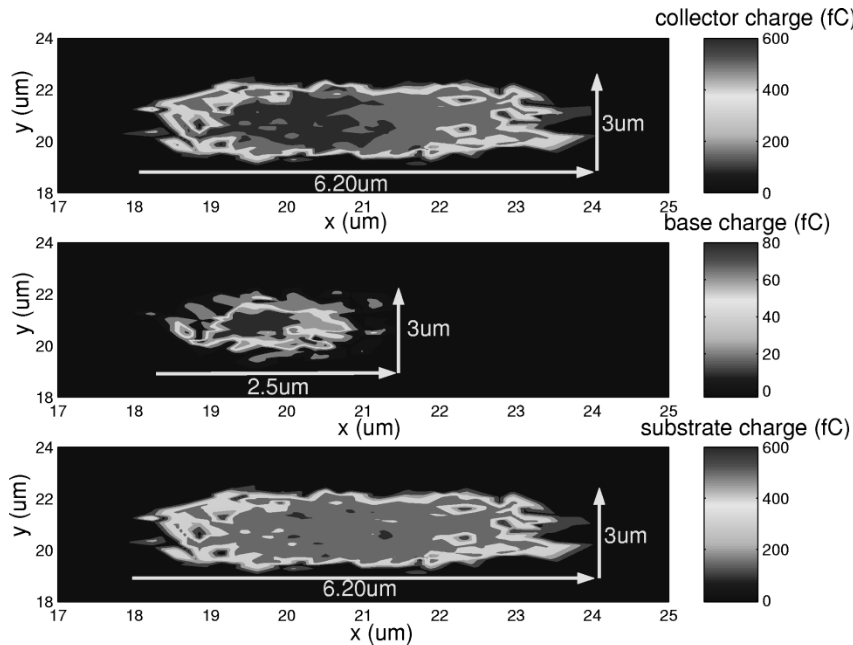


Fig. 12. Contour of the charge collected by the terminals of the experimental device as a function of the ion strike location.

collected by the collector, base and substrate are plotted versus the $x$ and $y$ coordinates of the ion strike. Maximum collector and substrate charge collection occurs over a $6.20 \times 3.0\ \mu\mathrm{m}^2$ area, which approximately corresponds to the area of the silicon island enclosed by the DT isolation. The charge collection is approximately constant for ion strikes within the silicon island. The area of maximum charge collection for base charge collection is clearly smaller than the area of maximum charge collection for collector and substrate charge collection. The base charge collection is maximum over a $2.5 \times 3.0\ \mu\mathrm{m}^2$ area, which approximately corresponds to the area of the silicon island containing the intrinsic device and defined by the ST isolation. As shown in Fig. 12, the outer edges of the area of maximum charge collection are irregular in shape. Hence, as discussed above, the rapid rise and fall of charge collection at the outer edges of Fig. 7 depends on the position of the cut.

## VI. Conclusion

We have presented 3-D simulation of heavy ion induced charge collection in a 0.5 $\mu\mathrm{m}$ SiGe HBT technology. The dependence of charge collection on ion striking position is simulated to identify the sensitive areas for charge collection at all of the transistor terminals. The collector and the substrate terminals collect the maximum charge when the strike is inside the deep trench, primarily through the collector-substrate junction. The base terminal collects the maximum charge when the ion-strike is inside the shallow trench area enclosing the emitter, primarily through the collector-base junction. For ion strikes within the silicon island enclosed by the deep trench, charge collection from 3-D simulation quantitatively agrees with that from microbeam test. For ion strikes outside the DT isolation, the charge collected from simulation is much less than that from microbeam test. Given that the charge collected for outside DT strike is significant to cause upset in sensitive circuits, further investigation is needed to understand the discrepancy between simulation and microbeam test for outside DT strikes.

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