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Jet Propulsion Laboratory
California Institute of Technology
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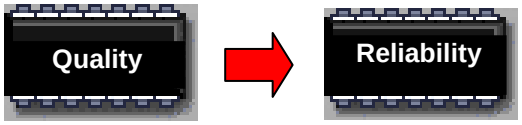
NASA Electronic Parts Program
Commercial Off-the-Shelf Parts Evaluation

Analysis of Plastic Parts Package Delamination

JPL Electronic Parts Engineering Office



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ABSTRACT

Acoustic microimaging (AMI) was successfully used to evaluate commercial off-the shelf plastic encapsulated microcircuits (PEMs). Samples from different commercial vendors were evaluated using C-Mode Scanning Acoustic Microscopy (C-SAM)—one of the AMI methods available for nondestructive detection of delamination. A number of interesting anomalies and potential reliability defects were found, including delamination at die attach, delamination at leads within the mold compound, delamination around the die within the mold compound, delamination on top of the die, and delamination at the backside of the die paddle. These anomalies analyzed by C-SAM imaging were evaluated and analyzed to determine their impact on the reliability of PEMs. CSAM, performed at the beginning of a screening flow, used as a predictor of good or poor electrical performance of evaluated devices, tended to correlate with changes in electrical performance. CSAM inspection and electrical parametric shifts of devices that were subjected to convection reflow were affected less than those equivalent devices exposed to hand soldering and vapor phase reflow; hand solder and vapor phase reflow are commonly used assembly processes within NASA.

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ACKNOWLEDGMENTS

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1. Introduction: Detecting Delamination Using C-SAM

PEMs are constructed of many interfaces which are adhered together in order to manufacture a reliable part: die, die attach, die paddle, and leads/leadframe. These elements form interfaces with the molding compound. The goal of the manufacturer is to offer parts that have strong interfaces. However, it has been found that under certain stress conditions the interfaces could lose adhesion (or delaminate) and thus allow any external contaminates and stresses to affect integrity of the package. It is this loss of integrity that could degrade the reliability of the part. This delamination can be detected with an analytical tool called C-mode scanning acoustic microscopy (C-SAM).

C-SAM analysis is a type of acoustic microimaging (AMI) that uses reflection-mode [pulse-echo] technology in which a single, focused acoustic lens mechanically raster-scans a tiny dot of ultrasound over the sample. As ultrasound is introduced (pulsed) into the sample, a reflection (echo) is generated at each subsequent interface and returned to the sending transducer for processing. Proper lens selection and proprietary high-speed digital signal processing allow information to be gathered from multiple levels within a sample. Images can be generated from specific depths, cross sections, or through the entire sample thickness, and are typically produced in 10 to 30 seconds. See Figure 1-1.

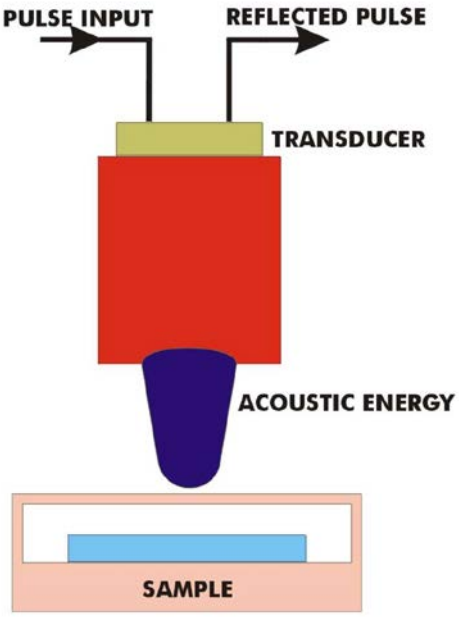


Figure 1-1. Schematic Representation of the C-mode scanning acoustic microscope. This instrument incorporates a reflection, pulse-echo technique that employs a focused transducer lens to generate and receive the ultrasound signals from beneath the surface of the sample.

Applications of C-SAM include nondestructive detection of delamination between lead frame, die face, paddle, heat sink, cracks, and plastic mold compound. The compatibility of a material with C-SAM testing is ultimately limited by ultrasound attenuation caused by scattering, absorption, or internal reflection. C-SAM is often used for process and quality control; it is also used for screening of devices where high reliability is desired for unique requirements such as space applications.

NASA/JPL has employed C-SAM analysis to characterize plastic encapsulated microcircuits (PEMs) from different commercial microcircuit suppliers. This analysis is part of an ongoing program to evaluate commercial off-the-shelf (COTS) parts for their reliability and acceptance for use as space hardware.

References and work by others (Section 7) have shown that plastic parts exhibit a number of anomalies and potential reliability defects, including delamination at die attach, delamination at leads within the mold compound, delamination around the die within the mold compound, delamination on top of the die, and delamination at the backside of the die paddle. However, not all types of delamination are regarded as serious enough to cause reliability risk. Therefore, reject criteria should be established for each package according to acceptable risk, application, and environment use. The delamination types described in this report are very similar to those reported by manufacturers and users evaluating PEMs. This report discusses the reliability concerns with delamination inside plastic packages.

2. Possible Failure Mechanisms from Plastic Encapsulated Microcircuits (PEM) Delamination, Based on Independent Studies

The following PEM failure modes due to delamination are based on independent studies:

- Stress-induced passivation damage over the die surface
- Wire-bond degradation due to shear displacement
- Accelerated metal corrosion
- Die-attach adhesion
- Intermittent electricals at high temperature
- Popcorn cracking
- Die cracking
- Device latch-up

Figure 2-1 shows one of the most common failure modes (popcorning) as a result of delamination, moisture accumulation, and pressure release within a plastic package during the board-assembly process.

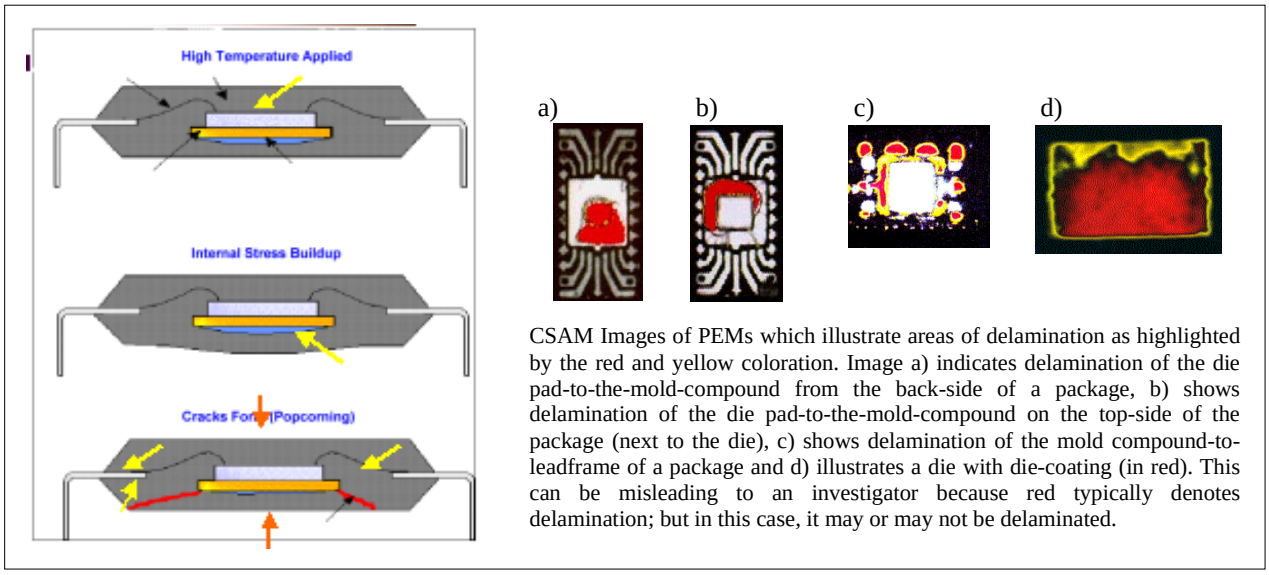


Figure 2-1. Examples of packages with delamination. The yellow arrows show areas where the existence of delamination can accelerate entry/collection of moisture; the red lines show where the cracks (popcorning) typically occur when the board is exposed to high-profile temperature exposures during assembly.

Delamination is dependent on package construction, package size, die size, lead design, number of leads, and environmental stresses, among other influences. A number of references listed at the end of this report address analysis and evaluation of delamination and associated reliability.

3. Industry Delamination Criteria

Strides are being made toward establishing standards for rejecting parts based on their degree of delamination; however, agreement has not yet been achieved. The reason is that it is still difficult to predict package failures based on the amount or type of delamination because package failures often result from delamination *in combination with* other effects. Although most manufacturers understand more of how and why their packages fail, users are still left to exercise their engineering judgment in establishing reject criteria based solely on delamination.

While it is generally agreed that exposing surface-mount plastic parts to high-temperature reflow profiles can generate package failures if delamination is present, the delamination most adverted (rejected) by everyone is on top of the die. Rejection based on delamination in others areas of the package is more subjective.

The key to success is to inspect at the right time(s) during processing and handling of the parts. Some process steps can initiate or change delamination before board assembly and thereby increase the likelihood of catastrophic failure or cause device degradation during board assembly. Figure 3-1 shows the rejection criteria established in the latest revision of JEDEC-J-STD-020D. Since this is an accepted industry-wide standard, it is reasonable to infer that delamination *per se* is not allowed within surface-mount packages. There are also arguments for having minimal or no delamination in other plastic packages as well (references are listed at the end of this document for many failures caused by delamination). High reliability must be predicated on high standards.

6.2.1 Delamination The following delamination changes are measured from pre-moisture soak to post reflow. A delamination change is the change between pre- and post-reflow. The percent (%) delamination change is calculated in relation to the total area being evaluated.

6.2.1.1 Metal Leadframe Packages:

a. No delamination on the active side of the die.
b. No delamination change >10% on any wire bonding surface of the die paddle (downbond area) or the leadframe of LOC (Lead On Chip) devices.
c. No delamination change >10% along any polymeric film bridging any metallic features that is designed to be isolated (verifiable by through transmission acoustic microscopy).
d. No delamination/cracking change >10% through the die attach region in thermally enhanced packages or devices that require electrical contact to the backside of the die.
e. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes: lead fingers, tie bars, heat spreader alignment features, heat slugs, etc.

6.2.1.2 Substrate Based Packages (e.g. BGA, LGA etc.):

a. No delamination on the active side of the die.
b. No delamination change >10% on any wire bonding surface of the laminate.
c. No delamination change >10% along the polymer potting or molding compound/laminate interface for cavity and overmolded packages.
d. No delamination change >10% along the solder mask/laminate resin interface.
e. No delamination change >10% within the laminate.
f. No delamination/cracking change >10% through the die attach region.
g. No delamination/cracking between underfill resin and chip or underfill resin and substrate/solder mask.
h. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, laminate, laminate metallization, PTH, heat slugs, etc.

Figure 3-1. Rejection criteria from JEDEC-J-STD-020D

4. Metrology Software – A Need for Objective Measurement

The C-SAM Metrology Software Tool (CMeST) was developed as part of this task to aid in the analysis of C-SAM images of plastic encapsulated microcircuits and has been extremely useful. In the normal C-SAM image, different colors can indicate areas of different degrees of delamination. Prior to development of this tool, the images were interpreted only by human examiners; hence, interpretations were not entirely consistent or objective. When statistical comparisons were made, no changes could be accurately measured for further processing. In contrast, CMeST processes the color information in image-data files to detect areas of delamination, without incurring inconsistencies associated with subjective judgment. Furthermore, CMeST can be used to create a database of images, i.e., images of packages acquired at given times for comparison with images of the same packages acquired at later times or after subsequent processing. Any area within an image can be selected for analysis, which can include examinations of different delamination types by location. CMeST can also be used to perform statistical analyses of image data. Results of analyses are available in a spreadsheet format for further processing. The results can be exported to any database-processing software.

Advantages of using CMeST are

- Examination of different delamination types by specific locations
- Transformation of imagery to quantifiable data formats
- Statistical processing of collected data
- Comparison analysis for different time domains
- Device failure analysis and/or correlations
- Assessment of vendor's assembly quality and reliability
- Assistance in device qualification and screening methodologies
- Accurate measurements for reject criteria.

The CMeST I/O parameters and operator display are shown in Figure 4-1.

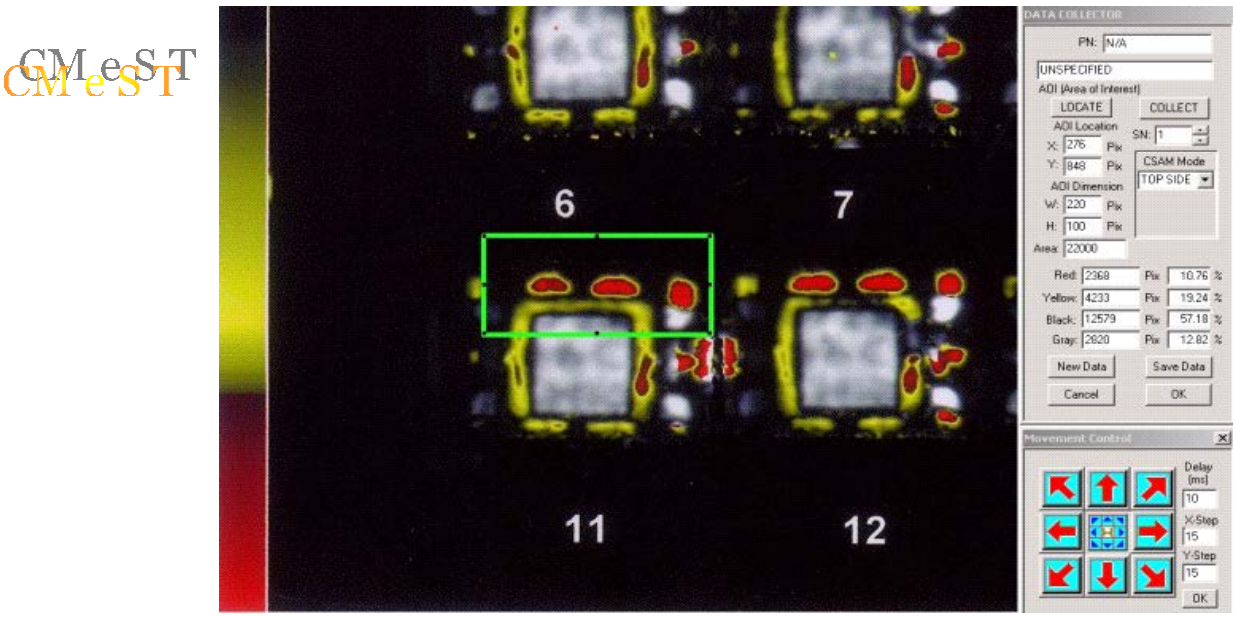


Figure 4-1. CMeST operator's screen

5. Inspection Results of Delamination Measurement Study

5.1 Incoming Inspection

Five different vendors, each with different packages were chosen that would represent typical commercial plastic parts and processes. All parts were procured as COTS and were 100% inspected using C-SAM. The areas inspected were the top of the die, including the lead frame; the backside of the die paddle, including the lead frame. There was also a thru-scan inspection, which looked at the die-attach area. Incoming inspection was performed to evaluate the manufacturers' outgoing quality, package assembly, and package processes uniformity. Table 5-1 summarizes the inspection results

Table 5-1. Overall results of C-SAM inspection of COTS parts
Numerical entries are numbers of parts.

		TOPSIDE									BACKSIDE						THRUSCAN		
		(top of lf)			(top of die)			(space around die)			(die paddle area)			(back of lf)			(die attach area)		
Package	Vendor	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR
24 Ld SOIC	A	250	0	0	250	0	0	0	35	215	109	126	15	237	8	5	11	74	165
28 Ld SOIC	B	251	0	0	247	4	0	11	240	0	244	7	0	251	0	0	237	2	12
8 Ld SOIC	C	226	0	0	220	6	0	225	1	0	225	1	0	226	0	0	223	2	1
8 Ld SOIC	D	203	24	1	NA1	NA1	NA1	34	120	74	224	2	2	153	0	0	NA1	NA1	NA1
8 ld SOIC	E	62	96	70	NA2	NA2	NA2	NA2	NA2	NA2	228	0	0	159	67	2	114	69	45
Totals		992	120	71	717	10	0	270	396	289	1030	136	17	1026	75	7	585	147	223

Each part was viewed at the topside in specific areas, including the top of the lead frame, the top of the die, and the area adjacent to the die or space around the die. Specific areas of each part were then classified as LR, MR, or HR. LR (low risk) was assigned for specific areas having ≤ 10% total area of delamination. MR (medium risk) was assigned for specific areas showing 10 to 50% delamination, and HR (high risk) was assigned for specific areas showing 50 to 100% delamination. From the data, each vendor and/or package type can be evaluated for typical delamination expected at incoming, without further processing. Note that the areas of inspection showing NA2 and NA1 in the table indicate that delamination could not clearly be demonstrated (not applicable). Therefore, no statistics were given.

Table 5-1 shows that Vendor C demonstrates the best assembly process control (less than 10% for all 6 areas) while Vendor A demonstrates the worst process control (greater than 50% for 2 out of 6 areas). Vendors B, D, and E demonstrate marginally acceptable (some room for improvement) process control. What is not known is what process controls (if any) are imposed by any of the vendors or what outgoing monitors are in place to ensure minimum delamination in the delivered product. From a user's point of view, clearly Vendor C products would be the first choice.

This data demonstrates that using products without inspecting them clearly puts the user at a disadvantage if material/assembly quality and reliability requirements are to be met. From this analysis it is not clear if delamination correlates with the number of leads and or package size. The most serious concern from this evaluation is the amount of delamination observed by thru-scan on three vendors' products, indicating inadequate die attach. This raises reliability concerns, especially for any high-power-consumption parts where it is necessary to remove the heat from the plastic package via the die attach and leads in order to ensure high reliability.

In summary, the incoming inspections and evaluations have shown that delamination exists with many vendors' products when they are shipped to the customer.

5.2 Comparison of Different Lots

All vendors except Vendor B were procured with single lot date codes. A discussion of observations made on lot date codes from Vendor B is given below.

5.2.1 Date Code 0206

Lots were procured with multiple date codes, when available, to evaluate variations between production lots. Vendor B parts were procured with three different date codes that were for three consecutive dates. The quantities from each date code were not equal. Therefore, statistical comparisons are not optimal. However, the general makeup and distribution of delamination among the three date codes are very similar. The majority of delamination occurs around the die as seen from the topside C-SAM view. Table 5-2 shows that the majority (96%) of the parts from this date code exhibited delamination around the die.

Table 5-2. Results of C-SAM inspection of Vendor B parts date coded 0206- 28 Lead SOIC

	TOPSIDE									BACKSIDE						THRUSCAN		
	(top of lf)			(top of die)			(space around die)			(die paddle area)			(back of lf)			(die attach area)		
SN	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR
005	1			1				1		1			1			1		
006	1			1			1			1			1			1		
007-012	6			6				6		6			6			6		
013	1			1			1			1			1			1		
014-016	3			3				3		3			3			3		
017	1			1			1			1			1			1		
018-028	11			11				11		11			11			11		
029	1			1				1		1			1			1		
030	1			1			1			1			1			1		
031-032	2			2				2		2			2			2		
033	1			1				1			1		1					1
034-035	2			2				2		2			2			2		
036	1			1				1		1			1					1
037-047	11			11				11		11			11			11		
048	1			1				1		1			1				1	
049-052	4			4				4		4			4			4		
053-057	5			5				5		5			5			5		
058	1			1				1			1		1					1
059-069	11			11				11		11			11			11		
070	1				1			1		1			1					1
071-076	6			6				6		6			6			6		
077-082	6			6				6		6			6			6		
083	1			1				1			1		1					1
084-087	4			4				4		4			4			4		
088	1			1				1			1		1					1
089-100	12			12				12		12			12			12		
101-102	2			2				2		2			2			2		
103	1			1				1		1			1				1	
104-118	15			15				15		15			15			15		
119	1				1			1		1			1					1
120-124	5			5				5		5			5			5		
125-130	6			6				6		6			6			6		
130	1				1			1		1			1					1
131-135	5			5				5		5			5			5		
136	1			1				1			1		1					1
137-139	3			3				3		3			3			3		
140	1			1				1			1		1					1
141	1			1				1		**1**			1			1		
142	1				1			1		1			1					1
143-145	3			3				3		3			3			3		
146	1			1			1				1		1					1
Total	**143**	**0**	**0**	**139**	**4**	**0**	**5**	**138**	**0**	**136**	**7**	**0**	**143**	**0**	**0**	**129**	**2**	**12**

5.2.2 Date Code 0207

There were fewer parts in date code 0207; however, the same distribution of delamination occurs with the majority of parts (86%), which exhibit delamination around the die. Table 5-3 shows the result of the inspection of this batch.

Table 5-3. Results of C-SAM inspection of Vendor B parts date coded 0207- 28 Lead SOIC

	TOPSIDE									BACKSIDE						THRUSCAN		
	(top of lf)			(top of die)			(space around die)			(die paddle area)			(back of lf)			(die attach area)		
SN	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR
298-314	17			17				17		17			17			17		
315	1			1			1			1			1			1		
316-319	4			4				4		4			4			4		
320	1			1			1			1			1			1		
321	1			1				1		1			1			1		
322	1			1			1			1			1			1		
323-330	8			8				8		8			8			8		
331	1			1			1			1			1			1		
332	1			1				1		1			1			1		
333	1			1			1			1			1			1		
Total	**36**	**0**	**0**	**36**	**0**	**0**	**5**	**31**	**0**	**36**	**0**	**0**	**36**	**0**	**0**	**36**	**0**	**0**

5.2.3 Date Code 0208

There were even fewer parts in date code 0208; however, the same distribution of delamination occurs with the majority of parts (98%), which exhibit delamination around the die. Table 5-4 shows the results of the inspection of this batch.

Table 5-4. Results of C-SAM inspection of Vendor B parts date coded 0208- 28 Lead SOIC

	TOPSIDE									BACKSIDE						THRUSCAN		
	(top of lf)			(top of die)			(space around die)			(die paddle area)			(back of lf)			(die attach area)		
SN	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR	LR	MR	HR
200-223	24			24				24		24			24			24		
224-240	17			17				17		17			17			17		
241	1			1			1			1			1			1		
242-247	6			6				6		6			6			6		
248-271	24			24				24		24			24			24		
Total	**72**	**0**	**0**	**72**	**0**	**0**	**1**	**71**	**0**	**72**	**0**	**0**	**72**	**0**	**0**	**72**	**0**	**0**

5.2.4 Lot-by-Lot Data Analysis

Figure 5-1, (a)–(f) graphically represents the testing for each date code. The area around the die exhibits proportionate delamination for each date code. Figure 5-1 f) shows date code 0206 as having delamination problems *in* the die attach also, which is of even greater concern than the delamination *around* the die. Therefore, date code 0206 is suspect for its reliability and would need to be further evaluated.

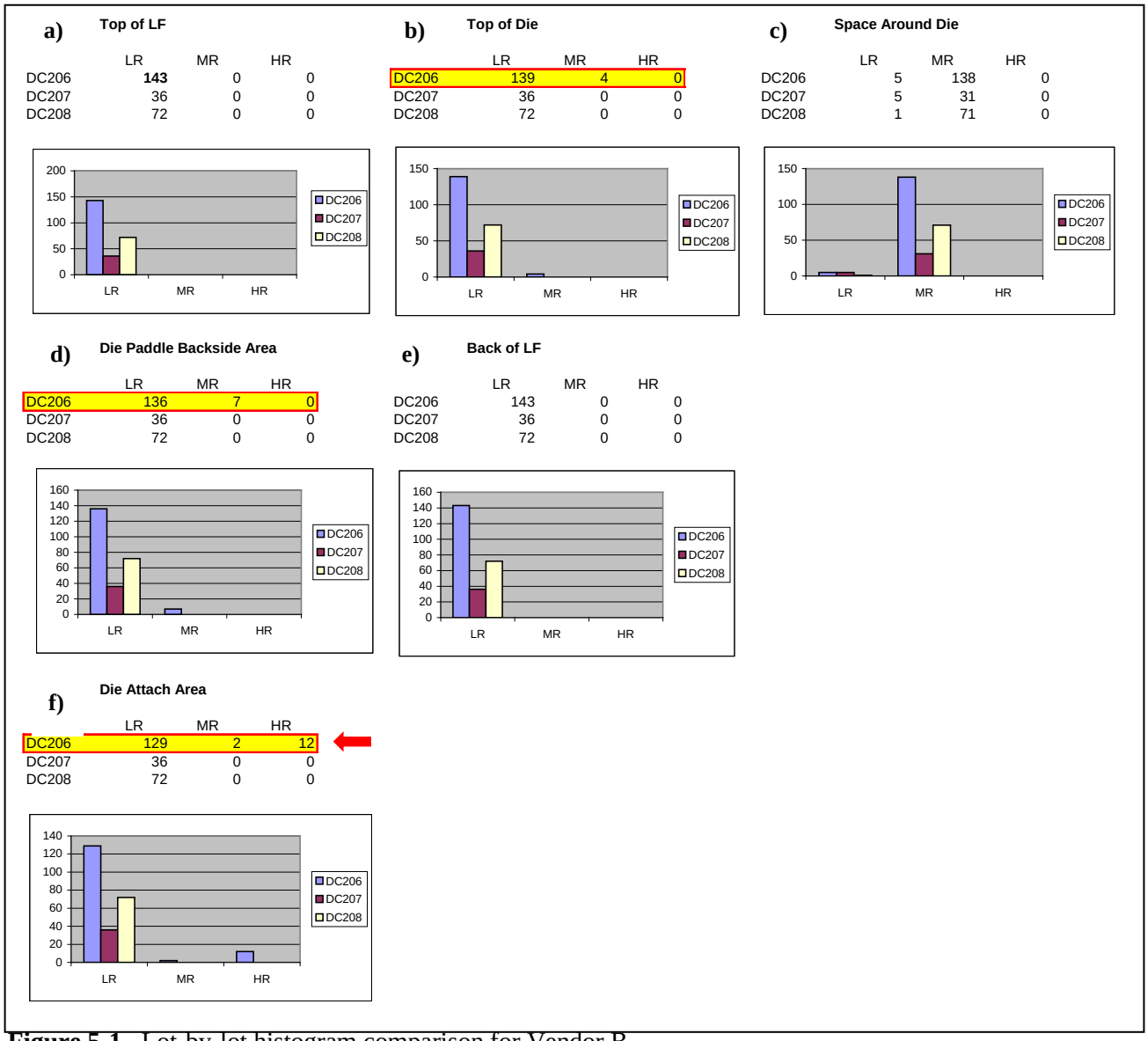


Figure 5-1. Lot-by-lot histogram comparison for Vendor B

The overall results for Vendor B indicate that the assembly process, although not optimal for eliminating all delamination, remains consistent by the distribution within each date code. On the other hand, it should not be inferred from this data that the process is in control since the sample sizes are not equal and the time lapse between date codes is not wide. Ideally, vendors who demonstrate minimum or no delamination in their product would be preferred by those using PEMs for high-reliability space flight applications. It is therefore advantageous to sample more than one date code when attempting to qualify a vendor's product.

5.3 Industry Standards Package Stresses

The parts from Vendors A, B, C, D, and E were stressed to packaging specification IPC/JEDEC J-STD-020B, entitled "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid-State Surface-Mount Devices." All parts were tested in the "as received" condition from each vendor, with no additional screening or testing (with the exception of initial electrical testing to ensure that each part was electrically good prior to the testing). Each part type was stressed to the appropriate classification, based on the manufacturers declared moisture sensitivity level (MSL). Vendors A through D parts were exposed to moisture level 1 (168 hours at 85%RH/85ºC) while parts manufactured by Vendor E were exposed to moisture level 3 (192 hours 65%RH/30 ºC) prior to reflow. Below are the steps used during the MSL conditioning. Figure 5-1 shows the initial topside C-SAM results for Vendor A. Figure 5-2 shows the initial results for the Vendor A backside view.

1a. **Serialization**, not part of the JEDEC test flow, added for the investigation.
1b. **Initial Electrical Test,** Test appropriate electrical parameters, e.g., data sheet values. Replace any devices that fail to meet this requirement.
2. **Initial Inspection,** 40X visual (required).
2a. **CSAM** (C-Mode Scanning Acoustic Microscopy), added for documentation of the part initial condition.
3. **Bake,** 24 hours minimum at 125 +5/-0°C.
4. **Moisture Soak**, Level 1: 85ºC/85%RH for 168 hours +5/-0, Level 3: 30ºC/60%RH for 192 hours +5/-0.
5. **Reflow,** Not sooner than 15 minutes and not longer than 4 hours after removal from the temperature/humidity chamber, subject the sample to 3 cycles of the appropriate reflow conditions.
6. **Final External Visual,** 40X visual to examine for cracks.
7. **Final Electrical Test,** Test appropriate electrical parameters, e.g., data sheet values.
8. **Final Acoustic Microscopy,** Perform scanning acoustic microscope analysis on all devices.

It is necessary to validate MSL in order to ensure that parts can be properly packaged, stored, and handled by flight projects during board assembly, solder reflow, or repair operations. The purpose of this portion of the evaluation was to verify that the plastic encapsulated packaging of the sample parts provides a moisture barrier to the industry standard level that each manufacturer claimed. Second, each part was monitored for any delamination changes or initiation that could compromise the package/device reliability.

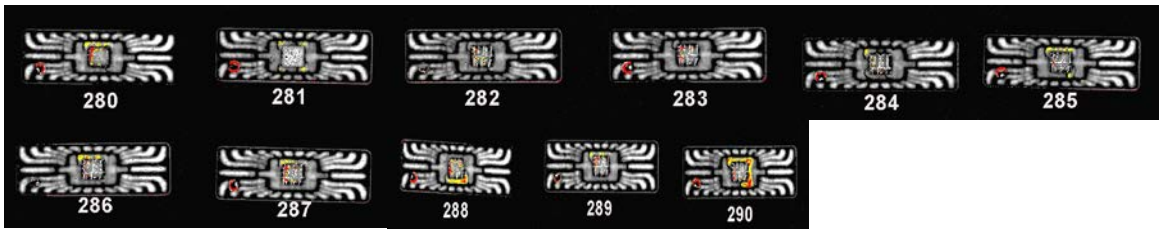


Figure 5-1. Vendor A initial C-SAM results for topside view

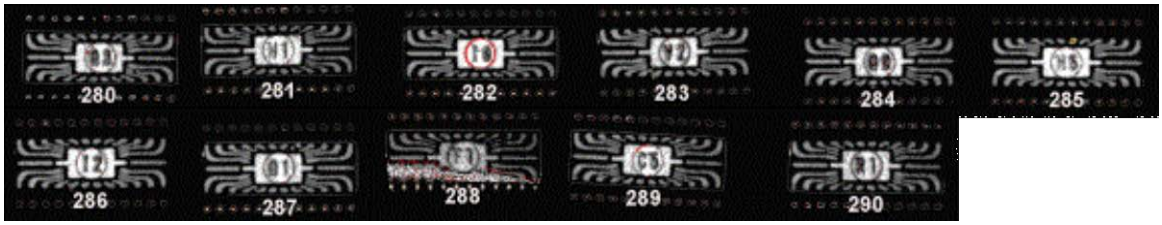


Figure 5-2. Vendor A initial C-SAM results for backside view

C-SAM inspection (as shown in Figure 5-1 and 5-2) shows very little initial delamination, but some delamination is evident around the die (SN 280, 285, 286, 287, 288, 290). These parts are shown in the as-received condition, and are representative of a typical part in the as-received condition; i.e. very little delamination present on top-side and bottom-side. Figures 5-3 and 5-4 show the C-SAM inspection of parts

manufactured by Vendor A following moisture exposure and reflow for the top and bottom, respectively. As can be seen (by the amount of red) there has been a large amount of delamination on the top-side of the part, primarily around the lead-frame area. Notice (from Figure 5-3) that the top of the die appears to remain intact with the mold compound thus 'protecting' the die surface. Two parts show significant delamination on the backside of the lead frame die paddle (Figure 5-4). Final visual inspection of the plastic package did not indicate popcorning.

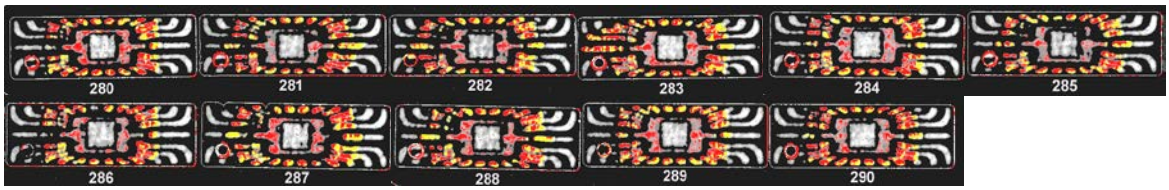


Figure 5-3. Vendor A final C-SAM results after processing for topside view

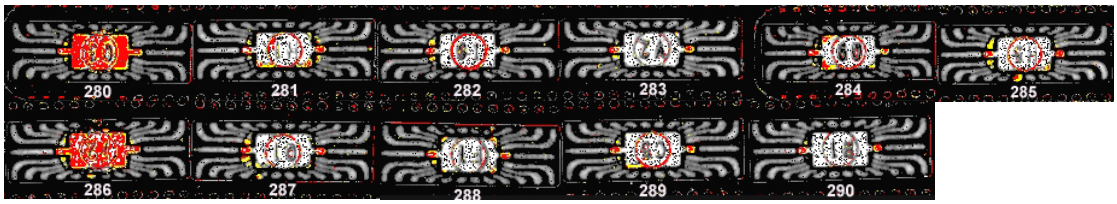


Figure 5-4. Vendor A final C-SAM results after processing for backside view

In these examples, there is more concern with the delamination on the top of the lead frame since this shows a clear path to the die from outside the package. This can lead to migration of contamination up the leads and could possibly cause failure at the die (from corrosion). The concern with the delamination on the back of the die paddle is the possibility of package cracking during reflows. The parts from Vendors B, C, D, and E showed similar delamination changes, but most parts were to a much lesser degree. Parts that meet MSL moisture level 1 are considered the ideal part for assemblers to solder onto a PCB as there are no special storage conditions required prior to board attachment. Therefore, manufacturers are aggressively attempting to meet MSL level 1. There are some manufacturers who do not meet or barely meet MSL level 1 but aggressively market their product as level 1 rather than conservatively market the product as level 2. For example, vendor C conservatively markets their product as MSL level 3 and passed all tests.

5.4 Effects of Soldering Method on Industry Standard Stresses

A sample of each part type was exposed to different conditions of conventional package stresses to determine what effect they had on initiating or changing delamination. The flow consisted of the following steps:

1. Form Group A and expose to hand soldering at 335°C, for 10 sec
2. Form Group B and expose to solder reflow, in accordance with JESD22 106B
3. Expose parts to preconditioning
4. Perform end-point electricals at 25°C and perform C-SAM
5. Expose parts temperature cycles, (-40 +0/-10) °C to (60 °C +10/-0) °C to simulate the shipping of the devices from the manufacturers to distributors, etc.
6. Perform end-point electricals at 25°C and perform C-SAM
7. Expose parts to autoclave
8. Perform end-point electricals at 25°C and perform C-SAM
9. Expose parts to temperature cycles, MIL-STD 883 condition C (-65 ºC to + 150 ºC)
10. Perform end-point electricals at 25°C and perform C-SAM.

Figure 5-5 shows an example of how serial 19 from Vendor B responded to package stressing per the above stress sequence. The part evaluated in the figure shows a considerable amount of delamination on top of the die after exposure to the autoclave stress test. However, the same degree of delamination detected following the autoclave test was not detected after exposure to temperature cycling. A possible explanation for this observation could be that the part was left in a (more) compressive mode following temperature cycling. That is, the gap between the mold compound and the top of the die was narrower than it was following the autoclave test and therefore the delamination was not detected by the equipment. It may be possible that CSAM performed following temperature cycling indicates a part with minimal delamination (above the die) while it actually has delaminated at some point during the stressing and the delamination was not detected. Further work is required to fully understand this observation.

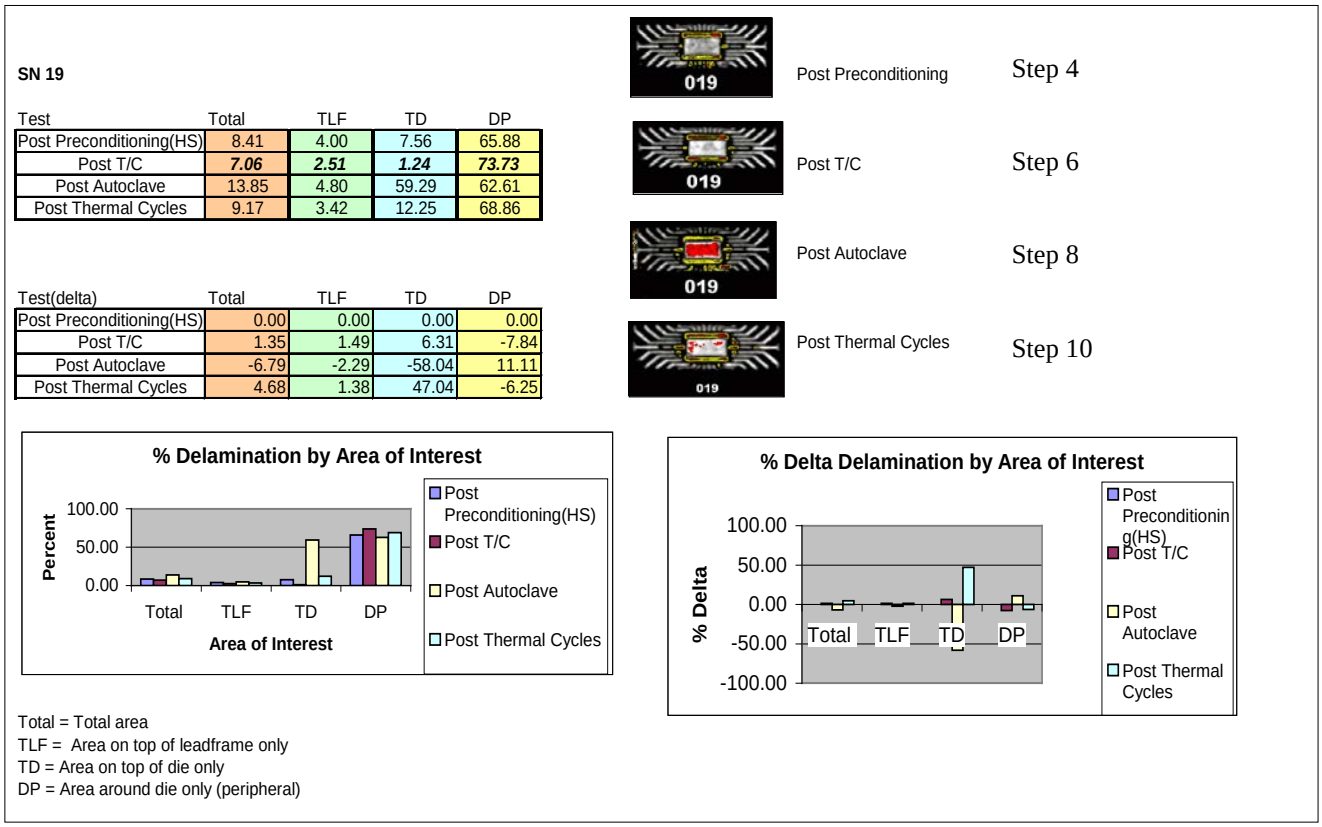


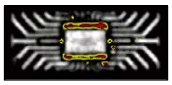
Figure 5-5: Effect of Package Stresses on Serial 19 from Vendor B.

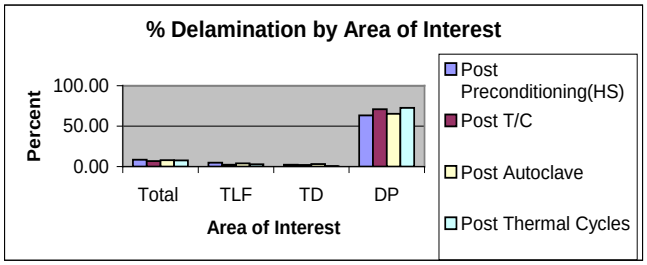
Figure 5-6 shows no significant changes in delamination due to package stress exposure in serial number 8.

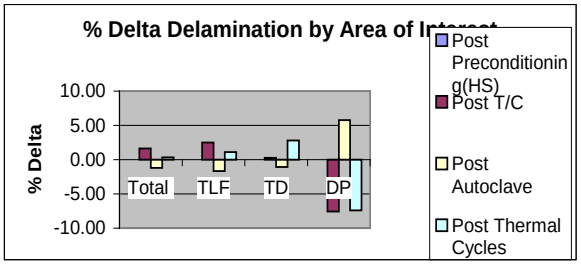
SN 8

Test	Total	TLF	TD	DP
Post Preconditioning(HS)	8.47	4.71	2.28	63.40
Post T/C	6.83	2.20	2.01	70.98
Post Autoclave	8.03	3.88	3.07	65.23
Post Thermal Cycles	7.71	2.78	0.27	72.63

Test(delta)	Total	TLF	TD	DP
Post Preconditioning(HS)	0.00	0.00	0.00	0.00
Post T/C	1.65	2.51	0.26	-7.58
Post Autoclave	-1.20	-1.68	-1.06	5.75
Post Thermal Cycles	0.32	1.10	2.79	-7.40







Total = Total area
TLF = Area on top of leadframe only
TD = Area on top of die only
DP = Area around die only (peripheral)

Figure 5-6: Effect of Package Stresses on Serial 8 from Vendor B.

5.4.1 Delamination versus Soldering Method

In order to determine the effects of different soldering methods and conditions, all parts from Vendors A, B, C, D, and E were conditioned to the generic flows shown below in Figure 5-7 and examined, evaluated, and analyzed for delamination anomalies and or occurrences.

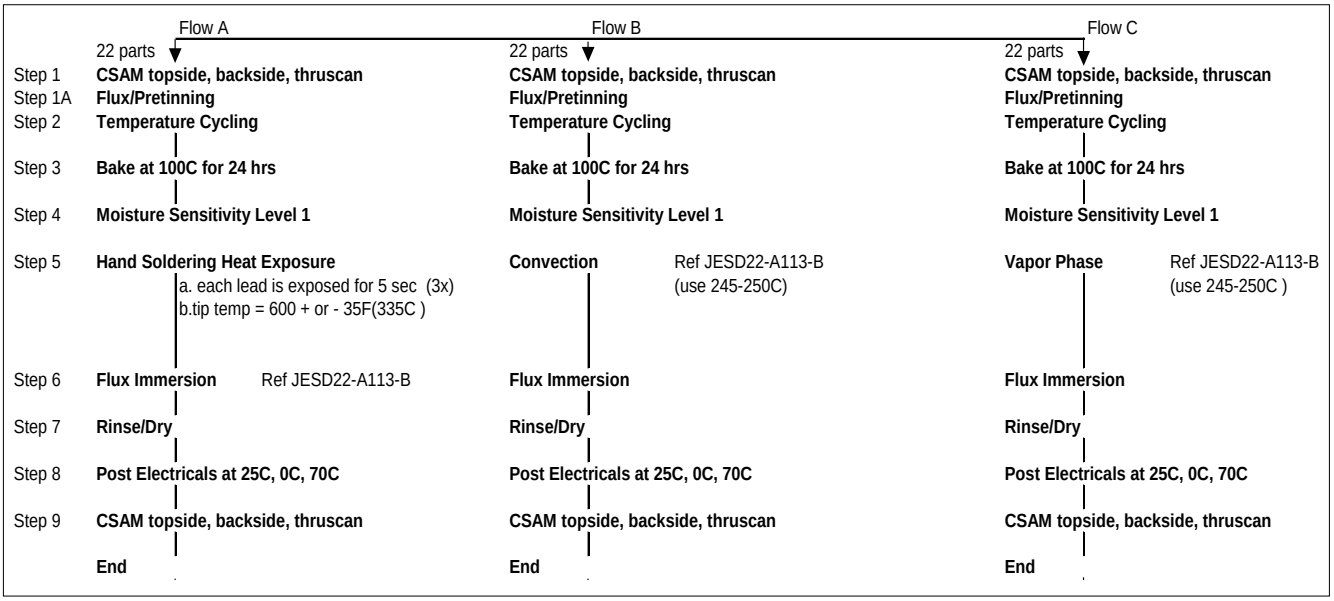


Figure 5-7: Preconditioning Flow for each Soldering Method Evaluated.

5.4.2 Analysis of Delamination Resulting from Soldering

The data in this section was compiled and analyzed using the C-SAM Metrology Tool (CMeST). Using this tool allows the pre- and post-image changes to be numerically quantified and evaluated. Discussed below is a summary of the data on the five part types evaluated.

5.4.2.1 A/D Manufactured by Vendor A

The backside data shows that parts exposed to Flow A (hand solder) did not have significant increase or decrease in package delamination on the back of the lead frame or the backside of the die paddle. In fact, the image samples shown for backside depict the same amount of delamination after hand soldering as before. However, in some cases (e.g., serial no. 077), there is a significant increase in delamination on the backside of the die paddle when parts are exposed to Flow C (Vapor Phase). The backside of the lead frame is also not significantly influenced by Flow C. The topside data shows an increase (up to 19%) in delamination on the top of the lead frame after it has been exposed to Flow A. However, the top of the die shows no delamination. After exposure to Flow C, the top of the lead frame has again shown an increase in delamination (up to 30%). There is no delamination on top of the die. It was also observed for Flow A and Flow C that delamination can decrease ~1 to 5%.

5.4.2.2 MUX Manufactured by Vendor B

The topside data shows that parts exposed to Flow A showed a significant increase (up to 68%) in delamination on the lead frame, especially with the short leads. However, there appears to be no delamination on top of the die as result of Flow A. The data from Flow C also shows a significant increase (up to 84%) in delamination on the lead frame, especially with the short leads. There is also evidence of delamination on top of the die as a result of Flow C. The thru-scan (die-attach area) data shows an increase (up to 22%) in the die-attach area as a result of Flow A. Under Flow C conditions, the delamination is greater (up to 47%) in the die-attach area. The backside data shows no increase in delamination under either Flow A or Flow C conditions. Additional evaluations for $DeltaR_{on}$ (change in channel on-resistance), which was measured under Flow A and Flow C, conditions, show no significant difference in the $DeltaR_{on}$ parametric shifts.

5.4.2.3 OP AMP Manufactured by Vendor C

The topside data shows that parts exposed to Flow A showed little increase in delamination around the die, but parts exposed to Flow C (e.g, serial numbers 61 and 65) show a significant increase in the same area around the die. The increase in delamination from Flow C was as high as 76%. This device also has a die topcoat that appears to be affected (reduced, due possibly to shrinkage caused by change in adhesion) by both Flow A and Flow C. The backside data shows no change for Flow A or Flow C. The thru-scan data (die attach) shows an increase in delamination (~10 to 18%). It appears that Flow A affects more parts for this type of delamination than Flow C. There is possibly some correlation between delamination and some electrical parameters (e.g., input offset voltage, VOS at ±15 V supply), as shown in the VOS Flow C delta distribution tables.

5.4.2.4 Voltage Reference Manufactured by Vendor D

The topside data shows that delamination increases (up to 58%) around the die for Flow A, Flow B, and Flow C. It appears that Flow B has more impact on the increase of delamination. This device has a die topcoat that appears to have more positive and negative distribution for Flow B. The backside data shows no significant differences with any soldering method. The thru-scan data shows no significant differences with any soldering methods; however, it appears that only Flow A shows no increase in die attach delamination. From the electrical data evaluation, it appears that the V_{out} tests at 2.5V and at 3.0V exhibited more change (delta shift) under Flow A conditions than under either Flow B or Flow C conditions.

5.4.2.5 OP AMP Manufactured by Vendor E

The topside data shows that the change in delamination is essentially the same for Flow A and Flow B. Flow C parts appear to have more delamination. Only one device (serial no. 272) experienced a 58% increase in delamination after exposure to Flow C. The delamination is limited to the top of the lead frame, with no delamination on top of the die. Flow A and Flow B have a negative effect on delamination. Review of the electrical data (delta shifts) indicates that Flow C has more of an affect on parameters CMRR AC and GAIN ERR than does either Flow A or Flow B. One may infer some correlation exists between negative part performance and increase of delamination for Flow C. However, this is difficult to validate without detailed analysis.

5.4.2.6 Summary of Soldering Evaluation

Table 5-5 was compiled from the above summaries from each Vendor (paragraphs 5.4.2.1 through 5.4.2.5). Note that in the table there is not a complete data set from Flow B (convection reflow). N/A is denoted under Vendors A, B, and C because only one test house had the capability to perform Flow B. Therefore, Flow B was performed only on parts from Vendors D and E. With the limited data gathered from the two Vendors, it appears that Flow B had less effect on electrical parametric shifts compared to Flow A (hand soldering) and Flow C (vapor phase) which showed some electrical parametric changes. These electrical changes correlated with parts showing topside delamination. Also, Vendor C parts exposed to Flow C showed increases in topside delamination and had electrical parametric shifts. Of all parts exposed to Flow A, the Voltage Reference part (Vendor D) experienced parametric shifts and showed significant topside delamination. Likewise for the parts exposed to Flow C, the OP Amp (Vendor C) and the OP Amp (Vendor E) both experienced significant parametric shifts and also showed topside delamination.

For all parts that showed parametric shifts there was a strong correlation to topside delamination (see Table 5-5). This observation is a one-way relationship; as all parts that showed increases in topside delamination did not necessarily show (or predict) parts that exhibited parametric shifts. But, as mentioned earlier, every time that there was a parametric shift, those parts did exhibit significant delamination on the topside of the package. Flows A and C are commonly used throughout the NASA community.

Table 5-5: Qualitative Summary of the Preconditioning Evaluation

	Flow A					Flow B					Flow C				
CSAM Area of Interest	Vendor A	Vendor B	Vendor C	Vendor D	Vendor E	Vendor A	Vendor B	Vendor C	Vendor D	Vendor E	Vendor A	Vendor B	Vendor C	Vendor D	Vendor E
Top side	**NC**	↑	**NC**	↑	↑	**N/A**	**N/A**	**N/A**	↑	↑	**NC**	↑	↑	↑	↑
Back side	**NC**	**NC**	**NC**	**NC**	**NC**				**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
Top of die	**NC**	**NC**	**NC**	**NC**	**NC**				**NC**	**NC**	**NC**	↑	**NC**	**NC**	**NC**
Lead frame	↑	↑	**NC**	**NC**	**NC**				**NC**	**NC**	↑	↑	**NC**	**NC**	**NC**
Die attach	**NC**	↑	↑	**NC**	**NC**				↑	**NC**	**NC**	↑	↑	↑	**NC**
Electrical shifts	**NC**	**NC**	**NC**	↑	**NC**				**NC**	**NC**	**NC**	**NC**	↑	**NC**	↑

N/A – not applicable, tests were not performed on these parts.
NC – no change in CSAM observation or electrical parameter shift described in the above paragraphs.
↑ *– length of arrow is proportional to the magnitude of CSAM delamination and/or electrical parametric shift.*

5.4.3 Analysis of Delamination Resulting from Life Testing

For this evaluation there were two different part types selected for a study to determine if CSAM could be used as a predictor for electrical performance of a device. Each part type, A-to-D Converter (from Vendor A) and a Multiplexer (from Vendor B), had 250 devices (each) that were electrically tested at the following test points:

- Initial.
- Post Temp. Cycling.
- Post Burn-in.
- Life Test (45 of each type).

It should be noted that the devices were not preconditioned prior to the 3 test points. All devices for this study were electrically tested at the three (above mentioned) test points and then 45 devices were selected from each device type and were subjected to life test for up to 1500 hours of testing. Only the final test point (at 1500 hours) was used as a data point for this study.

Components are then subjected to a small number (10) of temperature cycles to ensure that no package-to-die construction problems precipitate, including wire bonding and die attach. The temperature cycle conditions were in accordance with MIL-STD 883 condition C (-65 ^{o}C to + 150 ^{o}C)

Not all molding compounds used for this study exhibited the same Tg. The molding compounds that exhibit an extremely low Tg at incoming were evaluated for stability during subsequent processing including burn-in or storage. Parts with a low Tg are of concern due to the possibility of the release of flame retardants, namely bromine, which can be corrosive to the aluminum bond pads under certain conditions. Also, the presence of the flame retardant chemicals can contribute to the formation of intermetallics which would affect wire bonding integrity because of Kirkendal voiding.

The purpose of performing burn-in is to eliminate marginal devices from the (screened) remaining lot. Marginal devices represent those parts that may have inherent defects or defects resulting from manufacturing aberrations which are evidenced as time and stress dependent latent failures. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failure under normal use conditions. The burn-in method of screening out defective devices is only as effective as the testing conducted following burn-

in. Such testing must be thorough and include measurement of all device electrical parameters specified in the manufacture's specifications, including parametric degradations.

Table 5-6: Burn-in and Life Test conditions

Part Type	Sample Size	Vendor	Hours	Burn-in Temp
A/D	254	A	440	+85ºC
Multiplexer	250	B	168	+125ºC
Op Amp	253	C	400	+105ºC
Reference	252	D	168	+125ºC
Amplifier	230	E	168	+125ºC

The purpose of operating life is to evaluate the reliability of the packaged die and to generate defects resulting from manufacturing aberrations that are manifested as long-term and stress-dependent failures. The burn-in temperature and time chosen (for burn-in) were predicated on the vendor's glass transition temperature and the calculated junction temperature.

5.4.3.1 Electrical Index

Numerous parameters were measured for both devices. The number of parameters made it difficult to correlate the CSAM initial (predictor) measurement to an electrical parameter measurement without simplifying the data to a single electrical index. The electrical index used in this study was based on number of outlier incidents at all electrical test points. At each test point, if the device had a measured electrical parameter that fell into the top 10 percent or the bottom 10 percent, it was considered an outlier. A device with a higher electrical index is at higher risk of electrical reliability due to the fact that it has drifted electrically from the original electrical measurement to within 10 percent of the top or bottom electrical specification limit.

An example of how the index was utilized is shown in Figure 5-8 as a portion of a spreadsheet. In Figure 5-8, note the 3 measured conditions: initial, post temperature cycle and post burn-in are depicted as headers (in white) in the spreadsheet. The next row shows the temperatures at which the electrical tests were performed. The parameters that exhibited readings that were in the top or bottom 10% are denoted as a dark (purple) color in Figure 5-8. The Electrical Index column simply counts the number of dark boxes (purple) that are in each row. Therefore, the more parameters that exhibit outlier behavior, the higher risk is assigned to that particular serial numbered part.

Initial			Post Temp.Cycling				Post Burn-in						ELECT. INDEX
25	0	70	25	85	-40	-55	25	-40	-55	70	85	0	
S/N	S/N	S/N	S/N	S/N	S/N	S/N	S/N	S/N	S/N	S/N	S/N	S/N	
5	5	5	5	5	5	5	5	5	5	5	5	5	4
6	6	6	6	6	6	6	6	6	6	6	6	6	0
7	7	7	7	7	7	7	7	7	7	7	7	7	2
8	8	8	8	8	8	8	8	8	8	8	8	8	3
9	9	9	9	9	9	9	9	9	9	9	9	9	3
10	10	10	10	10	10	10	10	10	10	10	10	10	0
11	11	11	11	11	11	11	11	11	11	11	11	11	2
12	12	12	12	12	12	12	12	12	12	12	12	12	0
13	13	13	13	13	13	13	13	13	13	13	13	13	2
14	14	14	14	14	14	14	14	14	14	14	14	14	1
15	15	15	15	15	15	15	15	15	15	15	15	15	0
16	16	16	16	16	16	16	16	16	16	16	16	16	0
17	17	17	17	17	17	17	17	17	17	17	17	17	0
18	18	18	18	18	18	18	18	18	18	18	18	18	0
19	19	19	19	19	19	19	19	19	19	19	19	19	0
20	20	20	20	20	20	20	20	20	20	20	20	20	3
21	21	21	21	21	21	21	21	21	21	21	21	21	1

Figure 5-8: Example of a spreadsheet containing electrical data. The darker boxes (purple) denote parameters that exhibited an outlier behavior; meaning that the data has changed to within the top or bottom 10% of the specification limit. The electrical index is a summation of the number of outliers for each part number. The higher the index the higher the risk is assigned for that particular part.

Electrical test data of life test devices were collected at both pre and post test points. The delta shift of the data of each device was calculated on the basis of a percentage change. An example of the delta shift is illustrated in Figure 5-9 as a partial spreadsheet indicating % change between pre and post life test. The serial number (S/N) column has (red) highlighted cells which indicate percentage shifts in electrical performance greater than 10%.

			.	ICC(A+D)@5.25VFC=20MHZ	ICCD@5.25VFC=20MHZ	ICCA@5.25VFC=20MHZ
			MIN			
			MAX	10	10	10
			LO	0.54	0.00	0.27
			HI	2.15	1.68	2.27
			MED	1.34	0.67	1.33
			UNIT	%	%	%
S/N	TEMP	EM#	TIME			
1	25	<26r0>	12:02:29	1.21	0.00	1.33
2	25	<26r0>	12:02:29	1.74	0.00	1.73
3	25	<26r0>	12:02:29	1.88	0.34	1.87
4	25	<26r0>	12:02:29	1.07	0.34	1.20
5	25	<26r0>	12:02:29	0.67	1.01	0.93
9	25	<26r0>	12:02:29	0.94	0.34	1.07
13	25	<26r0>	12:02:29	0.54	0.67	0.80
20	25	<26r0>	12:02:29	1.48	0.34	1.60
25	25	<26r0>	12:02:30	0.67	0.67	1.07
31	25	<26r0>	12:02:30	1.61	0.34	1.60
34	25	<26r0>	12:02:30	0.94	0.67	1.20
35	25	<26r0>	12:02:30	1.74	0.34	2.00
36	25	<26r0>	12:02:30	1.07	0.67	1.20
37	25	<26r0>	12:02:30	1.88	0.67	2.27
41	25	<26r0>	12:02:30	0.94	1.01	1.33
42	25	<26r0>	12:02:30	1.07	0.67	1.33
44	25	<26r0>	12:02:30	1.74	1.01	1.33
45	25	<26r0>	12:02:30	1.21	0.67	1.33
46	25	<26r0>	12:02:30	0.94	1.01	1.47
47	25	<26r0>	12:02:30	1.61	0.00	1.47
49	25	<26r0>	12:02:30	1.74	1.68	1.20
50	25	<26r0>	12:02:30	0.94	0.34	1.07
51	25	<26r0>	12:02:30	1.88	0.00	1.87
54	25	<26r0>	12:02:30	1.34	0.00	1.33
56	25	<26r0>	12:02:30	1.34	0.34	1.47

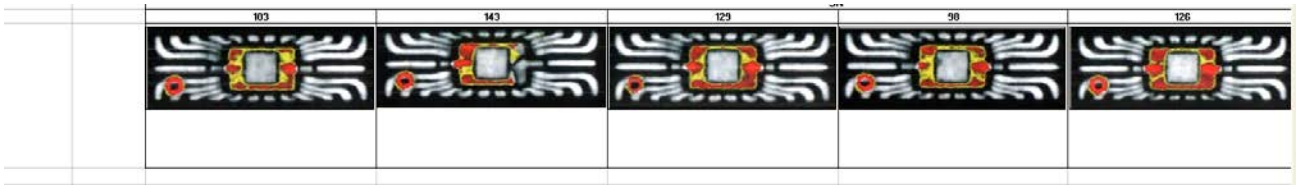
Figure 5-9: Example of a spreadsheet containing delta electrical data for parts pre and post burn-in. The shaded boxes (red) denote parameters that exhibited the highest 10% shift in electrical performance.

5.4.3.2 CSAM Index

CSAM data was treated in a similar manner as the electrical data; a CSAM index was formulated by utilizing the CSAM Metrology tool. Examples of CSAM data are depicted in Figure 5-10 for Top Side, Back Side and Thru Scans. There was significant disbonding illustrated in the top side and bottom side scans. Likewise, the Thru Scan Acoustic data shows significant die attach delamination in most parts.

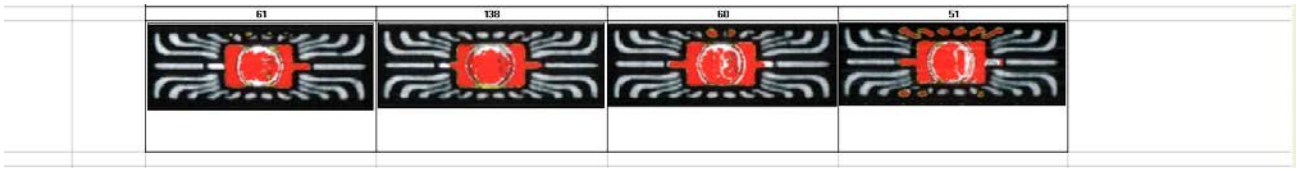
CSAM - Top Side Scan

Disbonds between molding compound and die paddle occur in all parts. However, there is no defect at the die surface and leadframe for all parts.



CSAM - Back Side Scan

Disbonds between molding compound and back paddle occur on most parts.



CSAM - Thru Scan

Die attach delamination occur in most parts.

Figure 5-10: Examples of Acoustic Microscopy data.

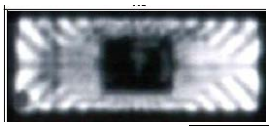
The CSAM Metrology tool was employed for each of the 250 parts from the two vendors and applied to all three scan modes. Each part was evaluated using the number of pixels in color (Red + Yellow) for the Top and Back-side Scans. An example of the Topside scan data is shown in Figure 5-11. The total numbers of red, yellow and red + yellow were compared to the total number of gray pixels in the area of interest to yield a percentage of colored pixels. The parts were then ranked from 1 to 250.

.	RED_PCT	YELLOW_PCT	RED + YELLOW_PCT
MIN	0	0	0
MAX	100	100	100
LO	0	1.98	1.98
HI	23.44	33.03	53.87
MED	0	13.04	13.255
UNIT	%	%	%

S/N	CSAM INDEX			
135	1	0	1.98	1.98
10	2	0	2.22	2.22
41	3	0	2.69	2.69
138	4	0	2.84	2.84
131	5	0	3.12	3.12
90	6	0	3.45	3.45
123	7	0	3.59	3.59
331	8	0	3.73	3.73
87	9	0	4.06	4.06
104	10	0	4.44	4.44
303	11	0	4.49	4.49
64	12	0	4.58	4.58
128	13	0	4.82	4.82
315	14	0	5.34	5.34
322	15	0	5.39	5.39
121	16	0	5.53	5.53
320	17	0	5.53	5.53
23	18	0	5.58	5.58
63	19	0	5.62	5.62
125	20	0	5.67	5.67
333	21	0	5.72	5.72
9	22	0	5.91	5.91
143	23	0	5.91	5.91
321	24	0	5.95	5.95
137	25	0	6.1	6.1
67	26	0	6.14	6.14

Figure 5-11: A sample of the Topside CSAM data by using the CSAM Metrology tool.

An example of the CSAM Metrology Tool utilized on the Thru-scan mode is shown in Figure 5-12. The total number of black pixels was compared to the total number of gray pixels in the area of interest to yield a percentage of black pixels. The parts were then also ranked from 1 to 250.



.	BLACK	BLACK_PCT
MIN	0	0
MAX	1088	100
LO	0	0
HI	1088	100
MED	861.5	79.18
UNIT	PIX	%

S/N	CSAM INDEX		
222	1	0	0
174	2	9	0.83
161	3	35	3.22
125	4	37	3.4
87	5	47	4.32
160	6	50	4.6
189	7	58	5.33
224	8	77	7.08
75	9	93	8.55
179	10	105	9.65
203	11	129	11.86
219	12	155	14.25
144	13	159	14.61
215	14	162	14.89
194	15	163	14.98
167	16	164	15.07
202	17	199	18.29
50	18	239	21.97
30	19	265	24.36
56	20	271	24.91
143	21	273	25.09
205	22	330	30.33
252	23	336	30.88
182	24	337	30.97
183	25	338	31.07
32	26	343	31.53
20	27	344	31.62
169	28	350	32.17
166	29	354	32.54

Figure 5-12: A sample of the Thru-scan CSAM data by using the CSAM Metrology tool.

By combining the CSAM results described above for the Top, Back and Thru Scans, an overall CSAM index was created. Devices with the highest CSAM index were considered to be at higher risk of disbonding and/or delamination. An example of the combined CSAM index is illustrated in Figure 5-13. The top portion of the Figure shows part ID numbers that are shaded in a blue color; this illustrates the best 10% of the CSAM index or virtually no delamination/disbonding. Also shown at the bottom of Figure 5-13 is an area of red shaded part numbers indicating the bottom 10% or a high level of delamination/disbonding.

5.4.3.3 Correlation between Electrical and CSAM Indices

To correlate the CSAM data (taken at the incoming stage of receiving parts) to the electrical performance data taken throughout the life of the parts (as simulated by life test/burn-in), the CSAM index and the electrical index were compared for the studied parts. Figure 5-14 illustrates a sample of the comparison chart used for the analysis. The first column contains the serial number of the parts under test, the second column contains the electrical index, the third column contains the CSAM index data while the remaining columns contain the detailed CSAM data (top, bottom and thru scans). The data sets were sorted by the electrical index data column from lowest index value to highest value. As can be seen in Figure 5-14, the best electrical performance parts are shown (i.e. electrical index value of 0 and shaded in blue). Also it can be seen that the CSAM data shows a high number of low value CSAM indices as shown by the blue shaded cells.

In order for the CSAM inspection to be a good predictor of electrical performance two conditions should apply: 1) parts with good CSAM inspections (i.e. little to no delamination detected) should be correlated to parts with good electrical performance and 2) parts that show poor CSAM inspections (large amounts of delamination detected) should be correlated to parts with poor electrical performance. From the data analysis performed in this study it has been shown that the devices with a low CSAM index are more likely to have a low electrical index. Figure 5-15 shows results for the MUX and ADC devices. Among the 25 lowest CSAM indexed devices (best 10%), only one device had an electrical index greater than 3. Likewise, for the ADC part type, the best 10% CSAM performance had only four devices with an electrical index greater than 3. These results suggest a strong correlation between good CSAM results and good electrical performance.

	.	RED_PCT	YELLOW_PCT	RED + YELLOW_PCT
	MIN	0	0	0
	MAX	100	100	100
	LO	0	1.98	1.98
	HI	23.44	33.03	53.87
	MED	0	13.04	13.255
	UNIT	%	%	%
S/N	CSAM INDEX			
135	1	0	1.98	1.98
10	2	0	2.22	2.22
41	3	0	2.69	2.69
138	4	0	2.84	2.84
131	5	0	3.12	3.12
90	6	0	3.45	3.45
123	7	0	3.59	3.59
331	8	0	3.73	3.73
87	9	0	4.06	4.06
104	10	0	4.44	4.44
303	11	0	4.49	4.49
64	12	0	4.58	4.58
128	13	0	4.82	4.82
315	14	0	5.34	5.34
322	15	0	5.39	5.39
121	16	0	5.53	5.53
320	17	0	5.53	5.53
23	18	0	5.58	5.58
63	19	0	5.62	5.62
125	20	0	5.67	5.67
333	21	0	5.72	5.72
9	22	0	5.91	5.91
143	23	0	5.91	5.91
321	24	0	5.95	5.95
137	25	0	6.1	6.1
67	26	0	6.14	6.14
6	222	0	23.2	23.2
22	223	0	23.3	23.3
237	224	0	23.35	23.35
21	225	0	23.44	23.44
244	226	0.71	22.78	23.49
142	227	0	23.58	23.58
54	228	0	24.01	24.01
260	229	0	24.57	24.57
61	230	0	25.19	25.19
5	231	0	25.47	25.47
48	232	0.14	25.47	25.61
218	233	0.61	25.24	25.85
49	234	0	25.9	25.9
223	235	0	25.95	25.95
35	236	0	26.47	26.47
259	237	0	26.75	26.75
204	238	0	27.36	27.36
248	239	0	27.5	27.5
219	240	0	29.44	29.44
36	241	2.32	28.21	30.53
255	242	0	31.1	31.1
214	243	0	32.84	32.84
136	244	22.5	12.57	35.07
146	245	23.44	17.58	41.02
88	246	19.09	22.02	41.11
140	247	22.31	19.99	42.3
83	248	19.33	23.82	43.15
33	249	14.74	28.69	43.43
58	250	20.84	33.03	53.87

Figure 5-13: A sample of the CSAM index developed by using the CSAM Metrology tool. The top 10% (low amounts of delamination detected) of the devices are shaded in blue and the bottom 10% (high amounts of delamination detected) of the devices are shaded in red.

S/N	ELECT. INDEX	CSAM INDEX	TOP SCAN	BACK SCAN	THRU SCAN
320	0	25	30	17	27
323	0	35	17	86	1
28	0	39	24	64	29
326	0	42	52	69	6
12	0	44	1	122	9
321	0	46	66	24	47
59	0	46	36	74	28
332	0	49	10	124	12
318	0	50	101	32	16
316	0	51	62	49	43
13	0	58	39	84	50
10	0	62	103	2	80
324	0	63	84	35	69
97	0	65	18	140	36
300	0	68	131	52	21
125	0	72	135	20	62
325	0	72	96	111	10
308	0	74	72	48	101
30	0	76	2	209	17
128	0	80	138	13	90
57	0	81	19	205	18
96	0	82	56	128	61
77	0	85	141	85	30
52	0	88	23	207	33
144	0	89	41	148	79
121	0	91	215	16	42
76	0	94	99	94	89

Figure 5-14: A sample of the comparison of the Electrical and CSAM indices. The dark (shaded) cells indicate low electrical and CSAM indices. Low indices represent good performance for each index.

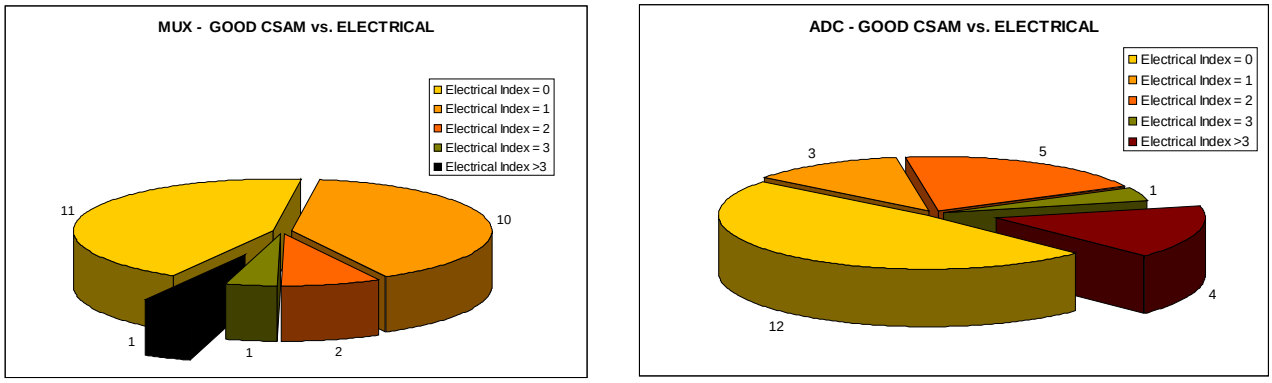


Figure 5-15: Pie chart representation of the breakdown of the electrical index data for the MUX and ADC parts, respectively, for the devices which exhibited good CSAM index values. For both devices, good CSAM observations correlated to good electrical (low index) performance.

For the MUX and ADC devices that had high CSAM indices there was a high likelihood that they had a high electrical performance shift in the life test data. Figure 5-16a shows that among nine MUX high shift percentage devices, seven devise have at least one very high CSAM index. The remaining two parts have a high CSAM index. Figure 5-16b illustrates the ADC devices that had a high shift following life test. Out of thirteen devices that were identified to have a high percentage shift in life test performance, seven devices have at least one very high CSAM index and four have moderately high CSAM index. The CSAM data tends to also be a good predictor of electrical performance for life test. When the devices with the highest electrical shifts were identified, their respective CSAM index was more likely to be high as visually depicted in Figures 5-16a and 5-16b by the large amount of (red) shaded cells.

a)

S/N	Shift_Pct	TOP SCAN	BACK SCAN	THRU SCAN
136	37.18	14	244	239
140	59.36	6	247	242
142	46.82	245	227	249
146	37.55	3	245	241
200	45.45	218	158	141
211	51.27	153	218	144
212	40.00	132	118	187
227	48.45	208	93	84
228	53.36	185	90	113

b)

S/N	Shift Pct	TOP SCAN	BACK SCAN	THRU SCAN
58	10.60	121	219	209
36	10.89	80	57	88
34	11.14	215	55	58
66	11.17	28.00	110	76
42	12.61	146	104	126
129	12.89	206	96	223
25	13.18	224	88	87
86	13.18	46	117	125
41	14.29	103	236	182
62	15.19	153	234	217
90	17.77	133	206	163
54	26.36	65	235	136
20	30.66	158	6	27

Figure 5-16: **a)** Life test data for the MUX device type shown as a percentage change pre and post life test, **b)** life test data for the ADC device type shown as a percentage change pre and post life test. Notice the large amount of (red) shaded cells in the spreadsheet in the CSAM columns.

6. Conclusions and Recommendations

First, it is important to note that this work was completed on five different part types that were assembled in five different package configurations from five different manufacturers. Therefore, the results and conclusions apply only to these five packages and should not be generalized for other package configurations, die constructions, or assembly processes. We do believe, however, that these results should be taken as an indicator of possible issues with other PEMs.

The study, evaluation, and experiments conducted on plastic packages and delamination for the purpose of understanding reliability ramifications continue in industry and academia, as well as among general users of PEMs. Test results do not always agree, and differing interpretations can lead to totally different courses of action. In the same way, the work done under this NASA contract also leaves room for interpretation. Nevertheless, some conclusions and observations can be made that give clearer focus to the subject of PEM delamination and reliability.

6.1 Conclusions

- *Smaller packages are not at high risk for cracking due to popcorning.* From all the test results, it is apparent that PEMs are prone to some delamination caused by the manufacturing process(es). This delamination will more likely increase rather than decrease with subsequent handling and exposure to conditioning (e.g., temperature cycling, preconditioning, HAST, soldering, reflows). Increases in delamination can be quite significant (up to 75%) for some package types. One important observation was that increases in delamination were practically nonexistent on top of the die. Industry claims this is the worst case for delamination because it can cause device failures as a result of popcorning. There was no evidence of any popcorning for the five packages evaluated. This may simply be because the package types evaluated were small in lead count and small in die surface area. Or they may be more robust than the very large packages, which collect more moisture based on critical volume and area.

- *Smaller packages with delamination are not at high risk for corrosion.* A large amount of delamination increase was seen on top of the lead frame before and after different types of conditioning. Failure analysis was completed on some devices exposed to HAST and preconditioning. The devices were then examined with scanning electron microscopy. There was no evidence of any corrosion, which might be expected if moisture had entered along the lead frame-to-compound interface leading to the die.

- *Smaller packages with increasing delamination from soldering are not at high risk for catastrophic functional failures.* Test results showed that different soldering methods could increase package delamination, but this delamination cannot be predicted by package type. It may solely be a function of the manufacturing process used. However, for this evaluation, there was no information from the manufacturers on their process variables. All of the devices tested after exposure to different soldering conditions passed electrical functionality.

- *Some packages with critical delamination may exhibit degraded device performance, which is a high risk until worst-case design/application analysis mitigates the risk.* In some cases, devices exposed to soldering exhibited an increase in delamination and failed to meet electrical performance specifications. It appears from the data for one case that there was a significant increase in delamination along with performance degradation. To determine if there is a direct cause and effect correlation would require further failure analysis and part deprocessing, which was not done.

- *CSAM inspection and electrical parametric shifts of devices that are subjected to convection reflow are affected less than those equivalent devices exposed to hand soldering and vapor phase reflow.* Hand solder and vapor phase reflow are commonly used assembly processes within NASA. Parametric shifts tended to occur in devices that were assembled (simulated) with hand solder and vapor phase methods. CSAM also tended to correlate to the parametric shifts.

- *CSAM, at the beginning of a screening flow, used as a predictor of good or poor electrical performance of linear devices, tends to correlate with changes in electrical performance, especially in the 'tails' (<10% change, >10% change) of the distribution of changes in electrical performance.* The evaluation of a lot size of 250 units of two linear device types showed that a good CSAM inspection result tended to be correlated to good electrical performance following temperature cycling. For a subset of devices (n = 45) that were placed on life test, to simulate use conditions, the best CSAM inspection results correlated to the best electrical performance results, and the poorest CSAM inspection results correlated to devices with the largest electrical life test induced shifts.

- *Whether or not CSAM is a reliable predictor of PEM reliability under long term usage and flight conditions remains an open question for those parts which are in the middle of the distribution for delamination changes determined by CSAM.* Prudent use and the potential success of CSAM as an added-value indicator of part reliability will continue to depend on a variety of factors including among other things, the parts in question, the application environment, the mission length, the required performance of the parts, the mission criticality of the part function and even programmatic considerations such as available funding and schedule.

6.2 Recommendations

- *For critical, highly demanding and long life missions, where it is prudent to be conservative, continue to use C-SAM to determine the incoming quality and reliability of plastic encapsulated microcircuits.* During this study, Flow A (hand soldering) and Flow C (vapor phase) showed substantial electrical parametric changes in three part types manufactured by three different Vendors which correlated with topside die paddle delamination. Also, parametric shifts in electrical performance tended to correlate with CSAM inspection results, as top electrical performers correlated to top CSAM performers. These results suggest that there may be a relationship between the delamination detected in PEMs and electrical parametric changes caused by burn-in, life test, and/or difficult application environments. Further evaluation is recommended.

- Besides the electrical delamination correlation mentioned above, *C-SAM can highlight other package related anomalies which could show up as a result of mechanical stresses*.

- *Add preconditioning prior to life test as a QCI step.*

Perform related studies

- Evaluate large pin count devices encompassing large area die (e.g., memories, microprocessors, field-programmable gate arrays, application-specific integrated circuits) under conditions similar to those established for this NEPP task.

- Develop additional failure analysis methods and techniques to validate the actuality of delamination within a package.

- Develop additional methods to correlate delamination with actual electrical failures and/or package construction, materials, and processing deficiencies as cross-sectional analysis can cause and/or mask delamination.

- Evaluate temperature cycle effects on the detection and possible latent effects of delamination. Figure 5-5 illustrated an example of a part that had shown delamination following HAST testing and did not exhibit delamination following temperature cycling, suggesting that it is possible to have delamination go undetected.

7. References

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The Application of Scanning Acoustic Microscopy to Control Moisture/Thermal Induced Package Defects; Texas Instruments.

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On the Role of Adhesion in Plastic Packaged Chips Under Thermal Cycling Stress; Siemens.

Correlation of Surface Mount Plastic Package Reliability Testing to Nondestructive Inspection by Scanning Acoustic Microscopy; Texas Instruments.

The Mystery of the Cracked Dice; Analog Devices.

8. Acronym List

AMI	acoustic microimaging
C-SAM	C-mode scanning acoustic microscopy
CMeST	C-SAM Metrology Tool
CMRR	common mode rejection ratio
COTS	commercial off-the-shelf
GAIN ERR	gain error
HAST	highly accelerated stress test
HR	high risk
IC	integrated circuit
LR	low risk
MR	medium risk
MSL	moisture sensitivity level
PEM	plastic encapsulated microcircuit
VOS	off-set voltage