# Reverse-Bias Degradation of SiGe Transistors at Normal and Cryogenic Temperatures


Alexander Teverovsky, QSS Group, Inc., Ashok Sharma, NASA/GSFC,
Jeffrey Piepmeier, NASA/GSFC
Alexander.A.Teverovsky.1@gsfc.nasa.gov


A decrease in the low-current gain as a result of exposure to reverse emitter-base voltages is considered as one of the major degradation mechanisms in silicon BJTs and has been also revealed in SiGe technology transistors. According to the existing models, this degradation is due to an increase of base currents caused by generation of recombination centers at the $Si/SiO_2$ interface in the emitter-base oxide spacer. This degradation might be accelerated at low temperatures causing failures of analog and mixed-signal devices at cryogenic conditions. Reverse bias, RB, degradation depends on design and materials used, increases as the size of transistors shrinks, and should be evaluated for all devices intended for low-temperature operation conditions.

In this work, RB degradation of SiGe NPN transistors manufactured by BiCMOS 0.35 μm technology has been studied at room temperature, +125 °C, -40 °C, and –196 °C. Five groups of transistors used differed by the sizes of emitter contacts: 0.32×1.04 mm (gr. I), 0.32×2.5 mm (gr. II), 0.44×2.5 mm (gr. III), 0.32×10 mm (gr. IV), 0.32 mm × 5 mm (gr. V). Transistors were stressed at open collector conditions and E-B voltages varying from 2.5 V to 4.5 V and up to 1200 hrs duration in some cases. The results allowed for assessment of accelerating factors of degradation and prediction of long-term reliability of the devices.

Forward and reverse EB currents were found to be a linear function of the emitter length and the normalized degradation of forward base currents, $IB(t)/IB(0) = h_{FE}(0)/h_{FE}(t)$, where IB(0) and $h_{FE}(0)$ are the initial base current and gain, did not depend on the size of emitter.

Measurements of reverse I-V characteristics of E-B junctions at room temperature (RT) and liquid nitrogen (LN) conditions showed that reverse currents of E-B junctions follow the interband tunneling current formula:

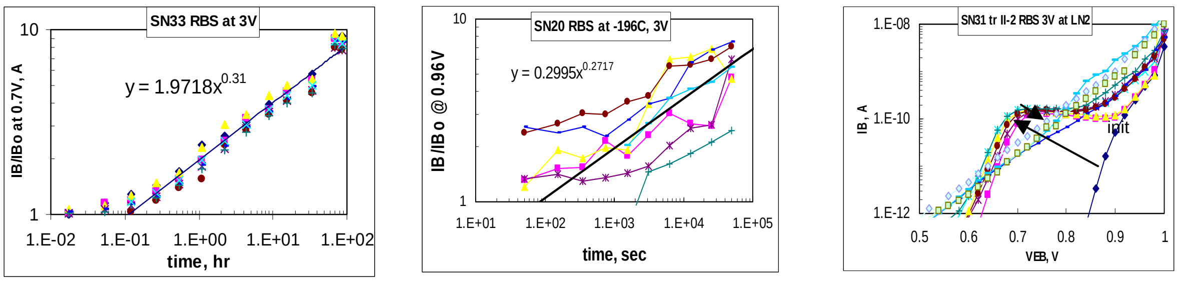
$$I_{RB} = A \times \exp\left( \frac{-B}{(V_{EB} + V_{bi})^{0.5}} \right),$$

where B is a least square fit (LSF) parameter (= 47.1); Vbi is the EB built-in voltage (=1.2 V)

The non-ideality factor of E-B I-V characteristics at RT after RB testing is close to 2 suggesting that degradation was due to increased surface recombination along the periphery of emitter. However, at -196 °C the non-ideality factor was anomalously large (n> 8), indicating that at cryogenic temperatures, the tunnel mechanism might prevail even at forward bias conditions.

Experiments showed that interim forward E-B current measurements during RB stress testing resulted in transients of reverse currents and changed the level of degradation. This indicates the importance of limiting of the maximum VF during Gummel plot testing and the necessity to be consistent during interim measurements.

Degradation of forward E-B currents as a result of exposure to reverse bias at -196 $^oC$ was less reproducible than at room temperatures (compare Fig. 1a and 1b). In some cases, anomalous behavior of forward I-V characteristics was observed (Fig.1c). In these cases, the base currents first increased sharply with time of RB resulting in a step-like I-V characteristic and then the currents decreased resulting in smoothing the "steps" and converting I-V curves to "normal" characteristics, with currents exponentially depending on forward voltages.



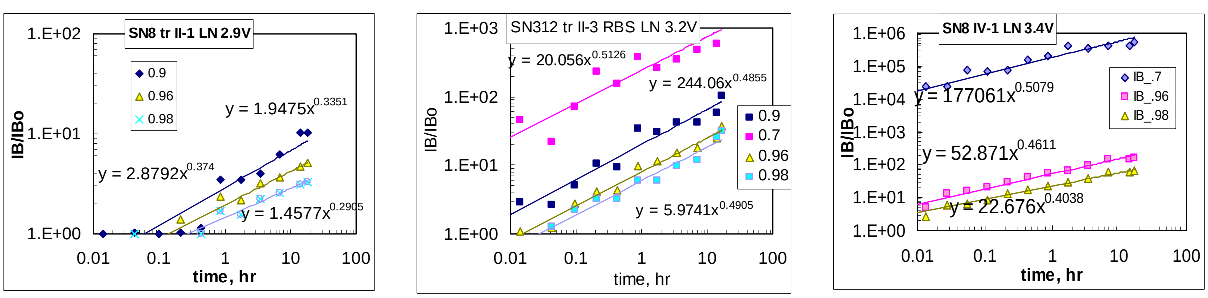

a) RBS at +25 $^oC$ b) RBS at -196 $^oC$ c) Anomalous forward IV characteristics during RBS at LN

Figure 1. Reverse bias testing at 3V and observed anomalies in forward EB I-V characteristics.

Similar to room temperature conditions, RB degradation at -196 $^oC$ (see Fig. 2) can be described with a power function:

$$IB/IBo \sim t^{\beta} \quad \text{at } t > t_i(VF),$$

where $0.6 < \beta < 0.3$, and $t_i(VF)$ is the induction period, which depends on VF. Degradation time exponent, β, has a trend of increasing at lower VF and is somewhat larger than at RT ($\beta_{avr}$ ~0.35 compared to 0.3 at room temperature).

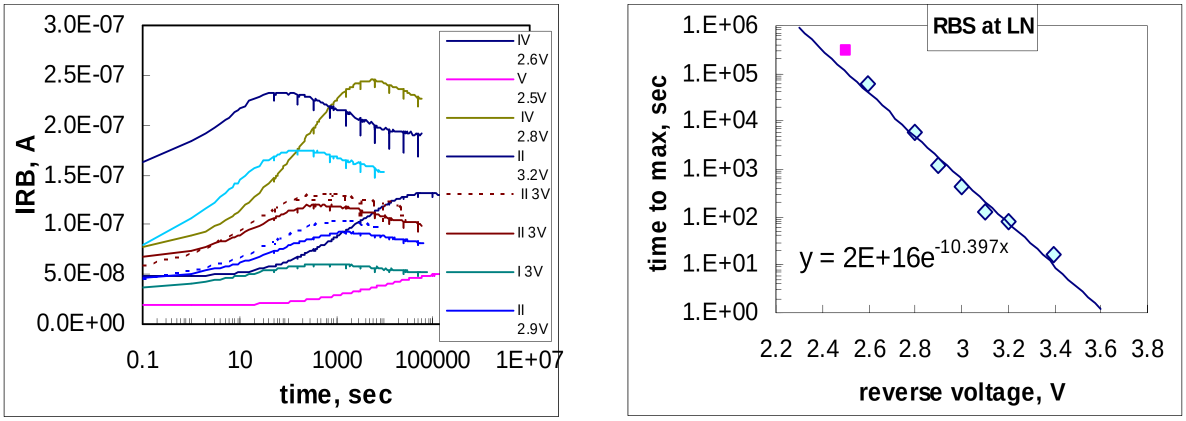



a) VRB=2.9 V b) VRB=3.2 V c) VRB=3.4 V

Figure 2. Variations of base currents, measured at VF in the range from 0.7 to 0.98 V, with time during RB testing at -196 $^oC$ and different VRB.

Kinetics of RB currents at RT and LN conditions was similar. At low voltages (VRB < 3V), the currents first increased with time, and then decreased after reaching maximum (see Fig. 3a); however, at VRB > 3.5V a decreasing section of $I_{RB}$-t curves was not observed.

Similar to room temperature conditions, the time-to-maximum of reverse current at LN conditions decreased exponentially with voltage (see Fig. 3b). Extremes in the $I_{RB}$ - t curves might indicate a change in the degradation mechanism.



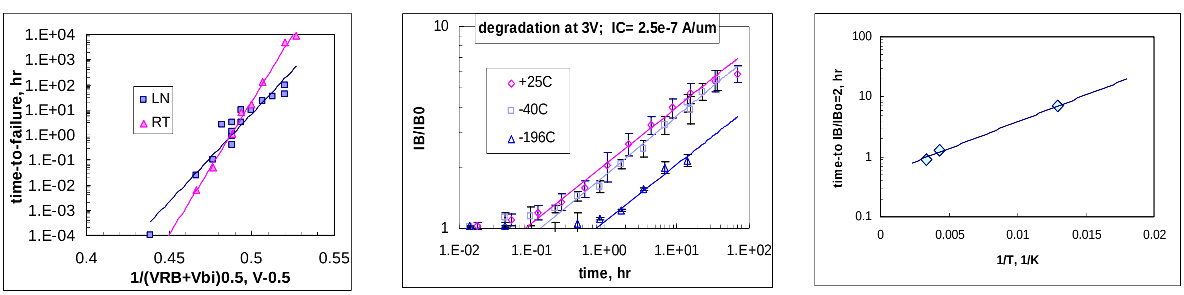

a) reverse currents at V = 2.5 to 3.2 V, T = -196 °C

b) voltage dependence of time-to-maximum $I_{RB}$ at -196 °C

Figure 3. Kinetics of reverse currents and dependence of time-to-maximum on stress voltage.

Time-to-failure, τ, (time to IB(τ)/IB(0) = 2) variations with a normalized inverse electrical field in the E-B junction [$E \sim (V+V_{bi})^{0.5}$] for room and LN temperature conditions are shown in Figure 4a. The results suggest that RB degradation increases and the time-to-failure decreases exponentially with the tunnel component of reverse E-B current, which prevails at room and low temperatures.

Figure 4b shows that variations of normalized base currents with time of RB degradation in the range from 25 °C to -196 °C can be approximated by a power law with $\beta \approx 0.3$.




a) Time-to failure as a function of reverse EB bias at +25 °C and -196 °C

b) Reverse bias test at 3V and three temperatures. Degradation is normalized to IC = 2.5×10-7 A/µm

c) Arrhenius plot of time-to-failure (IB/IBo = 2)

Figure 4. Effect of temperature and voltage during reverse bias stress testing.

A least square fit analysis has shown that experimental data on voltage dependence of τ at room temperature and -196 °C fit equally well to both approximations, the one, which is typically used in accelerated reliability testing, $\tau \sim \exp(-\alpha V_{RB})$, and the other, which is based on the voltage dependence of reverse E-B currents, $\tau \sim \exp[B/(V_{RB}+V_{bi})^{0.5}]$. This allows using a simple engineering model to describe accelerating factors of RB degradation in SiGe transistors at 2.5 < VRB< 4 V and temperatures from +25 to –196 $^{o}$C:

$$\boxed{IB/IB_0 = A \times t^{\beta} \times \exp(-\alpha \times V_{RB})} \quad , \text{ t > ti(VF)},$$

where $\beta \sim 0.3$, $\alpha \sim 4.4$ at RT and $\beta \sim 0.35$, $\alpha \sim 3.2$ at –196 $^{o}$C.

In the range from +25 $^{o}$C to -196 $^{o}$C and VRB = 3 V, the time-to-failure due to RB degradation has a weak temperature dependence with an apparent activation energy of Ea ~ 0.02 eV (see Fig. 4c). There is a trend of further decreasing of Ea at low VRB down to ~ -0.04 eV at VRB = 2.5V.

Experiments at 125 $^{o}$C have shown that RB degradation at high temperatures occurs much slower, than at RT and has a trend of saturation after a few hours of stress. These results are likely due to a decrease in the tunnel component of reverse current at high temperatures, rather than to annealing of the generated surface states.