Reliability Characterization of GaAs FET Test Structures for Applications in RF/Microwave Modules

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I. INTRODUCTION

Microwave technology, with its vast bandwidth capability, is the cornerstone of modern communications systems. Microwave systems applications in domestic and international satellite communications include personal communications systems, weather forecasting, television, and national defense applications such as reconnaissance, aircraft and missile detection, and guidance and control systems. The principal reason for fabricating microwave devices out of Gallium Arsenide (GaAs) is greater speed and performance (due to its higher electron mobility) as compared to commonly used technologies based on Silicon (Si).

GaAs has become the material of choice for manufacturers and customers in the fabrication of Monolithic Microwave Integrated Circuit (MMIC) devices for several important reasons, including the following:

1. Greater speed in performance, realized as maximum frequency of operation or higher logic switching speeds.
2. Wider frequency-bandwidth performance from the reduction of parasitics in discrete device packaging.
3. High resistivity semi-insulating property that reduces cross-talk between devices.
4. Cost reduction for medium- to large-scale production volumes.

GaAs-based microwave devices, such as power and low noise metal semiconductor field effect transistors (MESFETs), heterostructure FETs (HFETs), and pseudomorphic high electron mobility transistors (PHEMTs) have been used and continue to offer significant performance enhancements for applications in satellite- and ground-based communication systems in the Ku, K, and Ka bands (12 to 40 GHz). These devices have also shown promise for use in millimeter wave band (x > 40 GHz), as technology improvements allow device features, such as the gate lengths, to shrink. The main device feature limiting high frequency performance is the length and width of the gate. The gate length sets the high frequency limit, while the gate width defines the transconductance (g_m) and the drain-source saturation current (I_{DSS}). Device manufacturers strive to decrease the length of the gate for operations into the millimeter wave frequency band. GaAs devices are required in both receive and transmit functions of space communications systems; therefore, it is extremely vital for the space industry to understand the physics and operations of these devices.

Although all customers benefit from these advantages, the majority of devices and circuits manufactured are produced from Si for commercial applications and are tested for reliability accordingly. The degradation and failure mechanisms of Si-based devices are well understood, while GaAs reliability issues are far from maturity and are still under investigation. Space applications, which can require confidence in device performance for mission durations varying from a few weeks to several years, in addition to harsh environments, require extensive reliability testing to ensure cost-effective project planning and mission success.

Many of the tests currently conducted by manufacturers do not guarantee the reliability of their devices according to the stringent requirements necessary for military and space

applications. Although RF accelerated life testing of the RF devices would be optimal, it is quite costly. A much simpler DC testing can be used as a modest estimate to predict the RF device performance. For example, I_{DSS} can be used as an indicator of saturated power performance, and g_m can be utilized to predict gain and noise figure degradation in small signal and low noise devices. Once a device passes DC testing, it can be further characterized to study the effects of temperature cycling, accelerated life testing with RF parametric measurements. The goal of this task was to perform thermal cycling characterization of GaAs complementary heterostructure FETs (CHFETs) procured from Honeywell Solid State Electronics Center (SSEC) and to determine their performance reliability in applications utilizing RF/microwave transmit/receive (T/R) modules.

II. GaAs FET-BASED TECHNOLOGY OVERVIEW

As stated earlier, GaAs-based FETs and high electron mobility transistors (HEMTs) currently make up the vast majority of devices utilized in high frequency and high power applications. The main feature of the HEMT is the formation of the 2-D electron gas formed by the spatial separation between the charge carriers in the active channel and their parent impurities confined in the donor layer. Most recently, pseudomorphic high electron mobility transistor (PHEMT) technology, attaining superior mobility to standard FETs and HEMTs through an AlGaAs/InGaAs/GaAs structure, has been integrated into RF/microwave modules. Most developers of GaAs-based devices are now focusing on the further development and improvement of PHEMT devices.

Manufacturers currently producing GaAs-based devices for microwave applications include Agilent, Raytheon, TriQuint, and WIN Semiconductor. Table 1 provides an overview of their technology and process capabilities.

Table 1. GaAs discrete device manufacturer's technology and process capabilities overview.

				Low Noise Amplifiers	**Power Amplifiers**
Manufacturer	**Gate Length (μm)**	**Gate Width (mm)**	**Frequency Range**	**Noise Figure (dB)**	**Gain (dB)**
TriQuint	0.5 – 0.25	0.3 – 24	DC-22 GHz	1.2	1.5 – 4
Raytheon	0.25	*	4 – 40 GHz	1.4 – 2.7	N/A
Agilent	0.2	0.4 – 1.6	450 MHz – 10 GHz	0.4 – 2.2	N/A
WIN Semiconductor	0.5 – 0.15	0.3 – 1.2	15 – 100 GHz	0.4 – 1.0	18

*Information not available.

III. CHFET TECHNOLOGY

CHFET is an advanced GaAs-based IC technology that offers performance several times better than Si-based CMOS circuits. Its uniqueness lies in the fact that it is a complementary process based on GaAs as opposed to Si. It offers up to four times higher speed and draws one-sixth of the power required by Si-based CMOS devices. In addition, CHFETs have inherent radiation hardness and are suitable in high performance photodetectors for integrated optoelectronic applications. Superior performance of GaAs CHFET technology also includes low static power dissipation. In an ideal case, CHFET circuits dissipate zero static power and dissipate power only during the switching process. However, the attainment of the low static power requires both the n- and p-channel devices to be enhancement-mode devices. Their threshold voltages are typically set to be 20% of the supply voltage, so that neither device is turned on for quiescent high or low input voltages. Gate leakage current must also be limited, so as not to affect the logic swing of the circuit or contribute to the static power dissipation.

The advantage of CHFET circuits comes from the higher attainable carrier mobilities in III-V compounds. In the case of GaAs, the electron mobility is much higher than that of the Si, while the hole mobility is much lower. As a result, the p-channel devices limit the speed of GaAs-based complementary circuitry. Therefore, n-channel circuits, such as the MESFET and direct-coupled FET logic (DCFL), have been generally preferred. Enhanced hole transport in p-channel AlGaAs/GaAs HEMTs has increased the attention on various CHFET approaches. CHFET architectures based upon AlGaAs/GaAs HEMTs, metal insulator semiconductor FETs (MISFETs), semiconductor insulator semiconductor FETs (SISFETs), and quantum well (QW)-MISFETs are currently being explored.

The CHFET is an enhancement mode device whose operation is analogous to that of a Silicon CMOSFET. Applying a suitable gate voltage induces a charge to accumulate in the channel by drawing carriers from the source: electrons in the case of n-channel devices and holes in p-channel devices. The dielectric (for example, undoped AlGaAs insulator/barrier layer) plays a role analogous to the oxide in a MOS transistor. It provides a potential barrier that confines the channel charge, preventing conduction between the channel and the gate. It is expected, however, that some leakage current through the gate exists, caused by field emission (quantum mechanical tunneling of the carriers through the potential barrier) and thermionic emission of the carriers over the barrier. The magnitude of this current is likely to depend strongly on the gate voltage and the device temperature.

Honeywell GaAs CHFET technology incorporates an $Al_{0.75}GaAs/In_{0.25}GaAs/GaAs$ heterostructure and bandgap engineering techniques to maximize gate isolation. The InGaAs channel is used because of the higher electron velocity [1]. Figure 1 represents the typical n- and p-channel structure used in the Honeywell GaAs CHFET technology.

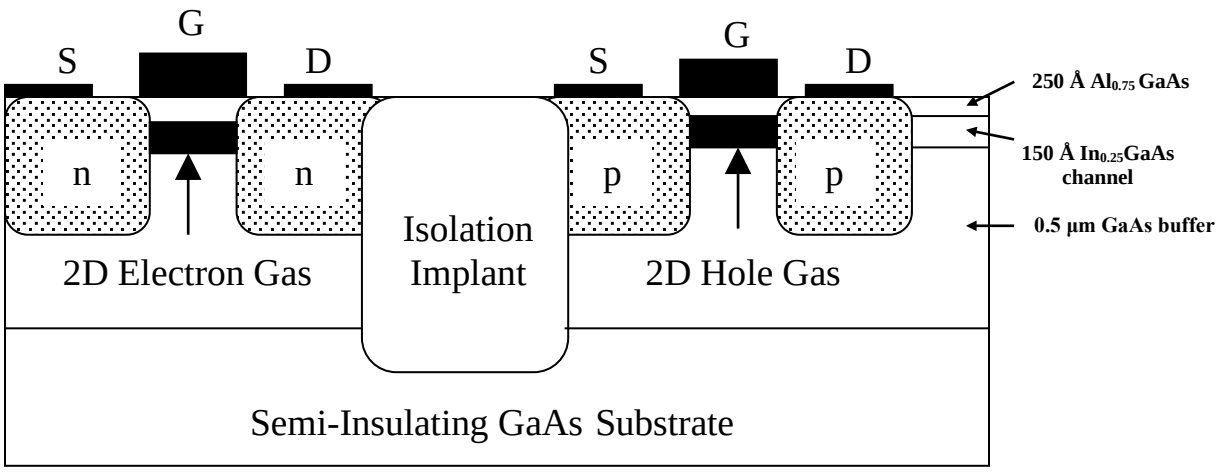

Figure 1. Basic Honeywell CHFET structure.

The $Al_{0.75}GaAs$ layer (with an energy bandgap of approximately 2 eV at room temperature) acts similarly to the gate oxide in Si-CMOS, reducing the gate leakage current from that of a comparable bulk GaAs MESFET. The $In_{0.25}GaAs$ layer forms the channel of the device and provides a 30% enhancement in lattice mobilities as compared to bulk GaAs for both electrons and holes. A silicon delta-doped layer is located below the InGaAs channel to provide control of the threshold voltages. The transistor gate lengths are 0.7 µm. InGe is used for making ohmic contacts and WSi for Schottky contacts. Fabrication is based on a self-aligned GaAs HFET process. Table 2 shows typical process parameter characteristics for a Honeywell GaAs CHFET.

Table 2. Typical parameters, Honeywell GaAs CHFET (0.7 µm length, 20 µm width).

	Parameter	**Value**
Threshold Voltage	Vtn	0.2 V
	Vtp	0.3 V
Gain Factors	β_n	6 mA/V^2
	β_p	0.6 mA/ V^2

CHFET technology allows for the combination of low power and high speed, unlike Si-based technologies. Figure 2 shows power versus frequency for a buffered CHFET technology versus SOI CMOS process, two-input NAND gate [2].

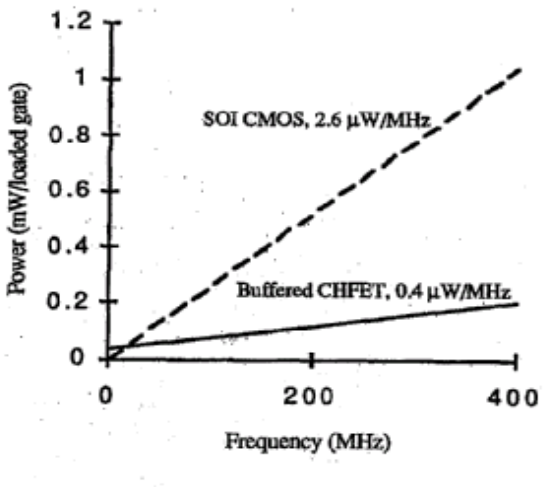

Figure 2. Power dissipation at 100% duty cycle for a buffered CHFET versus SOI CMOS process, two-input NAND gate (having the same gate width, gate length, and gate capacitance) with a fan out of two, and 0.2 pF capacitance at 85 °C.

The appendix contains the following CHFET technology electrical characteristic details:

A1. 4-Inch CHFET Map for Wafer #13 fabricated by Honeywell SSEC.
A2. I-V Characteristics for several CHFET devices fabricated on Wafer #1, taken at room temperature, 25 °C.
A3. 4-Inch CHFET Map for Wafer #9 fabricated by Honeywell SSEC.
A4. I-V Characteristics for several CHFET devices fabricated on Wafer #9, taken at room temperature, 25 °C.

IV. MAJOR RELIABILITY ISSUES FOR GaAs FET STRUCTURES

GaAs FETs represent the key semiconductor devices for high reliability applications. Therefore, determining their long-term stability, especially under harsh environments, is a crucial aspect of the evaluation process. Reliability work on compound semiconductor device technology was first concentrated on discrete components such as small signal GaAs MESFETs [3]. A large reliability base now exists for such devices. Less progress has been made on reliability problems associated with HEMT and PHEMT structures. Also, the reliability issues of power GaAs FETs have yet to be fully understood when operated at high temperatures under high bias for long periods of time.

Although HFET/HEMTs and PHEMTs suffer from many of the same reliability issues as the MESFETs, new issues are introduced from the heterostructure junctions forming the 2-D electron gas (2DEG). The reliability of HFET/HEMTs and PHEMTs is affected by the epitaxial structure, device fabrication, and device geometry. Burn-in screening, stressing the circuit above the normal operating conditions to accelerate early failures, should be performed prior to any extensive reliability testing in order to detect early failures that might occur from latent defects. The dominant reliability issues of GaAs HEMT and PHEMT structures are contact (ohmic and Schottky) degradation, 2DEG

instability, trap-related effects, and hydrogen poisoning occurring in hermetically sealed packages. Packaging issues must also be addressed, especially with the current trend of encapsulating MMICs in non-hermetic plastic packages for which the reliability data available is minimal.

Ohmic Contact Degradation

Ohmic contacts with low resistivity and uniform interface are essential in developing reliable HEMT/PHEMT structures. Source resistances should be minimized and remain stable during the operating life of the devices to maintain a low noise figure, which is one of the key parameters of HEMTs. An increase in source-to-drain resistance can usually be attributed to metal-semiconductor interactions occurring during the high temperature device operation. Under the normal operating conditions, the standard ohmic contact metallization scheme of AuGeNi is found to perform well. However, at elevated temperatures, Ga outdiffusion, Ni- and Au-indiffusion, and the formation of various intermetallic phases can result in degradation of ohmic contact characteristics.

Gate Contact and Channel Degradation

The performance of GaAs-based devices relies predominantly on the quality of the active channel area of the device—the area under the gate. Interdiffusion of the gate metal with GaAs results in a reduction of the active channel depth and a change in the effective channel doping. This phenomenon is referred to as the "gate sinking." Gate structures are based on the industry standard Au/Pd/Ti or Au/Pt/Ti. Au has a high diffusion factor, which is negligible at room temperature. However, with large surface defects, after accelerated life tests or operation at elevated temperatures, the rate of gold diffusion cannot be ignored; it commonly leads to degradation in the device performance manifested as a degradation in drain current, reverse breakdown voltage, and input capacitance.

Channel degradation can also occur due to the gate sinking and/or diffusion of impurities or defects from the substrate to the channel layer, causing an increase in the impurity scattering in the undoped channel layer, and thus deteriorating the high electron mobility of the 2DEG.

Trap-Related Effects

The deep levels associated with defect centers in doped AlGaAs may strongly modify the electrical properties of HEMTs, leading to low temperature collapse of the drain current, persistent photoconductivity, and high levels of low frequency noise.

Hydrogen Poisoning

An important problem that has received considerable attention recently is hydrogen poisoning of the hermetically sealed devices, a condition that is aggravated at high temperatures. It has been found that the PHEMTs and MMICs degrade rapidly due to the hydrogen evolution and interaction with the active devices in a sealed package that can result in predicted lifetimes of only 8 years in some applications.

V. CHFET RELIABILITY STUDIES

Although commercial reliability standards are required by all high temperature electronic components, not many studies of high temperature reliability have been documented in the literature. Conferences on high temperature electronics have been the main forum for such publications [4-14]. Previous studies have concentrated on interconnections [1], reliability modeling [5,8], metallization studies [7,9], passive components [14], and high temperature reliability studies of active devices [6,10-13].

High temperature digital operation of CHFETs has been studied to a maximum temperature range of up to 500 °C [15]. Test results showed that the n-channel devices were capable of digital operation to at least 400 °C, while p-channel devices failed at lower temperatures. At elevated temperatures, leakage currents showed high degradation in both n- and p-channel devices.

An accelerated life test reliability study was performed on CHFET MMICs, designed to deliver 29 dBm of output power across a 6 to 18 GHz bandwidth. The CHFET MMICs were deliverables on the MMIC program. The active devices are 0.25 μm gate length AlGaAs/InGaAs FETS with Ti/Pt/Au gates and Au/Ge/Ni ohmic contacts. A distributed input stage contains four CHFETs, each with a gate width of 850 μm. The circuits also contain passive interconnects, matching and biasing elements such as thin film resistors and metal insulator metal (MIM) capacitors. A thin layer of plasma enhanced chemical vapor deposition (PECVD) deposited silicon nitride was used for device passivation and as the insulating layer in the MIM capacitors. Via-hole technology was used to provide low inductance paths to ground for the CHFET source contacts and the bottom plates of the MIM bypass capacitors.

The MMIC chips were attached by the manufacturer to gold-plated copper-molybdenum carrier plates with an Au/Sn eutectic solder process to ensure the electrical, mechanical, and thermal integrity of the die attach over a long time period and wide temperature range. Copper-molybdenum was selected for the carrier plate material because it has similar thermal expansion properties to those of GaAs. Gold-plated brass test fixtures, designed to accommodate the carrier plates, were used for S-parameter measurements and for high temperature RF life testing. Each fixture included a center block to support a carrier plate with attached MMIC, and two end pieces, each with a microstripe-to-SMA type adapter and a coaxial DC feed-through connector. Wire bonds were used for all DC and RF connections, to ensure better measurement repeatability over time and temperature. During the life testing, a metal block was attached directly beneath each test fixture centerpiece and was heated with a small cartridge-heating element, thus minimizing temperature effects on the surrounding components.

A computer controlled RF life test system was used in this study. High power X-band dielectric resonator oscillator (DRO) sources, each followed by a four-way power divider, were used to drive out eight test channels. High temperature RF life tests were performed on 10 MMICs, each at several base plate temperatures. During the life tests, the circuits were biased at a certain voltage that was required to achieve desirable compression at room temperature. In order to ensure that all the MMICs at a given base

plate temperature were stressed at the same channel temperature, the gate voltage was adjusted periodically so that the power dissipation was the same for each MMIC throughout the life test. Prior to life testing, and at intervals of approximately 500 hours, the MMICs were measured at room temperature on the life test system to check for degradation in the drain current and large signal RF output power, and also on a separate network analyzer to check for degradation in the small signal S-parameters. These measurements were performed at an optimum drain voltage and the initial gate voltage that was required to achieve a substantial drain current before life testing. Failure was defined as a 1 dB decrease in large signal output power or the small signal S-parameter S21, or a 20% decrease in the DC drain current as measured at room temperature. All testing was performed in accordance with the JPL [16] and JEDEC [17] guidelines.

The primary failure mode in this life test was gradual degradation of one or more of the parameters designed as failure criteria. In fact, all MMICs exhibited decreases in output power, drain current, and small signal S21 to varying degrees. In order to calculate the expected lifetime of the circuits at actual use temperature, an activation energy was calculated from the life test failure distributions using an analysis methodology in accordance with JPL and JEDEC guidelines.

VI. CHFET THERMAL CYCLING TEST PROCEDURES

In order to space qualify CHFETs, this test plan was submitted to fulfill the thermal cycling (TC) test plan requirements, with the following objectives:

1. Conduct a literature search to determine what results have been previously reported concerning the thermal cycling/temperature stressing of CHFET parts.
2. Electrically characterize CHFET chips fabricated by Honeywell SSEC prior to thermal cycling.
3. Subsequent to thermal cycling, perform electrical characterization again to detect any degradation or catastrophic failure events occurrence.

The major activities that were performed as part of TC of CHFETs, with the goal of device qualification, are listed as follows:

1. A literature search was conducted to determine what results had previously been reported concerning the thermal cycling of CHFETs. Approximately 40 references were found through the NRL Library system, and the Honeywell CHFET Web site was also reviewed. The information gathered from these references was used as background information that was helpful in generating the test plan for the CHFET devices supplied. Although Honeywell provided minimal background information about the proprietary process, the literature search revealed that the CHFET structure had been developed with an $Al_{0.75}GaAs/In_{0.25}GaAs/GaAs$ structure, InGe alloyed ohmic contacts, a WSi gate metallization, and off-substrate gold interconnects, which were suitable for commercial digital integrated circuits.

2. Ten chips were supplied, each of which contained many individual CHFETs, with common gates all connected. Two of the chips were cracked into two pieces,

evidently as a result of some prior incident. The two chips that were cracked into pieces were used for preliminary testing. A total of eight individual CHFETs were electrically characterized, with at least two devices from each chip. One bare die was used as a control before and after the TC tests. Figure 3 shows a representative CHFET device shown from the drain end. Each bare die contained 38 columns of FETs, with five pairs of source and drain contact pads per column, and interconnected gate contacts at the top and bottom of each column.

3. CHFET chips fabricated by Honeywell SSEC were electrically characterized prior to thermal cycling, using an HP Curve Tracer to determine relevant electrical characteristics (I-V curves).

4. An additional parameter used for failure analysis was the small signal parameter S21 measured across the band from 2 to 8 GHz at room temperature in a separate measurement setup.

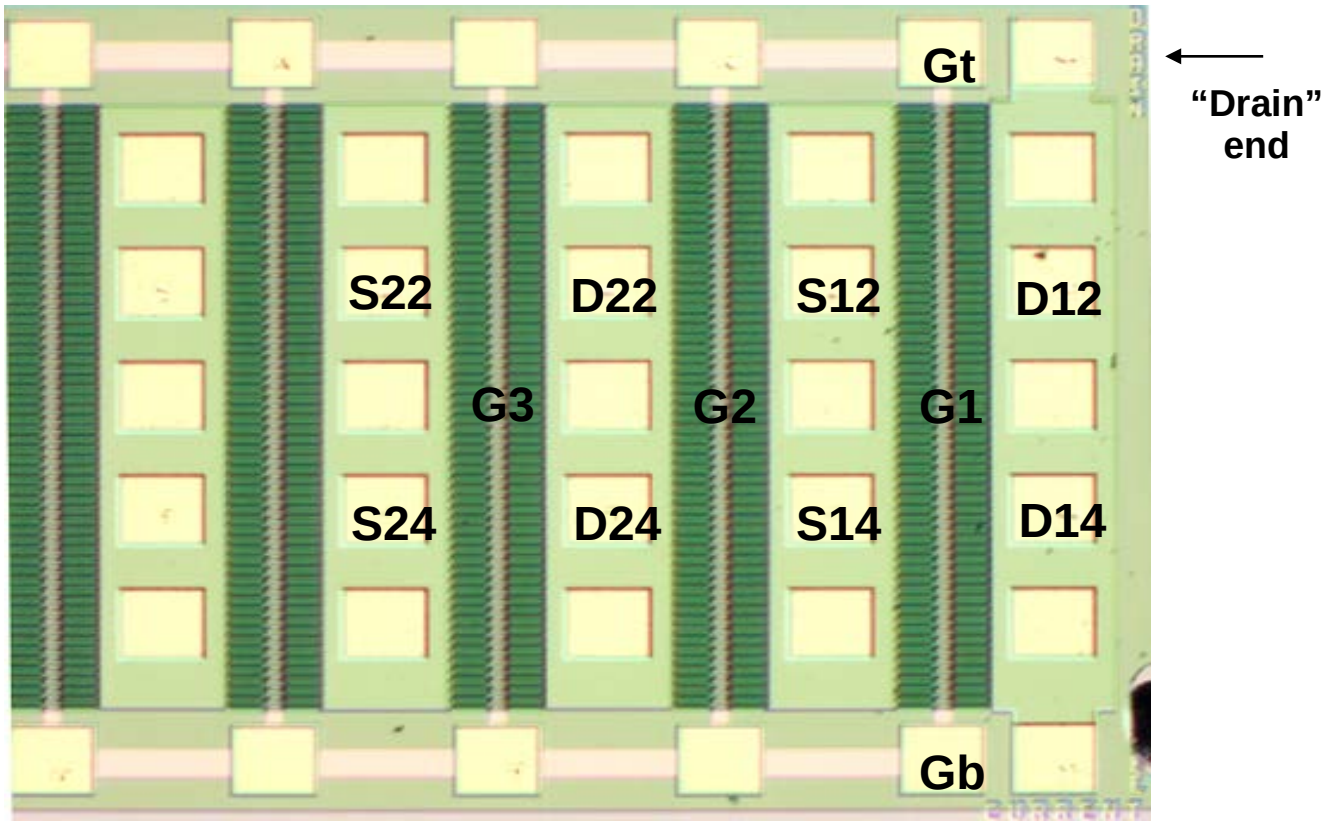

Figure 3. Drain end of a CHFET bare die at 50x magnification. D## = drain/column #/row #; S## = source/column#/row#; G# = gate column #; Gt/b = gate top/bottom.

1. Other tests done at the circuit level included a bake test for mobile ions, as well as electrical measurement of the combined via plus die-attach resistance. Electrical measurements included low frequency transconductance measurements of the CHFET. This was possible without modification to the circuits because the other circuit elements all had negligible effect at low frequencies. This test may often indicate no role of mobile ions or degradation of the via plus die-attach resistance.

2. CHFET chips that had been electrically characterized were placed in a thermal control chamber and TC performed according to the NASA GaAs MMIC Reliability Assurance Guideline for Space Applications (JPL Publication 96-25, 15 December 1996, p. 164). The chips were cycled between -65 °C and 200 °C for a total of 15 cycles. One chip was held back as a control and was not temperature cycled. As stated in the guidelines, packaged devices are normally used for the TC test "to detect flaws or weak point in the die attach, wire bonds, and package seals that would normally result in early failures." However, there are also thermal/mechanical stresses between the metallization and the semiconductor layers and between the heterojunction semiconductor layers. The objective of TC was to evaluate any degradation at the chip level.

No information was available about the intended application or packaging scheme for these devices.

3. After the thermal cycling tests were completed, the post-thermal cycling electrical characterizations were performed again, and any changes in electrical characteristics were noted. Failure was defined as a 20% change in drain current, gate leakage current, or threshold voltage.

VII. CHFET THERMAL CYCLING RESULTS

Normally, S21 and the output power degraded simultaneously as measured at the life test frequency. Also, fairly uniform S21 degradation across the frequency band was normally visible after life test. Occasionally, the failures due to S-parameter change were not distinguished from the failures due to a change in the RF output power. Also, at certain frequencies, S21 changes insignificantly after life testing.

Tables and figures of the results and testing conditions are shown on the following pages. Tables 3 and 5 show the NPN and PNP data of the devices that were actually thermally cycled. Note that for all devices, the change between uncycled and cycled saturated current was less than the 20% failure criteria. Therefore, all devices were considered to not have failed. Tables 4 and 6 show the NPN and PNP electrical characteristics, respectively, for the control sample (#8). The data for the control sample FETs were all within the 20% change criteria. The NPN characteristics are the predominant electrical measurements in this study. Figure 4 shows the typical I-V characteristics for an NPN device, and Figure 5 for a PNP device, before and after thermal cycling.

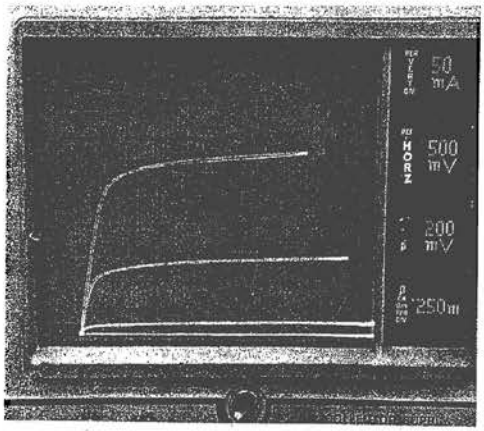

Figure 4a. Device #2 (2UD12G1T) npn characteristics before cycling.

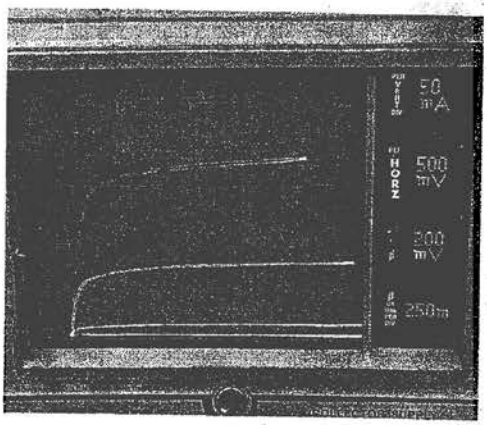

Figure 4b. Device #2 (2UD12G1T) npn characteristics after cycling.

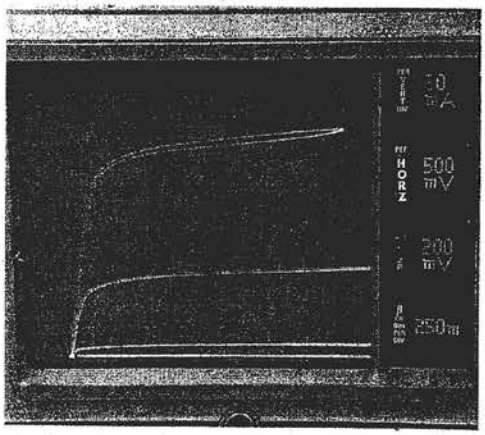

Figure 5a. Device #7 (7UD12G1T) npn characteristics before cycling.

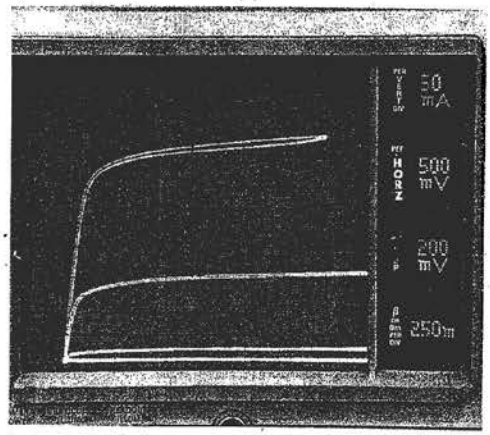

Figure 5b. Device #7 (7UD12G1T) npn characteristics after cycling.

Failure analysis was not performed because there were no failed parts. The devices showed no signs of obvious degradation under an optical microscope.

Although all devices were analyzed through parametric degradation, there were no signs of obvious damage to the surface passivation or metallization of the thermally tested MMICs by observation with an optical microscope.

Table 3. NPN electrical characteristics before and after thermal cycling for seven CHFET chips.

		NPN				
		Id @ Vds = 2.5V, Vgs = 0.6V (mA)			**Iu – Ic**	
Sample	**Device**	**Uncycled**	**Cycled**	**Iu – Ic**	**20%max allowable change (mA)**	**Actual change (%)**
1	D1	330	285	45	66	-14
1	D20	330	330	0	66	0
2	D1	320	330	-10	64	3
2	D20	330	330	0	66	0
3	D1	315	315	0	63	0
3	D20	330	350	-20	66	6
4	D1	310	320	-10	62	3
4	D20	345	375	-30	69	9
5	D1	400	360	-40	80	-10
5	D20	425	425	0	85	0
6	D1	380	345	35	76	-9
6	D20	435	410	25	87	-6
7	D1	375	360	15	75	-4
7	D20	410	410	0	82	0

Table 4. NPN electrical characteristics before and after thermal cycling for the control CHFET chip.

	NPN Control Sample 8: D12G1T			
	Id @ Vds = 2.5V, Vgs = 0.6V(mA)			
Cycling Samples	**Before Cycling**	**After Cycling**	**Ib – Ia**	**Ib – Ia Change (%)**
Sample 1	325	325	0	0
Samples 2,3,4	325	330	-5	2
Samples 5,6,7	330	350	-20	6

Table 5. PNP electrical characteristics before and after thermal cycling for seven CHFET chips.

		PNP				
		Id @ Vds = 0.8 Vgs=0.8V (mA)			Iu – Ic	
Sample	**Device**	**Uncycled**	**Cycled**	**Iu – Ic**	**20% max allowable change (mA)**	**Actual change (%)**
1	D1	250	*	*	50	*
1	D20	200	190	10	40	-5
2	D1	225	225	0	45	0
2	D20	230	200	30	46	-13
3	D1	200	225	-25	40	13
3	D20	150*	*	*	30	*
4	D1	215	225	-10	43	5
4	D20	150*	*	*	30	*
5	D1	210	200	10	42	-5
5	D20	205	210	-5	41	2
6	D1	230	275	-45	46	20
6	D20	245	255	-10	49	4
7	D1	220	210	10	44	-5
7	D20	230	200	20	46	-9

*Insufficient data—cannot be measured.

Table 6. PNP electrical characteristics before and after thermal cycling for the control CHFET chip.

	PNP Control Sample 8: D12G1T			
	Id @ Vds = 0.8V, Vg s=0.8V (mA)			
Cycling Samples	**Before Cycling**	**After Cycling**	**Ib – Ia**	**Ib – Ia Change (%)**
Sample 1	200	215	-15	8
Samples 2,3,4	215	205	10	-5
Samples 5,6,7	205	230	-25	12

VIII. SUMMARY

CHFET chips manufactured by Honeywell SSEC were obtained for reliability testing, including thermal cycling characterization. These chips contained several NPN and PNP transistors. A total of eight chips were electrically characterized with at least two devices from each chip. One device was used as a control sample for before and after TC testing. The devices were cycled between -65 ºC to 200 ºC for a total of 15 cycles, in accordance with NASA MMIC Reliability Assurance Guidelines for Space Applications. Failure was defined as a 20% change in the drain current, gate leakage current, or threshold voltage. The pre- and post-thermal cycling measurements showed that all devices did not exceed the 20% change criteria and were considered as passing. No signs of device degradation were observed during optical inspection after completion of thermal cycling.

IX. RECOMMENDATIONS

CHFET technology was developed by Honeywell SSEC and partly funded by NASA/JPL for X2000 and Europa Orbiter program. This technology was pursued because of the advantages offered of inherent radiation hardness combined with high frequency operation at reduced power consumption. Honeywell SSEC is no longer offering CHFET technology development for space applications because of funding cutbacks.

Therefore, it is recommended that some alternative technologies such as pseudomorphic high electron mobility transistors (PHEMTs) and compound semiconductor devices such as Gallium Nitride (GaN) FETs should be evaluated to determine their suitability in space applications

ACKNOWLEDGEMENTS

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APPENDIX

A1. 4-Inch CHFET Map for Wafer #13 fabricated by Honeywell SSEC

A2. I-V Characteristics for several CHFET devices fabricated on Wafer #13 taken at room temperature, 25 ℃

A3. 4-Inch CHFET Map for Wafer #9 fabricated by Honeywell SSEC

A4. I-V Characteristics for several CHFET devices fabricated on Wafer #9, taken at room temperature, 25 ℃