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NASA Electronic Parts and Packaging Program
Technology Information for Future NASA Missions

NEWS FLASH NOVEMBER 2001

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Building Reliability into ASIC Design

Jonathan Perret
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Work performed under the Innovative Parts and Packaging Assessment and Qualification (IPPAQ) task within the NEPP Program has identified the key processes for qualifying complex mixed signal ASICs for space applications. The emphasis in this work was to achieve qualification by including design validations that are completed during the ASIC design phase, rather than after the fact when the ASIC has been built. A methodology flow was implemented to control the design flow and verification steps for both digital and analog mixed signal devices making up a complex ASIC. This design flow verification methodology has been used to implement reliable ASIC designs for an actual flight project application. Specific design requirements were developed in order to standardize the Europa PDR and CDR design review process for ASICs to be used in Europa flight systems. In the course of this implementation, the following seven new design principles/best practices were developed to help insure the production of flight qualifiable ASICs:

- Verify that the ASIC design is functional in the system via behavioral modeling prior to fabrication.
- Verify that ASIC hardware and software designs are compatible prior to fabrication. Verify back-annotated ASIC netlist prior to fabrication.
- Validate IP design compatibility prior to ASIC integration.
- Validate ASIC specification quality and control.
- Validate that screening tests are compatible with ASIC design verification prior to fabrication.
- Validate node-toggle (IDDQ), stuck-at-fault test coverage of digital ASIC designs prior to fabrication.

These design principles are generally applicable and will help to insure that ASICs for NASA flight systems have built-in high probability of being easily flight qualified.

View the article in PDF.

Thermo-Mechanical Characterization of Motorola MMA1201P Accelerometer Test Report

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Motorola MMA1201P is a single-axis, surface micromachined MEMS accelerometer rated for ± 40 G and is packed in a plastic 16-lead DIP package. The operating temperature range is -40 ° C to +85 ° C with a storage temperature range of -40 ° C to +105 ° C. The part can sustain accelerations up to 2000 g from any axis, while unpowered and powered accelerations up to 500 g. The main components of the MMA1201P consist of a surface micromachined capacitive sensing cell (g-cell) and a CMOS signal conditioning ASIC. The g-cell's mechanical structure consists of three consecutive semiconductor plates, defining sensitivity along the Z-axis (orthogonal to flat plane of the chip). A fourth semiconductor plate located in the g-cell allows testing of the accelerometer mechanics and electronics.

A total of 70 of these Motorola MEMS accelerometers were subjected to Incoming Inspection. The Incoming Inspection consisted of visual examination, serialization, X-ray, Thermal Cycling within Low Range -40 to +105 ° C (25 samples) and Thermal Cycling Extended Range -65 to +155 ° C (25 samples). Electrical tests were performed after 100, 200, 500, and 1000 cumulative cycles. Twenty parts were subjected to Mechanical Shocks (MS) of 2000 g with electrical tests after 30, 130, 430, 1430, 2500, 5000, 10000 cumulative shocks.

Preliminary test results show no failures during low TC range testing till 100 cycles and 4% parts failing post 300 - 1000 TC electrical tests. During extended range TC testing, 8 % parts failed post 30 TC electricals and 96% parts failed post 300 electricals. Mechanical shock testing showed no failures till 16 MS and 16 - 20% failures from 130 - 10,000 MS. The failed parts were subjected to failure analysis. Analysis indicated that temperature cycling caused the shrinkage of the internal silicon glop surrounding the sensor, resulting in broken internal wires and accelerometer failure. The failure mechanism for the parts failing shock testing has not been determined yet. However, the hybrid construction of the part suggests that multiple shocks in the z-axis might overstress the fragile silicon membrane of the transducer. These parts are not recommended for use in rugged environment and space flight applications.

View the complete Motorola MMA1201P MEMS Accelerometers Test Plan and the Final Test Report on the NEPP Web Site.

View the summary article in PDF.

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Electromigration Failure in Au and Joule Heating Induced Oxidation in Cu Conductors

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Background/Motivation
Electromigration is the mass transport of a metal due to the momentum transfer between conducting electrons and metal atoms. Electromigration was discovered more than 100 years ago and it has been a problem ever since. As device features reduce in Ultra-large-scale integrated circuits, current densities increase with the metallization layer complexity. These issues make understanding Electromigration (EM) induced failure essential to design more reliable circuits.

In this work, electromigration of copper and gold conductors targeted for micro-inductors in System on a Chip (SoC) application is studied. We intend to use this study to predict:

- Maximum current densities that can be used in micro-inductor interconnects.
- Expected device life-time under use conditions.
- Identify EM failure mechanisms in SoC metallization structures.

Discussion of Results
One of the main findings from this work was the very high exponent (n=3.2) for the current density

found for Au conductors, as compared to n=1.7 for standard commercial Al:Cu structures. Also, the Au (and Cu) conductors were not able to withstand moderate current densities. The low current densities that caused significant degradation can become a problematic even in normal (rather than accelerated) use conditions. Some of the reasons for these differences when compared to Al:Cu could be:

- The Al:Cu were bamboo structures, where since the line dimensions are of the order of grain sizes, very little grain boundary diffusion occurs. With these structures, Average grain sizes (~ 1 micron) are smaller than conductor dimensions (10 by 4 microns) making grain boundary diffusion an important mechanism which accelerates electromigration (grain boundary diffusion has a lower activation energy than bulk diffusion so electromigration occurs at lower temperatures)
- Al forms a very tough oxide (Al_2O_3), which is almost lattice-matched to the parent metal (Al). This has the effect of passivating the surface, so surface diffusion is very low. Au on the other hand, does not form oxides, so the surface is free to act as an additional diffusion path. This again, has the effect of diminishing the total or "effective" activation energy for electromigration.
- Poor adhesion was found in several of these structures, and delamination of he metallization was often a problem. At elevated temperatures, this could become a problem if delamination occurs in part of the conductor. Since the delaminated area would be dissipating less heat, a thermal gradient could occur and this could accelerate electromigration. During the testing, the increase in resistance with temperature was monitored at very low current densities. The current density was then increased to the test conditions, and the sample resistance was monitored for increases that can be due to Joule heating. This did not seem to be a problem, but if delamination later occurred during the test, then it could explain failure of the metal lines toward the middle portion of the lines, as is seen in the failure analysis. It is also well known that if the current density was too high (causing Joule heating even with good adhesion) the failures would have been observed near the bond pads.

Summary of Findings:

- Au test structures could only withstand current densities (j) < 9 x 10^5A/cm^2 (at 200 C). At this value of j the interconnects failed in less than 15 minutes.
- In Au structures, times to failure vs current density have been used to determine the value of the exponent (n) in Black's equation, where meantime to failure (mttf) = A j^{-n} e $^{Ea/kT}$,where we found that n=3.2
  This exponent is much larger than what was obtained for Al:Cu lines under similar conditions. We attribute this large exponent value to the fact that we do have grain boundary diffusion, surface diffusion, and poor adhesion of the metal lines to the substrates.
-

At current densities > 1.8 x 10^5A/cm^2 recovery is observed in Au interconnects. After a first increase in line resistance, the value of the resistance drops, showing an apparent "recovery".

- Measurements of lifetimes at different current densities in air and at 60ºC show that failure of unprotected Cu lines are mainly due to oxidation failure.

View the complete Electromigration Failure in Au and Joule Heating Induced Oxidation in Cu Conductors on the NEPP Web Site in 3 Parts.

- Part 1
- Part 2
- Part 3

View the summary article in PDF.

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Evaluation of Data Retention Characteristics for Ferroelectric Random Access Memories (FRAMs)

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Alexander Teverovsky, Ph.D.
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Abstract

Data retention and fatigue characteristics of 64 Kb PZT-based FRAM microcircuits manufactured by Ramtron were examined over temperature range from -85°C to +310 °C for ceramic packaged parts and from -85°C to +175 °C for plastic parts, during retention periods up to several thousand hours. Intrinsic failures, which were caused by a thermal degradation of the ferroelectric cells, occurred in ceramic parts after tens or hundreds of hours of aging at temperatures above 200 °C. The activation energy of the retention test failures was 1.05 eV and the extrapolated mean-time-to-failure (MTTF) at room temperature was estimated to be more than 280 years. Multiple write-read cycling (up to 3x107)

during the fatigue testing of plastic and ceramic parts did not result in any parametric or functional failures. However, operational currents linearly decreased with the logarithm of number of cycles thus indicating fatigue process in PZT films. Plastic parts, that had a more recent date code as compared to ceramic parts, appeared to be using die with improved process technology and showed significantly smaller changes in operational currents and data access times.

This paper will be presented at NVMTS2001 Conference, San-Diego, CA in November 2001.

View the article in PDF.

CALCE Electronic Products and Systems Center Technical Review and Planning Meetings

Ashok K. Sharma
Goddard Space Flight Center/NASA

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Computer Aided Life Cycle Engineering (CALCE) Technical Meetings Overview

A bi-annual CALCE Consortium Technical Review and Planning Meeting was held at the University of Maryland, College Park, MD campus on October 9-11, 2001. The main purpose of this meeting was to present to the CALCE consortium members, the status of on-going research in electronic component testing and packaging; including effects of environmental stresses on reliability, Computer Aided Life Cycle Engineering and Physics of Failure (PoF) models. The technical review meetings were divided into two sections, with the first two days devoted to presenting of status of on-going (Year 2001) projects, and the third day reserved for Year 2002 project proposals.

The CALCE research program theme is focused on the identification and development of technologies, methodologies, and guidelines for assessing, mitigating, and managing the risks associated with the design, manufacture and fielding of electronic products and systems. This past year, under consortium project C01-05, CALCE has been working on creating a guidebook for Plastic Encapsulated Microcircuits (PEMs). This guidebook provides information useful is assessing the reliability of PEMs

in high altitude applications, especially those involving exposure to rapid altitude cycling. The CALCE webbooks are continuing to be refined and updated with information and test results, as they become available from the projects.

Several on-going projects at CALCE, as well as the ones proposed for 2002, have a NEPP Area of Emphasis (AOE) associated with it. Examples for both the current year (2001) and the projects proposed for 2002, along with the NEPP Areas of Emphasis are listed below.

CALCE Current Projects (Year 2001)

1. Guidebook on the Use of PEMs at High Altitudes and in Space - Extreme Environment Electronics and Packaging
2. Integral and Integrated Passives Web Book Update (3 parts) - Substrates and Embedded Passives Technologies-
    - Part 1
    - Part 2
    - Part 3
3. Effect of Proof Testing on Optical Fiber Fusion Splices - Photonic Systems and Devices
4. MEMS Sensors and Carrier-Level Reliability - MEMS/MOEMs Reliability Assurance
5. Compatibility of Current Components with Lead-Free Solder Reflow Profiles - Advanced Interconnect Reliability

CALCE Proposed Projects (Year 2002)

1. Reliability of Optical Interfaces to MEMS - MEMS/MOEMs Reliability Assurance & Photonic Systems and Devices
2. Embedded Passive Reliability and Tradeoff Analysis- Substrates and Embedded Passives Technologies
3. Guidelines and Improvements for Conducting Virtual Qualification (CADMP-II/calcePWA) - Development of Innovative Qualification Method
4. Virtual Qualification of Power Components and Modules - Development of Innovative Qualification Methods
5. Thermal Management Solutions for Low Volume Complex Electronic Systems (LVCES) - Thermal Management for Reliability
6. Radiation Induced Failure Mechanisms and Preventive Shielding of Electronic Parts - Radiation Hardness Assurance

Future Events:

The next bi-annual CALCE Consortium Technical Review and Planning Meetings will be held in March 2002. An agency-wide subscription for CALCE Consortium Membership for all NASA Centers in is process of implementation. Additional details about CALCE activities and projects are available

at http://www.calce.umd.edu

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2001 Microelectronics Reliability and Qualification Workshop

Pasadena, California
December 11 - 12, 2001

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The 4th annual Microelectronics Reliability and Qualification Workshop will be held December 11-12, 2001 at the Hilton in Pasadena, California. The purpose of the workshop is to provide a forum for open discussion in all areas of microelectronics reliability and qualification for high reliability and commercial applications. This year the format will consists of 8 main technical sessions with two keynote speakers each day. Expert invited speakers will cover the latest results or work in progress, in all areas of microelectronics device reliability and qualification methodologies including:

- Advanced Memories
- MEMS Reliability
- FPGAs Reliability and Qualification
- Advanced Technologies Reliability
- Qualification Methods
- COTS/PEMS Screening and Qualification
- DC/DC Converter Reliability
- Space Radiation Effects

This link will provide you with registration and general information on the 2001 Microelectronics Reliability and QualificationWorkshop.

View the article in PDF.

Articles Are Still Being Accepted For The "December 2001" Issue Of

EEE LINKS

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Guidelines for EEE Links Article Submission

EEE Links is a quarterly publication. The next publication focus will be:

Chip Technology

Submitting articles for EEE Links is a great means by which information and knowledge can be transferred inside and outside of the NASA community.

EEE Links support the NASA Electronic Parts and Packaging (NEPP) Program. The EEE Links Newsletter information will augment the electronic parts, packaging, and radiation technologies.

EEE Links publishes many types of articles that relate to Electronic Parts, Packaging, and Radiation. First consideration goes to articles that deal specifically with the NEPP program. We also consider articles outside of the NEPP program, but related to electronic parts, packaging, or radiation.

The submitted articles can be on current efforts referencing status and completion date. Articles can be informal and from one paragraph to three pages in length on the following subjects:

- Current Events within the NEPP Program and Projects
- Parts
- Packaging
- Radiation
- Reliability Issues Concerning NEPP
- New / Emerging Technology
- Space Flight Hardware
- Quality Assurance Issues

To submit an article, please send it in a text-only format, preferably Microsoft Word, to Nancy Ford at nford@qssmeds.com. Please provide a copy of the Article Submission Checklist, found on the NEPP website. Provide the following information with your article submission:

Abstract - This two- to four-sentence paragraph summarizes the key points to capture the readers attention.

Contact Information - The author must include his or her business address, phone, fax, and email address.

Notes and References - Most articles require some references, and some contain incidental information best treated as notes. Use brackets for references and superscripts for notes, then list the two groups separately at the end of the article. These should be numbered in the order they appear in the article, not alphabetically.

Additional Reading - Our readers appreciate pointers to relevant books and articles. List these at the end of the article in the same format as references.

The author is responsible for obtaining any copyright releases or other releases necessary for their article. The releases should be forwarded to the EEE Links Editor.

Letters to the Editor

Limit letters to 250 words. Include your name, phone number, and e-mail address. Names are withheld from publication upon request. We reserve the right to edit for style, length, and content.

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