

# Heavy Ion Test Results for Electronic Devices

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## Abstract

This paper presents the heavy ion test results for electronic components. Device types include SRAMs, PALs, ADCs, I/O devices, microprocessors, et al... Testing was performed at the Brookhaven National Laboratory's Single Event Upset Test Facility (SEUTF).

## INTRODUCTION

The objective of this study was to determine the Linear Energy Transfer (LET) threshold (as recommended in Ref. [1]) as the minimum LET value to cause an effect at a fluence of  $1E7$  particles/cm<sup>2</sup> and saturation cross section [1] of candidate spacecraft electronics for Single Event Upset (SEU) and latchup (SEL) due to heavy ions. The parts are as shown in Table 1.

Table 1 Summary of Devices Tested

PART NUMBER	MANUFACTURER	FUNCTION	PROCESS	COMMENT
RS Encoder	UTMC/NASA VLSI Design Center	Data and Command Encoding	Bulk CMOS/EPI	New part on rad hard process
UT71256	UTMC	32Kx8 SRAM	Bulk CMOS/EPI w/cross coupled resistors	Samples with two different resistor values
Hot Rod	Gazelle	High-speed Comm. Transmit and Receive pair	GaAs	SEL only
22V10	Cypress	PAL	CMOS, CMOS, and BiCMOS	Three types: Bulk CMOS, CMOS EPROM, BiCMOS
Alpha	Digital Equipment Corporation	64-bit Microprocessor	CMOS	SEL only
TAXI	AMD	High-speed Comm. Transmit and Receive Pair	CMOS, ECL, Bipolar	SEL only

7202RE	IDT	FIFO	CMOS	Radiation Enhanced process
HM628512	Hitachi	4 Mbit SRAM	Hi-CMOS/EPI	-
CS5327	Crystal Semiconductor	Dual 16-bit ADC	CMOS	-
EMXO	Ball Efatrom	Temp. Controlled Precision Oscillator	Hybrid Circuit	-

## TEST TECHNIQUES AND SETUP --- FACILITY USAGE

The test facility used was the Brookhaven National Laboratories (BNL) Single Event Upset Test Facility (SEUTF). The SEUTF utilizes a tandem Tandem Van De Graaff accelerator suitable for providing various ions and energies. Test boards containing the device under test (DUT) are mounted inside a vacuum chamber.

The SEUTF provides a computer-driven monitor and control program for the ion beam and the test board setup as well as a user friendly interface for running experiments via an IEEE488 interface with the experimenter's test computer (also used to interface with the DUT test board for data collection).

Ions used are listed below. Intermediate LETs were obtained by changing the angle of incidence of the DUT to the ion beam, thus changing the path length of the ion through the DUT [\[2\]](#).

ION	ENERGY in MeV	LET at Normal Incidence in MeV*cm/mg
C-12	98	1.45
F-19	140	3.45
Cl-35	211	11.5
Ni-58	263	26.7
I-127	320	59.7
Au-197	341	81.9

Energies and LETs are nominal due to slight variances in the beam at multiple test dates during the calendar year.

## TEST METHOD

Three modes of testing are typically used depending on the DUT. They are as follows:

*static* - load device prior to beam irradiation, then retrieve data post-test run counting errors (either transients or bit flips),

*dynamic* - actively exercise a DUT during beam exposure while counting errors, and for SEL only,

*biased* - DUT is biased and clocked while lcc (power consumption) is monitored for SEL conditions.

## TEST RESULTS AND DISCUSSION

Presented herein are the tabular and graphic results (LET vs. cross-section) obtained during the heavy ion experimentation. Table 2 is a summary of the results. Individual DUTs are discussed in more detail. All results were obtained at room temperature. All units for LET values are in MeV\*cm/mg.

Table 2 Summary of Test Results

PART NUMBER	SEU LET <sub>th</sub> in MeV*cm <sup>2</sup> /mg	Sat. Cross-section in cm <sup>2</sup>	SEL LET <sub>th</sub> in MeV*cm <sup>2</sup> /mg
RS Encoder	38	6.5E-4/device	> 120
UT71256	> 80	< 3.1E-12/bit	> 120
Hot Rod	NA	NA	> 120

22V10D-15 (CMOS)	NA	NA	<< 26
22V10B-15 (CMOS EPROM)	NA	NA	<< 26
22V10C-10 (BiCMOS)	> 120	< 1E-7/device	> 120
Alpha	NA	NA	< 3.35
TAXI	NA	NA	> 50
7202RE	3.5	4.24E-3/device	38-40
HM628512	< 1.5	3.0E-7/bit	> 90
CS5327	< 3.5	NA	> 40
EMXO	> 85	NA	> 85

## RS Encoder

The Reed Solomon (RS) Encoder is a custom IC designed by NASA Space Engineering Research Center (SERC) fabricated on UTM's radiation hardened Bulk CMOS/EPI process. An RS code is a powerful symbol error correcting code useful in obtaining data through a burst error channel. Potential applications include communication and digital data and command systems.

Essentially, a full set of test vectors were sent from a pattern generator to the test board. Power supply current was monitored to check for a SEL condition. The test circuitry detected the existence of errors. These error signals are then tallied by an external counter. A Built-in-Test (BIT) function is included in the test circuit for system verification. The test circuitry ran at 1.0 Mhz with a 5.0V power supply.

The RS Encoder tested well. [Figure 1](#) is a log-linear graph of the raw data for two device samples. [Figure 2](#) is the linear-linear plot of the same data. The SEU LET<sub>th</sub> is approximately 38 the LET<sub>0.1</sub> is ~58). [Figure 2](#) shows that a saturation device cross-section is not reached. The maximum device cross-section (@ LET = 120) is 6.5E-4 cm<sup>2</sup>.

## UT71256

The UTM UT71256 is a 32Kx8 Static RAM (SRAM) device. This device is a candidate for spacecraft computer program memory and critical data storage. This DUT is built on a bulk 1.2 micron CMOS/EPI using cross-coupled resistors to enhance SEU performance. Two sample wafer lots with differing resistor values were tested. A static test using alternating 1/0 test pattern was performed on this device. Test circuitry nominally ran at 1.3 Mhz at a test voltage of 5.0V.

Both wafer lots tested well. No SEUs were seen up to a LET of 81.9. Sporadic SEUs were seen on six runs (LETs between 81.9 and 120) and mixed between lots, but repeatability of the SEUs was impossible. A noisy ground line on the test set was determined to be the cause of these SEUs. To be conservative, however, the SEU LET<sub>th</sub> is > 80 with a device cross-section of < 3.1E-12 cm<sup>2</sup> per bit. No SEL was seen on any test run up to a LET of 120.

## Hot Rod

The Gazelle Hot Rod chipset consists of two GaAs ICs: a transmitter and a receiver. These devices modulate and format data transfers for potential high speed (> 100 megabits per second) spacecraft instrument or communication applications.

SEL test only was performed. No signs of SEL were seen up to the maximum tested LET value of 120.

## 22V10

Three device type samples of 22V10 Programmable Array Logic (PAL) devices from Cypress Semiconductor were irradiated. Tests were conducted dynamically.

Two device types, PALC22V10B-15DDB (CMOS w/ internal EPROM) and PALC22V10D-15DDB (CMOS), latched up at the initial LET offering of 26.4 as soon as the beam was placed on these devices. After power resetting the devices, permanent errors were discovered in both types (this is akin to SEUs causing reprogramming of the devices). SEL LET<sub>th</sub> is << 26. The SEU threshold is presumed to be even lower. Based on the initial result, no further tests were performed on these samples.

The PALC22V10C-10 performed much differently. This is a BiCMOS (Bipolar and CMOS) process device. This device exhibited no sign of SEL or SEUs up to LET values of 120 with a fluence of 1E7 particles per cm<sup>2</sup>.

## Alpha

The Alpha is a 64-bit Reduced Instruction Set Computer (RISC) processor from Digital Equipment Corporation fabricated on a 0.75 micron CMOS process. The device was biased, clocked at 50 MHz, and tested for SEL only. SEL was seen at all tested LET values (3.35 to 11.4). SEL LET<sub>th</sub> is < 3.35 with a device cross-section (at LET = 11.4) of > 5E-4 cm<sup>2</sup> per device.

## TAXI

The Advanced Micro Devices AM7968 TAXIchip Transmitter and AM7969 TAXIchip Receiver Chipset is a general-purpose interface for very high-speed (up to 175 Mbaud serially) point-to-point communications via coaxial or fiber optic media. Both DUTs have TTL and Analog logic sections while the Transmitter has an ECL Serial I/O section.

The DUTs were placed on a test board with power and ground supplied, inputs biased, and a 16 MHz oscillator clocking the DUTs. No signs of latchup were exhibited during any of the test runs. Maximum LET value tested was 50 with a fluence of 1E8 particles per cm<sup>2</sup>. Therefore, either the SEL LET threshold is > 50 or the effective saturation cross section for SEL is < 1E-8 cm<sup>2</sup> per device.

## 7202RE

The Integrated Device Technology (IDT) 7202RE is a 1Kx9 FIFO built on IDT's radiation enhanced CMOS/EPI process. This DUT was tested dynamically with the following results.

1. SEL was seen in all DUTs with LET thresholds varying from 38 to 40 at particle fluences of < 1E6 particles/cm<sup>2</sup>. This is consistent with data reported in Ref. [3].
2. [Figure 3](#) shows the SEU cross-section per bit for all three DUTs versus the tested LET value. The maximum cross-section measured was ~4.24E-3 cm<sup>2</sup> per device at an LET of 34. Cross-sections at higher LET values were unable to be obtained due to the occurrence of SEL. The SEU LET<sub>th</sub> is ~3.5. The SEU LET<sub>0.1</sub> is ~7.5.

Several test runs were performed with test patterns other than a checkerboard with no statistical difference in the data. No significant statistical difference was seen for 0-to-1 versus 1-to-0 SEUs in the data as well.

## HM628512

The Hitachi 4Mbit SRAM is a candidate for usage in spaceflight solid state recorders (SSRs) for flight data storage. For SSRs, data is typically stored during a spacecraft's orbit "scrubbed" with Error Detection and Correction (EDAC) codes then periodically downlinked to the ground. For this utilization, devices need not be error-free since EDAC typically corrects single bit error and detects double bit errors. Only multiple errors in a word is a failed word. This probability for a failed word is what the spacecraft designers need to be concerned with.

Over 130 test runs were performed using a static mode. The following is a summary of the results.

1. No SEL was seen on any test run (maximum LET of 90) during this experiment.
2. [Figures 4](#) and [5](#) show the cross section per bit for all three DUTs versus the test LET value. The maximum (saturation) cross section per bit is ~3E-7 cm<sup>2</sup> (1.25 cm<sup>2</sup>/device). The SEU LET<sub>th</sub> < 1.5. The LET<sub>0.1</sub> is ~5. No statistical difference was seen for 0-to-1 versus 1-to-0 bit flips. Several test runs were performed with test patterns other than a checkerboard (all zeroes) with no statistical difference in the data.

3. Single Hard Errors (SHEs) or "stuck bits" (i.e., bits that were stuck at one value) were seen at LET values of 90, 40, and 26.6 for DUTs 1, 2 and 3, respectively. These were "onesies and twosies" numbers of errors and no cross section was able to be determined.

Hitachi was unable to supply the experimenters with a physical bit map of the device. Therefore, we were unable to determine multiple upsets within the same word from a single ion strike as would be desired for failed word rate analysis as described above.

## **CS5327**

The Crystal Semiconductor CS5327 is a stereo 16-bit Analog- to-Digital Converter (ADC) which utilizes a delta-sigma modulation scheme. This ADC has two die: a 3.0 micron CMOS analog portion, and a 2.0 micron CMOS digital section.

Because of difficulty with noise reducing effective number of bits of the device, as well as problems capturing an accurate number of SEUs we were unable to determine device cross- sections. However, we were able to see SEUs (qualitatively in reconstructed output data) at every test LET value, hence the SEU LET<sub>th</sub> is < 3.5.

No SEL was seen at any tested LET values (maximum LET of 40).

## **EMXO**

The Ball Efatrom EMXO is a hybrid precision temperature controlled oscillator. Power was supplied to the DUT and the frequency monitored to 1 part in a million (i.e., definition for this DUT of an SEU). Power was 5.0V for SEU tests and 5.5V for SEL tests.

Neither SEUs nor SEL was seen on the Ball Efatrom EMXO oscillator at LET values between 3.4 and 85 (MeV\*cm<sup>2</sup>/mg).

## **CONCLUSIONS AND RECOMMENDATIONS**

The devices tested may be conveniently divided into the following categories based solely on SEU and SEL concerns:

1. Recommended for all space missions.
2. Recommended with system design constraints or for non-critical applications.
3. Recommended for SEL concerns but requires further SEU testing.
4. Not recommended for space usage.

Devices in *category 1* include the RS Encoder, UT71256 SRAM, 22VIOC-10 PAL, and EMXO Oscillator. All these devices have SEL and SEU LET<sub>th</sub>s high enough to provide nearly zero probability for SEUs or SEL during extended mission lifetimes.

Devices in *category 2* include HM628512 SRAM and IDT 7202RE FIFO. The HM628512 provides a reasonable solution for mass data storage in a SSR, but definitely requires EDAC schemes to keep the data relatively free of failed words. The 7202RE may be used in a non-critical application that can tolerate SEUs, but only in low earth orbits (LEOs) which are relatively free of higher LET value particles.

*Category 3* devices include the Hot Rod chipset, the TAXI chipset, and the CS5327 ADC. All these devices showed reasonable SEL characteristics, but require full SEU characterization. The Hot Rod is being planned for CY93 by GSFC, while the CS5327 will be tested by Jet Propulsion Laboratories in a joint venture with GSFC.

*Category 4* devices are 22V10B and 22V10D PALs, and the Alpha processor. These devices showed a low SEL LET<sub>th</sub> and are not recommended for usage.

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## **REFERENCES**

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