Heavy Ion Single Event Effects Test Results for Three Candidate 22V10 Reprogrammable Logic Devices

Scott Kniffin[1], Chris Palor[1], and Mike Xapsos[2]

1. NASA/Orbital Sciences Corporation
2. NASA/GSFC

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I. INTRODUCTION

This study was undertaken to determine the radiation-induced single event transient (SET), single event functional interrupt (SEFI) and single event latchup (SEL) sensitivity of three programmable array logic devices. The device specifics are as follows: the Cypress PALCE22V10 is a flash erasable, reprogrammable CMOS PAL device, the Atmel ATF22V10B is a high performance EE programmable logic device (PLD) and the Lattice GAL22V10/883 is a high performance E^2CMOS PLD Generic Array Logic (GAL) device. Heavy ion testing was done at Brookhaven National Laboratory's Single Event Upset Test Facility. The output of the device was monitored for radiation-induced errors.

II. DEVICES TESTED

The 22V10 is a fully reprogrammable 132x44 AND-array, suitable for any number of logic functions. All three devices were configured/programmed identically. Outputs 1-4 count from 1 to 15. Output 5 is a Carry Out, which senses the end of the count to 15, drives the Output Low, then back to High. Output 6 is a Flip-Flop, toggling from 0 to 1 with each clock pulse. Outputs 1-6 are compared to a reference device under test (DUT) (an Atmel device with the identical program loaded) to look for SET. Output 7 is High, Output 8 is Low; both are compared with an exclusive NOR to look for SEL. The Cypress and Atmel devices typically drew about 70-80mA I_{CC} and the Lattice drew about 20mA I_{CC}. This was due to differences in chip architecture. The output of the DUT being irradiated was compared to a reference part (Atmel) to determine the error induced by radiation. There were a total of six DUTs, two from each manufacturer (DUTs C1, C1, A1, A2, L1, and L2). The DUTs were irradiated with several different ions. The devices were delidded before exposure. DUTs C1 and C2 were marked PALC22V10D-10DMB 5962-8984106LA Q712201 THA0134 on the top and 125928 Thailand on the bottom, DUTs A1 and A2 were marked C 9B0127 A 5962-8984106LA ATF22V10B-10GM/883 on top and 9B2398-19423K 1 Philippines-F 9B0127 on the bottom, and DUTs L1 and L2 were marked 5962-8984106LA GAL22V10D-10LD 883ΔΔC D0B0043B on top and 0043 5F36AM1 Philippines on the bottom.

III. TEST FACILITIES

Heavy Ion Test Facility: Brookhaven National Laboratory Single Event Upset Test Facility.
Flux: $8.52 \times 10^3 - 1.14 \times 10^5$ particles/cm^2/s.
Particles: linear energy transfer (LET)

Ion	LET (MeV•cm^2/mg)
O-16	2.57
Si-28	7.88
Cl-35	11.44
Ti-48	18.6
Ni-58	26.69
Br-79	37.43
I-127	59.39

Table 1: List of ions used and their LET at normal incidence.

IV. TEST METHODS

Case Temperature: ambient in a vacuum

Test Hardware: A custom test set was used to supply a nominal input level to the DUTs and monitor the DUT output for changes resulting from the radiation exposure. Each radiation event occurring on the output was captured in a custom error capture software package running on a laptop computer or with the HP5316B Universal Counter. The compare DUT determined if there was a difference in outputs given by the test DUT and the reference DUT, sending the error code to the software. Additionally, the High and Low of the test DUT were checked with an exclusive NOR gate. Upon an error condition, a "1" was sent to the universal counter. An HP6624A power supply provided power to all devices.

Software: Customized LABVIEW® software provided a user interface to control signals to the DUTs. The software also automatically monitored the DUT output and generated an SET/SEL file history.

Test Techniques: Tests were performed on the DUTs to measure the SET/SEL susceptibility as a function of particle LET for the specific application described in this report. Any deviations from the application described should be reviewed carefully. The test setup did not allow for monitoring or changing the temperature, therefore temperature effects were not considered. The power supply was set at +5V with nominal current. The DUTs were driven at 1MHz. The DUTs were programmed as given above and placed on to a test board as shown in Figure 1. The setup allows for continuous monitoring of all parameters by the software.

The device was deemed to have experienced an SET when the output of the Test DUT did not match the output of the Reference DUT as compared by the Compare DUT (See Fig. 1.) or there was a momentary loss of one of the rails as detected by the counter as an occasional single count on the display. The device was deemed to have experienced a SEFI if the counter goes into runaway (the exclusive NOR gate comparing Outputs 7 and 8 give continuous errors) without the device drawing excessive current. The device was deemed to have experienced a SEL if the power supply current exceeded a specified amount, set in the software. The number of deviations during an irradiation was tabulated. The software captured all events.

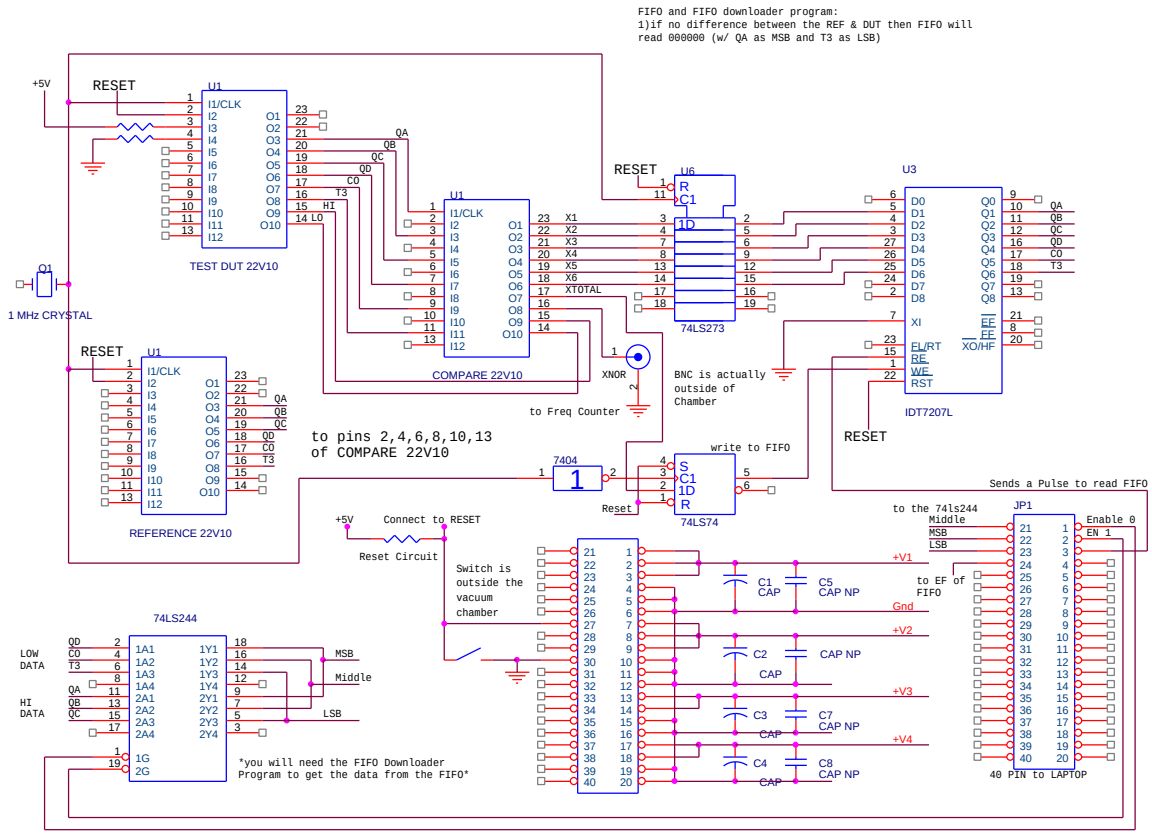

Figure 1: Schematic of 22V10 test circuit.

V. RESULTS

A. Cypress PALCE22V10

The DUTs showed SEFI and one non-destructive SEL at an LET of 7.9 MeV•cm^2/mg (Si-28 at normal incidence). Typically, the SEFI occurred simultaneously with ~110-130 errors from Outputs 1-6 while the counter monitoring the High and Low rail of the device counted literally every clock cycle as one of the rails had failed. Each time the device recovered after a reset. Nominal current was 76mA; during one run, DUT C2 latched and the power supply current went to 110mA and recovered after a reset.

B. Atmel ATF22V10B

The DUTs showed no SEL up to an LET of 84.39 MeV•cm^2/mg (I-127 at 45° from normal incidence). One DUT was also tested at an LET of 84.1 MeV•cm^2/mg (Au-197 at normal incidence) with no SEL. There were a few SET mismatch errors, with the cross section tending to increase slightly with increasing LET (see Fig. 2). The mismatch threshold LET was 13.21 MeV•cm^2/mg (Cl-35 at 30° from normal incidence). Additionally, the software can detect timing errors when they occur separately from other mismatch errors in Outputs 1-6. These timing errors were detected in several runs with timing error threshold LET of 23.02 MeV•cm^2/mg (Cl-35 at 45° from normal incidence) (see Fig. 3). The High/Low comparator also saw an increasing number of SETs with increasing LET, (see Fig. 4) with a comparator threshold LET of 11.44 MeV•cm^2/mg (Cl-35 at normal incidence) (see Fig. 4).

C. Lattice GAL22V10/883

The DUTs showed a non-destructive SEL with an LET threshold of 26.55 MeV•cm^2/mg (Ni-58 at normal incidence). Typical I_{CC} was ~20mA and the SEL took the current to 99-110mA. These events also led to the High/Low rail counter monitor to count all clock cycles as in the case of the Cypress parts. There were very few SET mismatch errors, typically one or two per run. The threshold for mismatch errors was at an LET of 22.88 MeV•cm^2/mg (Cl-35 at 60° from normal incidence). Additionally, timing errors were detected in four runs with the same onset as that of the mismatch errors.

A summary of all effects is given below in Table 2. A complete run log can be provided if needed.

Manufacturer	Mismatch SET	SEFI	SEL	High/Low SETs	Timing Error SETs
Cypress	Occurred with SEFI	$LET_{th} < 7.9$	One at LET of 7.9	Continuous errors with SEFIs or SEL	Some occurred with SEFIs
Atmel	$SET_{th} < 13.21$	None detected	None up to LET of 84.39	$LET_{th} < 11.44$	$LET_{th} < 23.02$
Lattice	$SET_{th} < 22.88$	None detected	$LET_{th} <$ 26.55	Onset at LET of 11.44 but continuous errors with SELs	$LET_{th} < 22.88$

Table 2: Summary of SEE. All numbers given are in MeV•cm^2/mg.

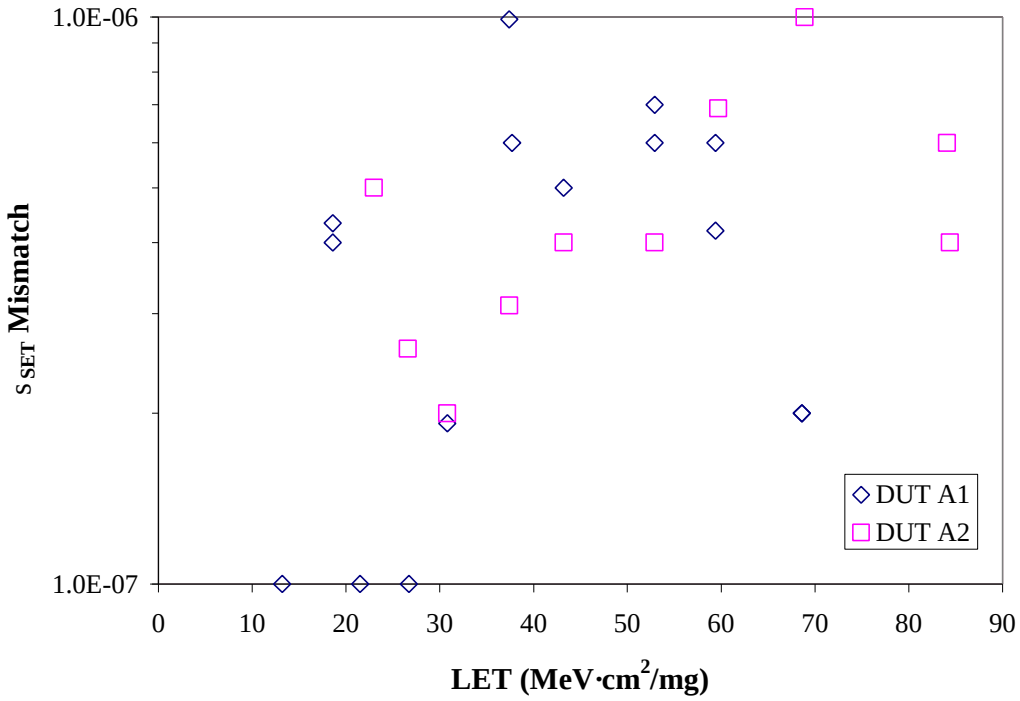

Figure 2: SETs that result from the Atmel test DUT output not matching the reference DUT.

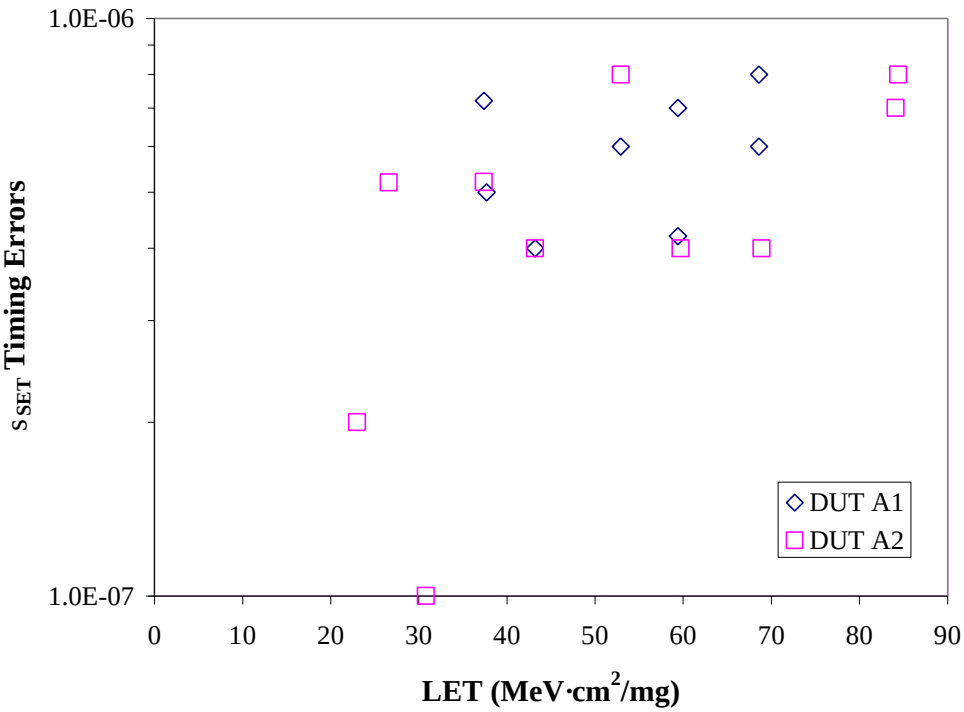

Figure 3: SETs that are single detections of timing glitches within the Atmel test DUT.

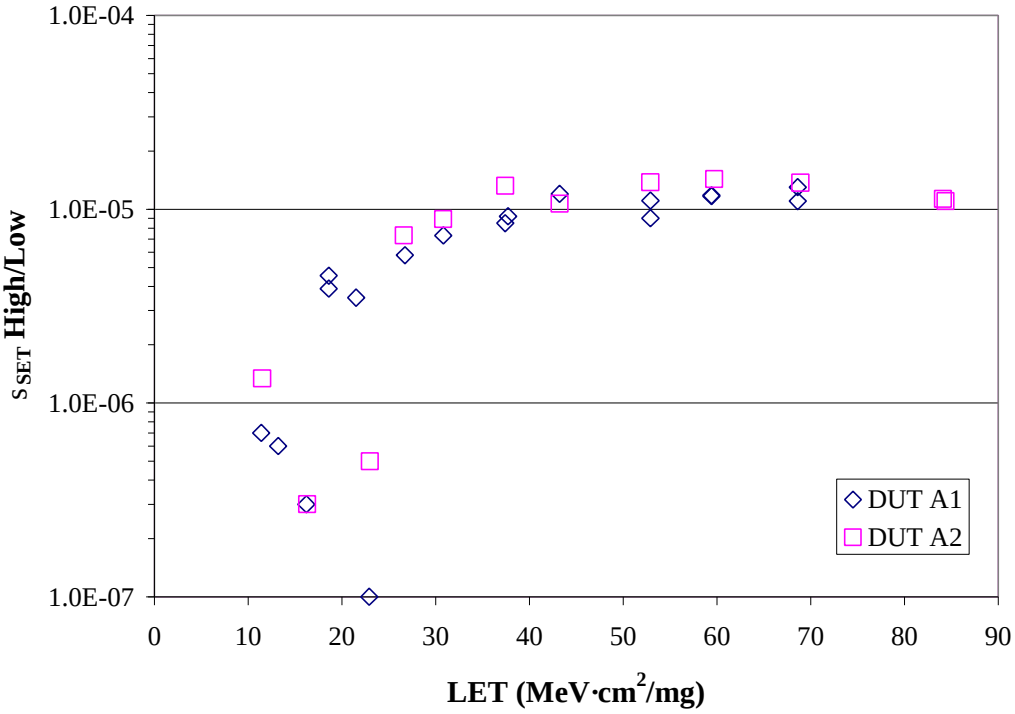

Figure 4: SETs in the output that compares the High and Low rails of the Atmel test DUT.