Effects of via-conductor geometry in the electromigration failure of Al:Cu

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Outline

- Experimental set-up/Background
- Resistance vs. Time
  - Conductor orientation dependence
  - Results without vias
- EBIC imaging
- Activation energy determination
- Cross-sectional images
- Some of the problems, difficulties...
- Summary
Motivation/Purpose

• As device features reduce in Ultra-large-scale integrated circuits, current densities increase with the metallization layer complexity. These issues make understanding Electromigration (EM) induced failure essential to design more reliable circuits.

• EM failure models for Al-Cu metallization at tungsten plug contact/via areas are examined in this work. In particular, we examine changes induced solely by the geometry of the plug/via conductor arrangement.

• Resistance vs. time 4-point probe experiments were performed at various temperatures and current densities; which allowed to uncover effects from geometry alone and to determine activation energies.

• Experiments with these electromigration resistant Al:Cu structures provide a baseline for comparison with planned experiments using Cu ultra-fine conductors and Cu used in SoC micro-inductors.
Experimental details

• Four probe measurements at constant current

• Two via geometries in 2 layer metallization test structures*
  • two structures tested at one time
  • different vias are made to fail by reversing current direction
  • experiments were also performed with no vias

• Test structure is Al:Cu (2% Cu). TiN diffusion barrier(s) - SiO₂ and Silicon Nitride passivation layers - Tungsten plugs - Conductor critical dimensions: 0.67 microns deep by 0.67 microns wide - Bamboo structure (grain sizes ~ 1 micron)

• Resistance is measured and acquired digitally every 30 minutes

• Measurements at four (4) temperatures: 180, 200, 220 and 240° C

• Currents used are 8, 10, and 20 mA (corresponding to current densities of 1.6 x 10⁶, 2 x 10⁶ and 4 x 10⁶ Amps/cm²).
  • R vs. T at low currents was measured to detect possible Joule heating at high current densities.

• Measurements were performed in air and at 1 atmosphere

• EBIC (Electron Beam Induced Conductivity) to isolate failure sites was performed at 10 KeV

*Fabricated at IDT (Integrated Device Technology, Inc.)
Test structure for Al:Cu electromigration experiment(s)
Parallel or co-linear geometry

Aluminum:Cu line

Perpendicular geometry

Cathode $e^-$

Cathode $e^-$
Joule heating measurements for Al:Cu test structures:

Measurements performed as structures are heated at very low current densities (current of 0.05 mA) show Joule heating of 0.05 ohms/degree C. Current density is then increased to test stress current (20 or 10 mA). No significant increase in resistance is observed at beginning of measurement.
Co-linear or parallel conductor geometry shows well defined “steps in the Resistance vs. time curves

Proposed mechanism to explain “steps” in co-linear geometry. Progressive void formation at each plug/conductor interface could explain measured resistance data, where each step increase in resistance happens upon void formation at each different plug/conductor interface.
Dramatic differences in degradation seen in tests with and without vias (1 and 2 layer metallization)

This observation can be explained by the absence of flux divergence in the no-via 1-metal layer structure.

Previous studies have shown that the interface between the Al conductor and the refractory metal (W plug) is most vulnerable to voiding. This is due to the discontinuity in the flux of electromigrating Al atoms.

The rate of void formation is controlled by the Al drift velocity:

\[ V_d = \frac{D_i}{kT} eZ_i^* \rho j \]

where: \( D_i \) is the diffusion coefficient of Aluminum, \( j \) is the current density, \( \rho \) is the resistivity (of Al), and \( eZ_i^* \) is the effective electromigration charge.
EBIC has shown to be a very useful tool to identify point of failure. Image shows EBIC contrast when there are no open conductors.

Failure point cannot be seen in plan-view (top) standard SEM imaging even for an open circuit failure after electromigration testing.
EBIC analysis of open circuit structure after electromigration testing at 220°C

Connections were reversed to ensure that failure is only at one of the two vias
Fit with Black’s equation,

$$t = A j^{-n} e^{Ea/kT}$$

$t$ is time to reach failure (20% degradation)

$j$ is current density

$Ea$ is activation energy (in eV)

$k$ is Boltzmann’s constant

$T$ is temperature

Similar activation energies were obtained for the perpendicular and co-linear geometries, however, our measurements show that perpendicular vias have a higher probability of failing sooner. This is reflected in a different (smaller) pre-exponential factor in the Arrhenius curve.
Cross sectional SEM image of a “good” structure prior to EM testing, which shows one of the Tungsten plugs.
Cross-sectional SEM image of voided area at Tungsten/Al:Cu interface. Void was formed from electromigration testing at 240 C and structure failed catastrophically (open circuit).
Summary of data for Al:Cu electromigration experiments – black and blue indicates measurement done in pairs. R1 is connected so perpendicular via fails, R2 is connected to fail with parallel via.

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Via failure = or ⊥</th>
<th>Current (mA)</th>
<th>Current density (A/cm²)</th>
<th>T (C)</th>
<th>Initial R at test T (Ω)</th>
<th>Time to degrade 10% (h)</th>
<th>Time to degrade 20% (h)</th>
<th>Time 100% failure (open) (h)</th>
<th>Comments</th>
<th>Failure mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>43 (Greg)</td>
<td>R to L</td>
<td>8</td>
<td>1.6 x 106</td>
<td>220</td>
<td>22.2</td>
<td>65 h</td>
<td>80 h</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>117 (Greg)</td>
<td>L to R</td>
<td>8</td>
<td></td>
<td>220</td>
<td>21.9</td>
<td>&gt; 90 h</td>
<td>&gt; 90 h</td>
<td></td>
<td>Some degrad.</td>
<td></td>
</tr>
<tr>
<td>150</td>
<td>L to R</td>
<td>10</td>
<td>2 x 106</td>
<td>220</td>
<td>24</td>
<td>34 h</td>
<td>35 h</td>
<td>In Series</td>
<td></td>
<td></td>
</tr>
<tr>
<td>117</td>
<td>L to R</td>
<td>10</td>
<td></td>
<td>220</td>
<td>23</td>
<td>&gt; 70 h</td>
<td>&gt; 70 h</td>
<td>No degrad.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>92</td>
<td>none</td>
<td>20</td>
<td>4 x 106</td>
<td>220</td>
<td>21.5</td>
<td>&gt; 500 h</td>
<td>&gt; 500 h</td>
<td>No R change</td>
<td>No via</td>
<td>ESD zapped</td>
</tr>
<tr>
<td>131</td>
<td>none</td>
<td>20</td>
<td></td>
<td>220</td>
<td>21.6</td>
<td>&gt; 500 h</td>
<td>&gt; 500 h</td>
<td>No R increase</td>
<td>No via</td>
<td>ESD zapped</td>
</tr>
<tr>
<td>45 (R1)</td>
<td>⊥</td>
<td>10 and 20</td>
<td>2 and 4</td>
<td>220</td>
<td>23.1</td>
<td>50 h (10mA)</td>
<td>58 h</td>
<td>315 h (EBIC (Ron))</td>
<td>Via failure</td>
<td></td>
</tr>
<tr>
<td>58 (R2)</td>
<td>=</td>
<td>10 and 20</td>
<td>X 106</td>
<td>220</td>
<td>22.7</td>
<td>80 h (10mA)</td>
<td>85 h</td>
<td>362 h (Via open)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14 (R1)</td>
<td>⊥</td>
<td>20</td>
<td>4 x 106</td>
<td>220</td>
<td>24.8</td>
<td>63 h</td>
<td>65 h</td>
<td>127 h (In ESD bag)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>141 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>220</td>
<td>24.4</td>
<td>105 h</td>
<td>117 h</td>
<td>189 h (In ESD bag)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>33 (R1)</td>
<td>⊥</td>
<td>20</td>
<td></td>
<td>240</td>
<td>25.1</td>
<td>8.5 h</td>
<td>17.5</td>
<td>37.5 h (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>150 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>240</td>
<td>26.4</td>
<td>23.5 h</td>
<td>44.5 h</td>
<td>57.5 h (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>31 (R1)</td>
<td>⊥</td>
<td>20</td>
<td></td>
<td>200</td>
<td>23.7</td>
<td>105.5 h</td>
<td>222 h</td>
<td>347 h (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>297 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>200</td>
<td>23.8</td>
<td>28 h</td>
<td>162 h</td>
<td>290 h (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>180 (R1)</td>
<td>⊥</td>
<td>20</td>
<td></td>
<td>180</td>
<td>23.2</td>
<td>43 h</td>
<td>403 h</td>
<td>663 h (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>185 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>180</td>
<td>22.7</td>
<td>290 h</td>
<td>497 h</td>
<td>773 h (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>6 (R1)</td>
<td>⊥</td>
<td>20</td>
<td></td>
<td>240</td>
<td>25.3</td>
<td>12.7 h</td>
<td>16 h</td>
<td>47 (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>35 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>240</td>
<td>25.1</td>
<td>6.4 h</td>
<td>10.6 h</td>
<td>18.9 h (In ESD box)</td>
<td>Via open</td>
<td></td>
</tr>
<tr>
<td>95 (R1)</td>
<td>⊥</td>
<td>20</td>
<td></td>
<td>200</td>
<td>24.5</td>
<td>14.4 h</td>
<td>14.4 h</td>
<td>377 h (In ESD box)</td>
<td>Both to 35 Ohms</td>
<td></td>
</tr>
<tr>
<td>283 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>200</td>
<td>23.5</td>
<td>70 h</td>
<td>70 h</td>
<td>256 h (In ESD box)</td>
<td>(not open)</td>
<td></td>
</tr>
<tr>
<td>63 (R1)</td>
<td>⊥</td>
<td>20</td>
<td></td>
<td>220</td>
<td>24.0</td>
<td>10 h</td>
<td>58 h</td>
<td>161 h (In ESD bag)</td>
<td>Open circuit</td>
<td></td>
</tr>
<tr>
<td>326 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>220</td>
<td>24.7</td>
<td>31 h</td>
<td>74 h</td>
<td>108 h (In ESD box)</td>
<td>Open circuit</td>
<td></td>
</tr>
<tr>
<td>262 (R1)</td>
<td>⊥</td>
<td>20</td>
<td></td>
<td>220</td>
<td>24.3</td>
<td>15.7</td>
<td>44.5</td>
<td>103 (In ESD box)</td>
<td>40 ohms</td>
<td></td>
</tr>
<tr>
<td>284 (R2)</td>
<td>=</td>
<td>20</td>
<td></td>
<td>220</td>
<td>24.2</td>
<td>10</td>
<td>57</td>
<td>103.5 (In ESD box)</td>
<td>40 ohms</td>
<td></td>
</tr>
<tr>
<td>44 (R1)</td>
<td>⊥</td>
<td>10</td>
<td>2 x 106</td>
<td>240</td>
<td>24.7</td>
<td>29</td>
<td>222</td>
<td>325 (In ESD box)</td>
<td>open</td>
<td></td>
</tr>
<tr>
<td>158 (R2)</td>
<td>=</td>
<td>10</td>
<td></td>
<td>240</td>
<td>25.3</td>
<td>32</td>
<td>179</td>
<td>313 (In ESD box)</td>
<td>open</td>
<td></td>
</tr>
</tbody>
</table>
Problems (1): High ESD (electrostatic discharge) sensitivity. Damage often seen in dry winter days.

Solution:

1. Use appropriate ESD precautions during test structure handling (according to the JPL Standard procedures for handling ESD sensitive samples).

2. Store structures in ESD bags or boxes in between tests or after testing and prior to cross-sectioning.
Problem (2): Ultrahigh current densities in thinning areas can cause arcing with localized melting of metals and partial structure “repair”. This is undesirable for cross-sectional studies since this process might mask “real” (meaning electromigration induced) degradation mechanism.

Curve for R1 (red) shows a case of localized metallization “self-repair” due to melting of metals at ultra-high current densities after Al conductor thinning due to electromigration induced voiding.

Test can be stopped earlier, before circuit is completely open.
Summary of observations

• We find sharp steps in the Resistance vs. time curves (for the co-linear geometry).

• Times to failure (or 20% degradation) have the expected Arrhenius dependence.

• Activation energies obtained from Arrhenius plots are 1 eV - high for Al conductors.

• EBIC (electron beam induced conductivity) is a useful technique to locate failure, but it works best if line is open.

• Perpendicular geometry is more likely to fail earlier than structures with co-linear (parallel) geometry (as seen in 8 out of 10 test pairs).

• Failure is due to void formation at the Al:Cu/W interface near cathode.