Effects of via-conductor geometry in the electromigration failure of Al:Cu

R. Leon, D. Vu, A.S. Johnson, R. Ruiz, J. Okuno, J. Uribe, and G. Hather
Jet Propulsion Laboratory, California Institute of Technology, 4800 Oak Grove Drive, Pasadena, CA 91109

J. R. Lloyd
IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, NY 10598

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

JPL

Outline

- Experimental set-up/Background
- Resistance vs. Time
  - Conductor orientation dependence
  - Results without vias
- EBIC imaging
- Activation energy determination
- Cross-sectional images
- Some of the problems, difficulties...
- Summary

Motivation/Purpose

•As device features reduce in Ultra-large-scale integrated circuits, current densities increase with the metallization layer complexity. These issues make understanding Electromigration (EM) induced failure essential to design more reliable circuits.

•EM failure models for Al-Cu metallization at tungsten plug contact/via areas are examined in this work. In particular, we examine changes induced solely by the geometry of the plug/via conductor arrangement.

•Resistance vs. time 4-point probe experiments were performed at various temperatures and current densities; which allowed to uncover effects from geometry alone and to determine activation energies.

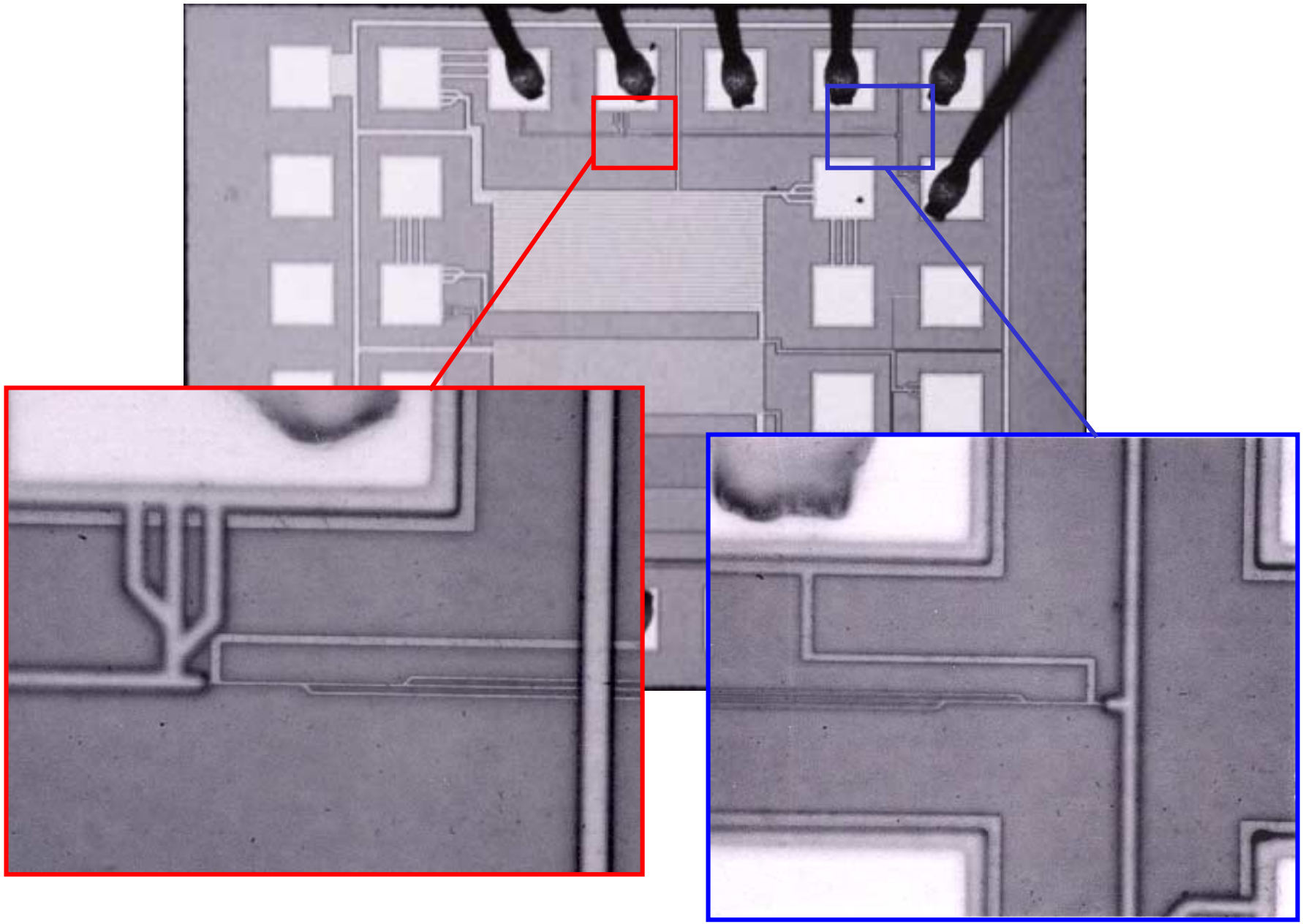
•Experiments with these electromigration resistant Al:Cu structures provide a baseline for comparison with planned experiments using Cu ultra-fine conductors and Cu used in SoC micro-inductors.

Experimental details

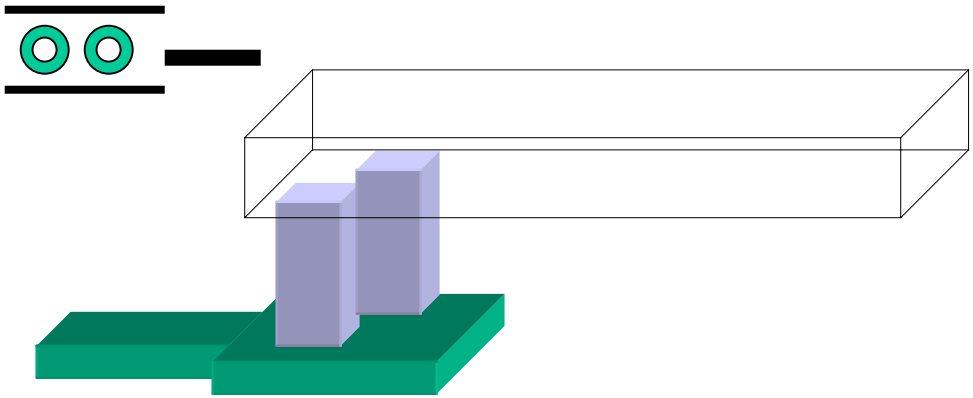
- Four probe measurements at constant current
- Two via geometries in 2 layer metallization test structures*
  - two structures tested at one time
  - different vias are made to fail by reversing current direction
  - experiments were also performed with no vias
- Test structure is Al:Cu (2% Cu). TiN diffusion barrier(s) - SiO_2 and Silicon Nitride passivation layers - Tungsten plugs - Conductor critical dimensions: 0.67 microns deep by 0.67 microns wide - Bamboo structure (grain sizes ~ 1 micron)
- Resistance is measured and acquired digitally every 30 minutes
- Measurements at four (4) temperatures: 180, 200, 220 and 240ºC
- Currents used are 8, 10, and 20 mA (corresponding to current densities of 1.6×10^6, 2×10^6 and 4×10^6 Amps/cm^2).
  - R vs. T at low currents was measured to detect possible Joule heating at high current densities.
- Measurements were performed in air and at 1 atmosphere
- EBIC (Electron Beam Induced Conductivity) to isolate failure sites was performed at 10 KeV

*Fabricated at IDT (Integrated Device Technology, Inc.)

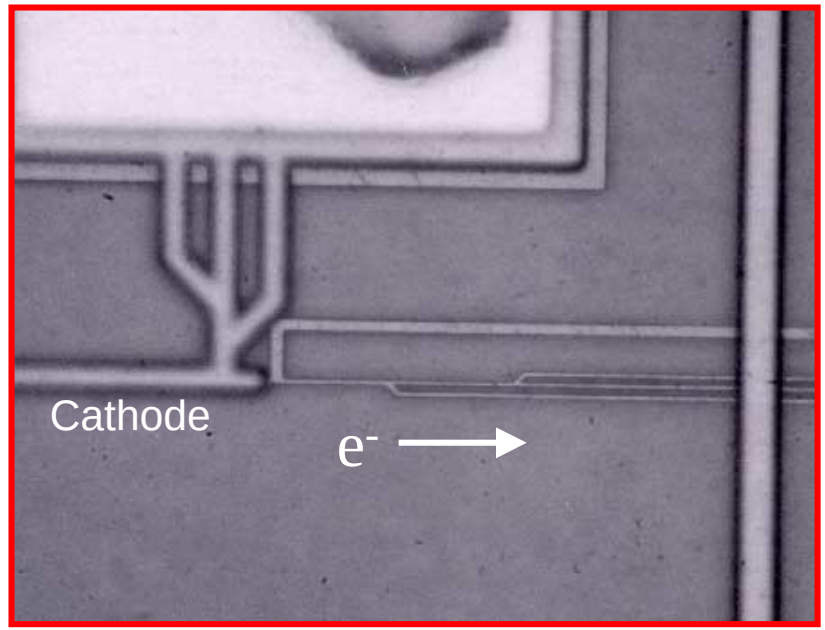
Test structure for Al:Cu electromigration experiment(s)



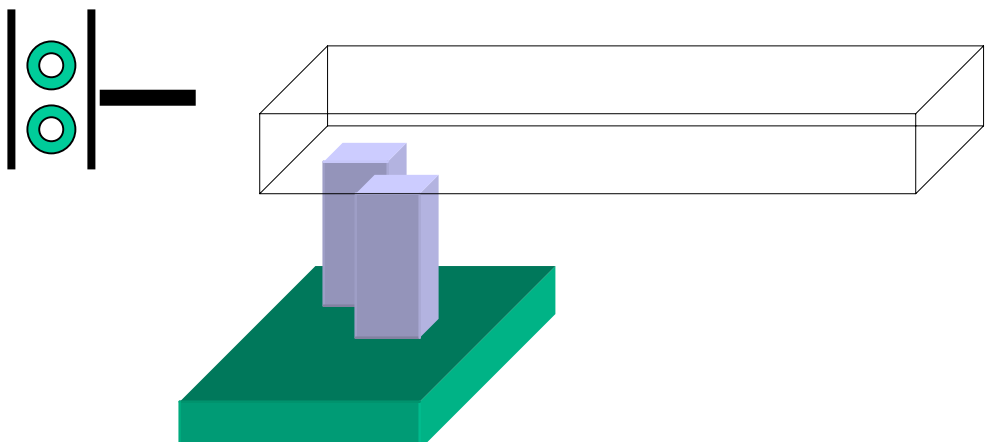
Parallel or co-linear geometry

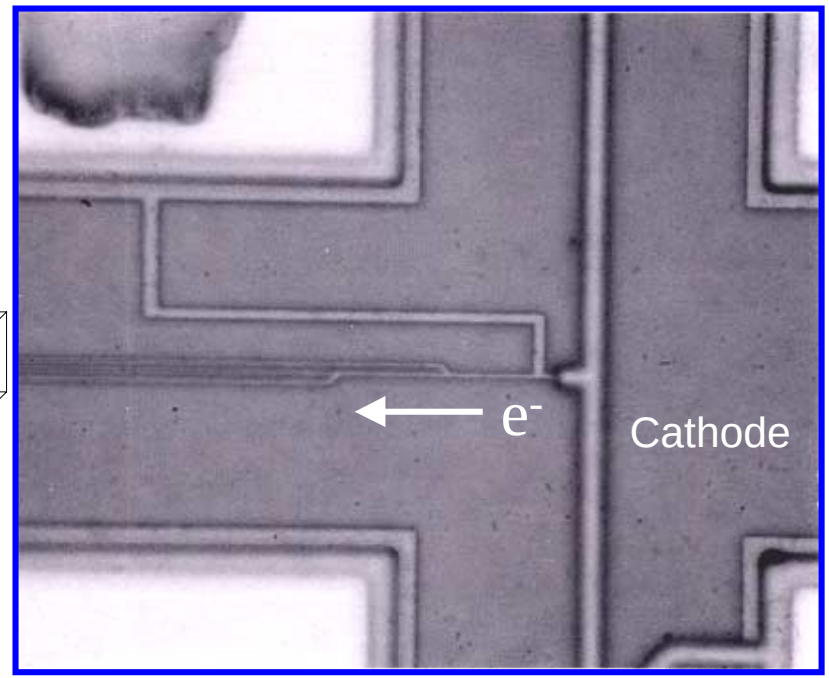


Aluminum:Cu line

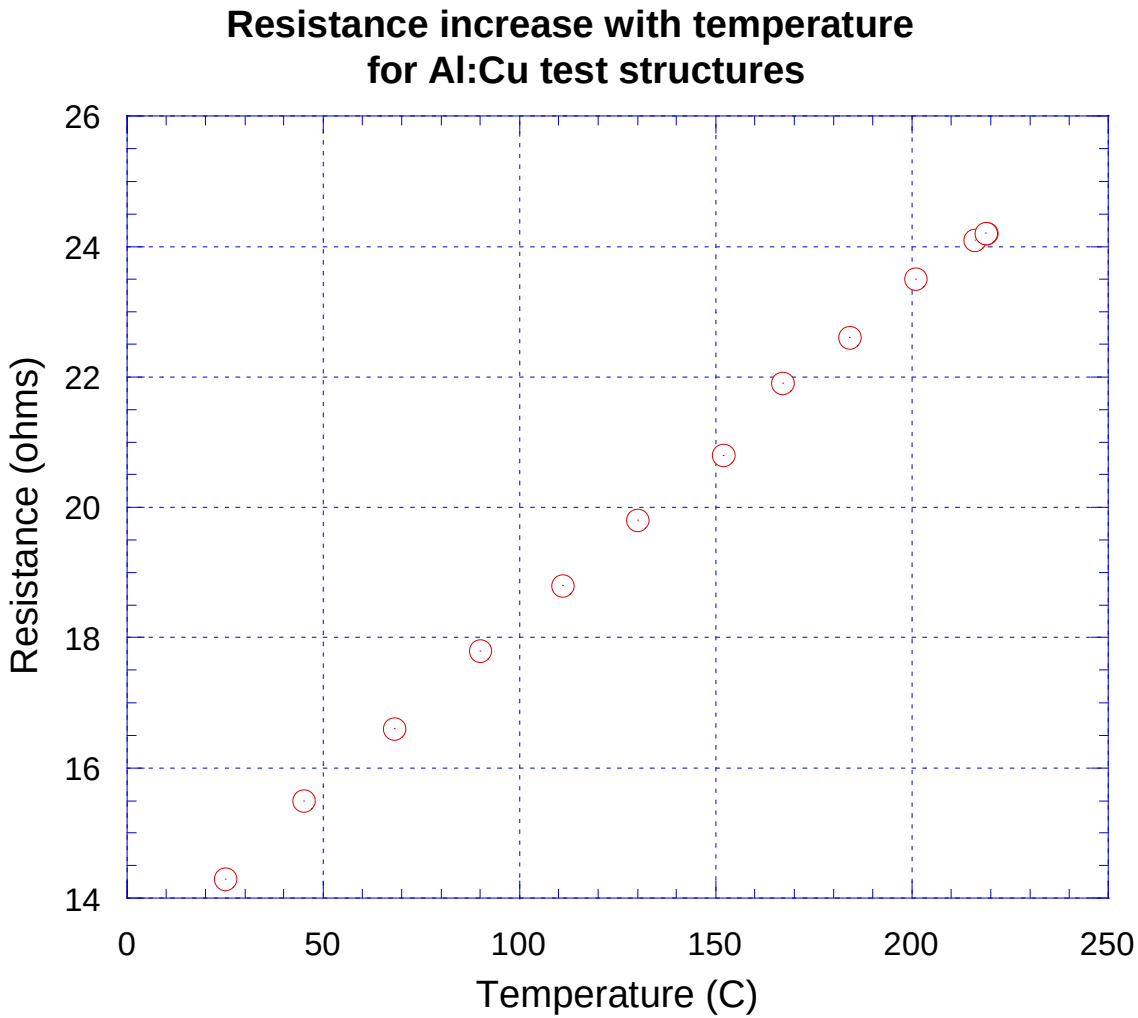


Perpendicular geometry



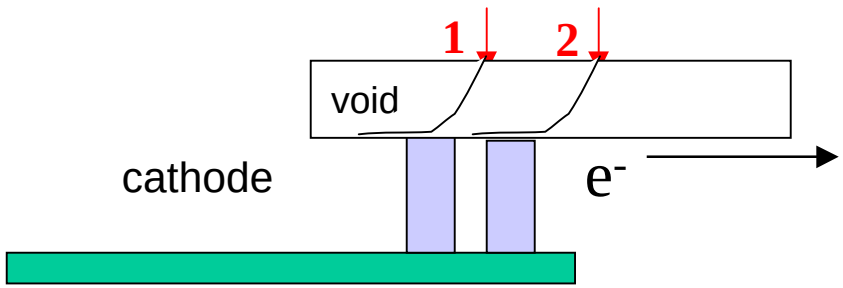


Joule heating measurements for Al:Cu test structures:

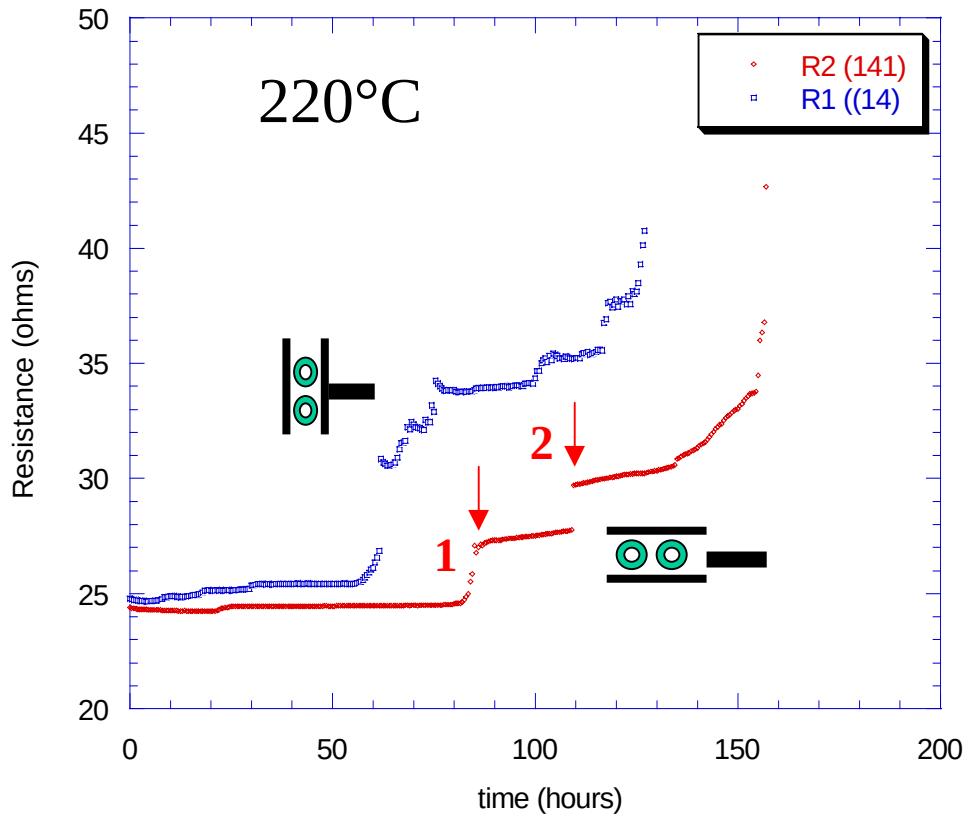


Measurements performed as structures are heated at very low current densities (current of 0.05 mA) show Joule heating of 0.05 ohms /degree C. Current density is then increased to test stress current (20 or 10 mA). No significant increase in resistance is observed at beginning of measurement.

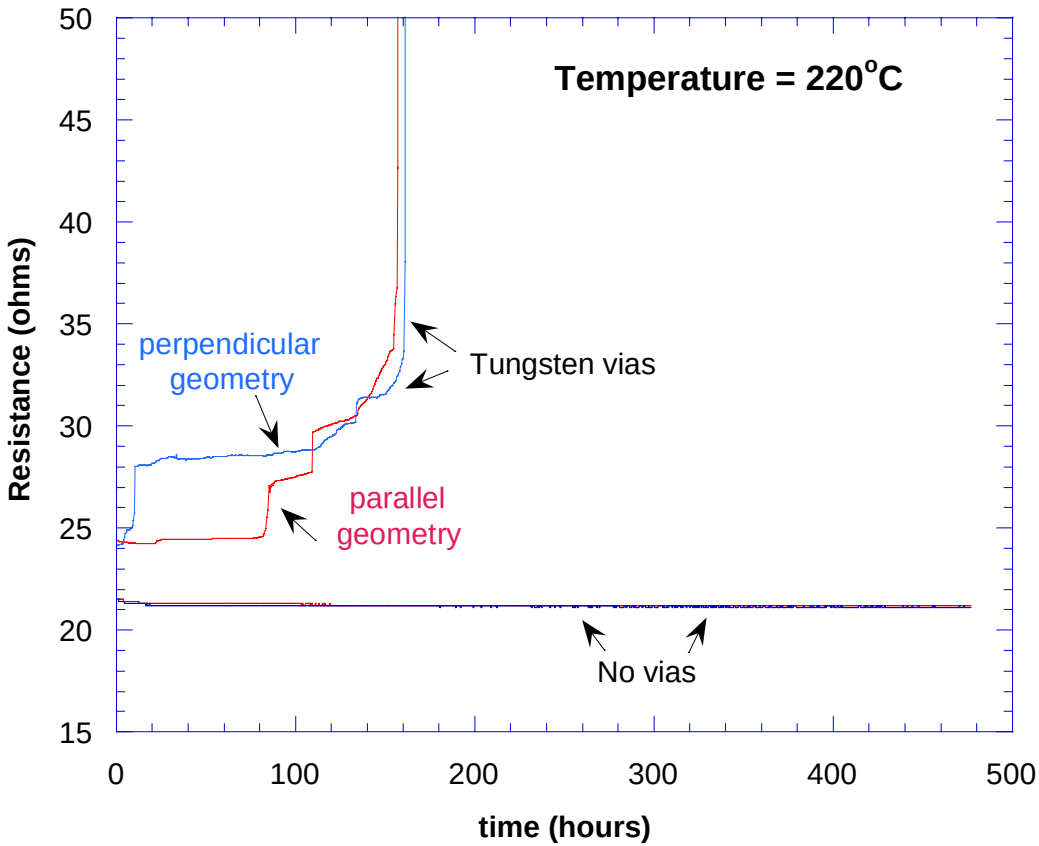
Co-linear or parallel conductor geometry shows well defined “steps in the Resistance vs. time curves



Proposed mechanism to explain “steps” in co-linear geometry. Progressive void formation at each plug/conductor interface could explain measured resistance data, where each step increase in resistance happens upon void formation at each different plug/conductor interface.



Dramatic differences in degradation seen in tests with and without vias (1 and 2 layer metallization)



This observation can be explained by the absence of flux divergence in the no-via 1-metal layer structure. Previous studies have shown that the interface between the Al conductor and the refractory metal (W plug) is most vulnerable to voiding. This is due to the discontinuity in the flux of electromigrating Al atoms.

The rate of void formation is controlled by the Al drift velocity:

$$V_d = D_i/kT\ eZ_i^*\ \rho\ j$$

where: Di is the diffusion coefficient of Aluminum
j is the current density, r is the resistivity (of Al),
and eZi* is the effective electromigration charge

EBIC has shown to be a very useful tool to identify point of failure

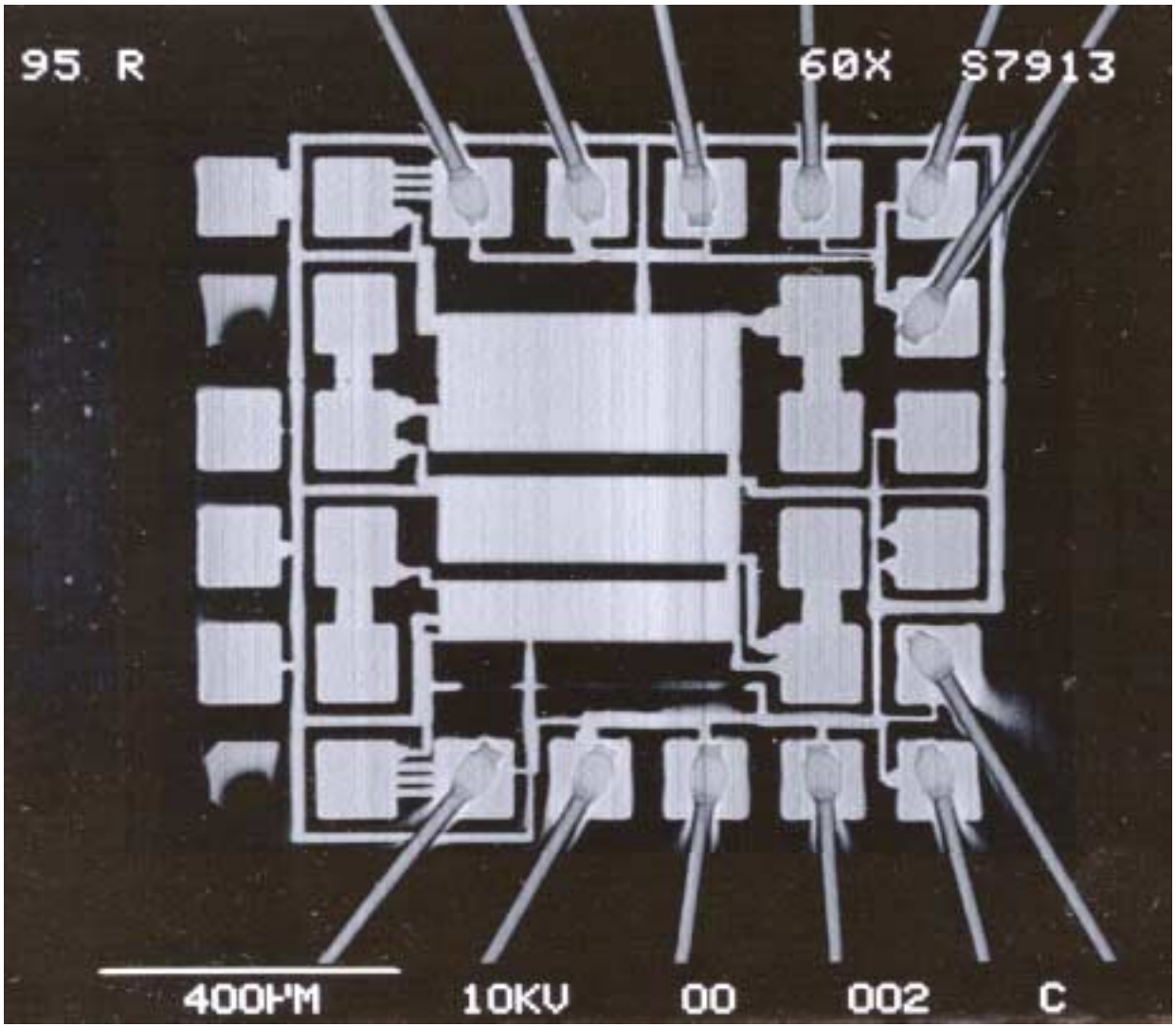
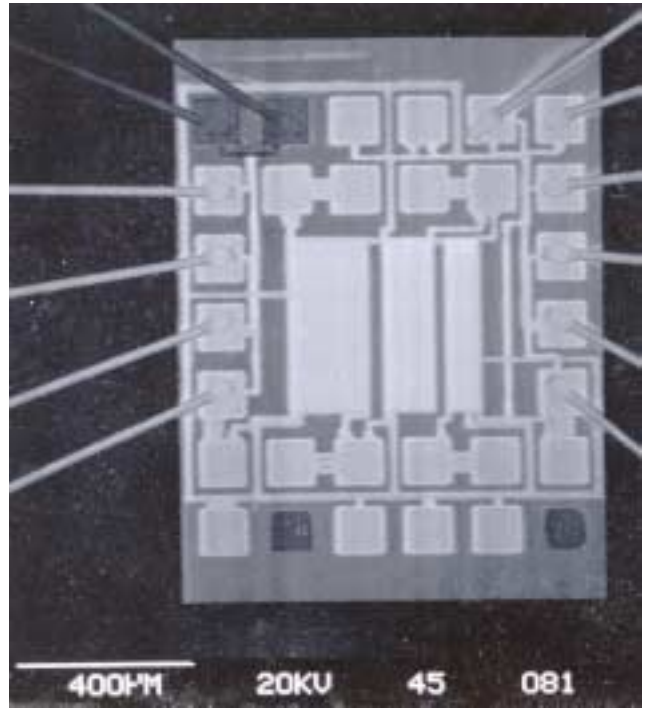
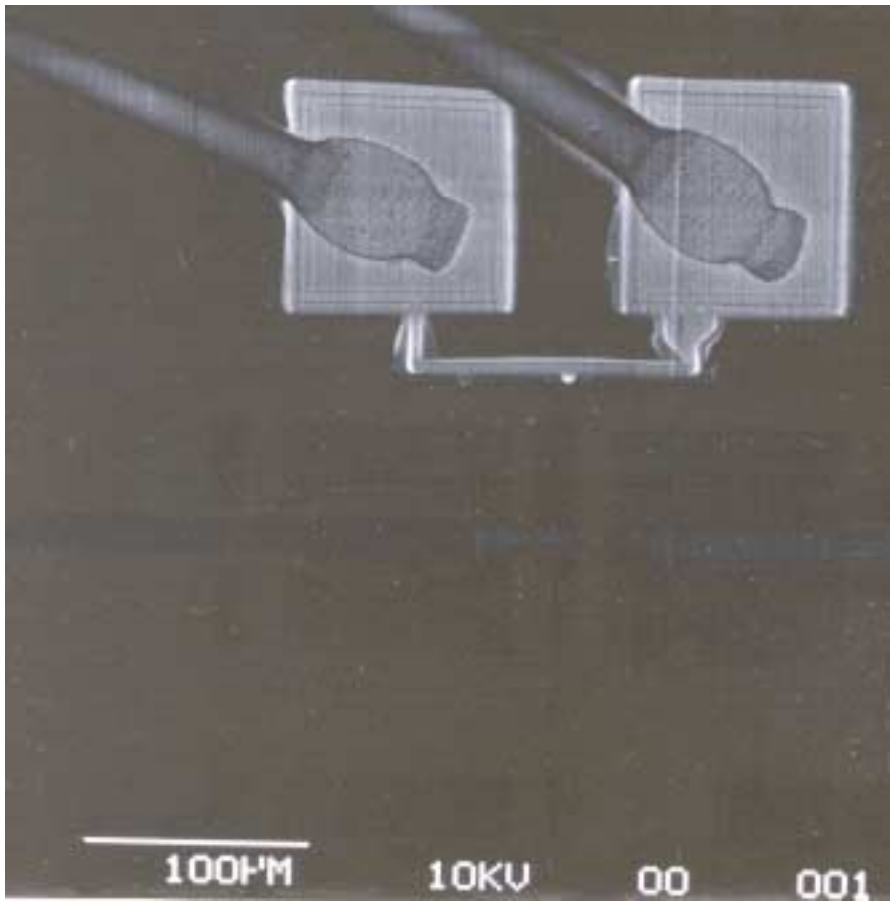


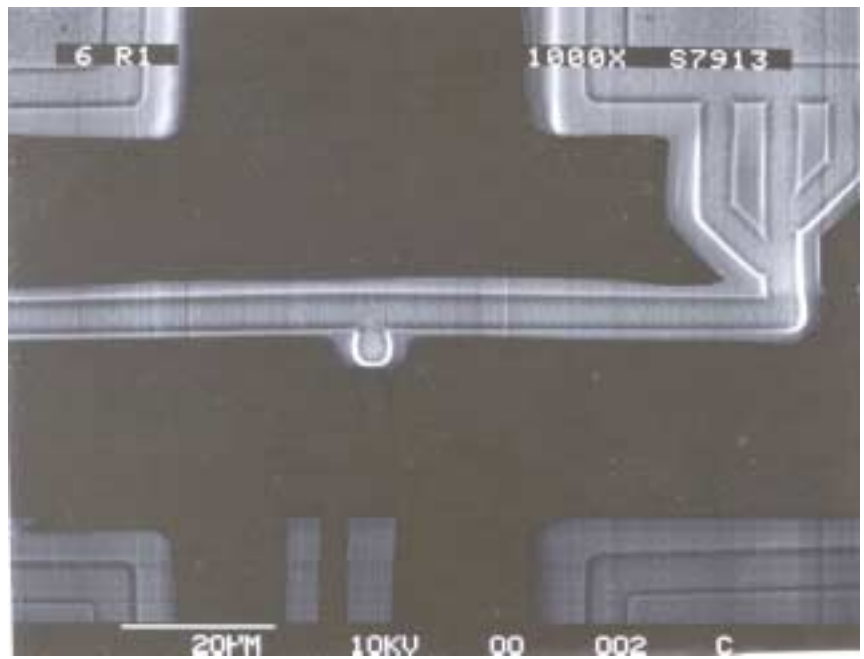
Image shows EBIC contrast when there are no open conductors.

Failure point cannot be seen in plan-view (top) standard SEM imaging imaging even for an open circuit failure after electromigration testing.

EBIC analysis of open circuit structure after electromigration testing at 220°C

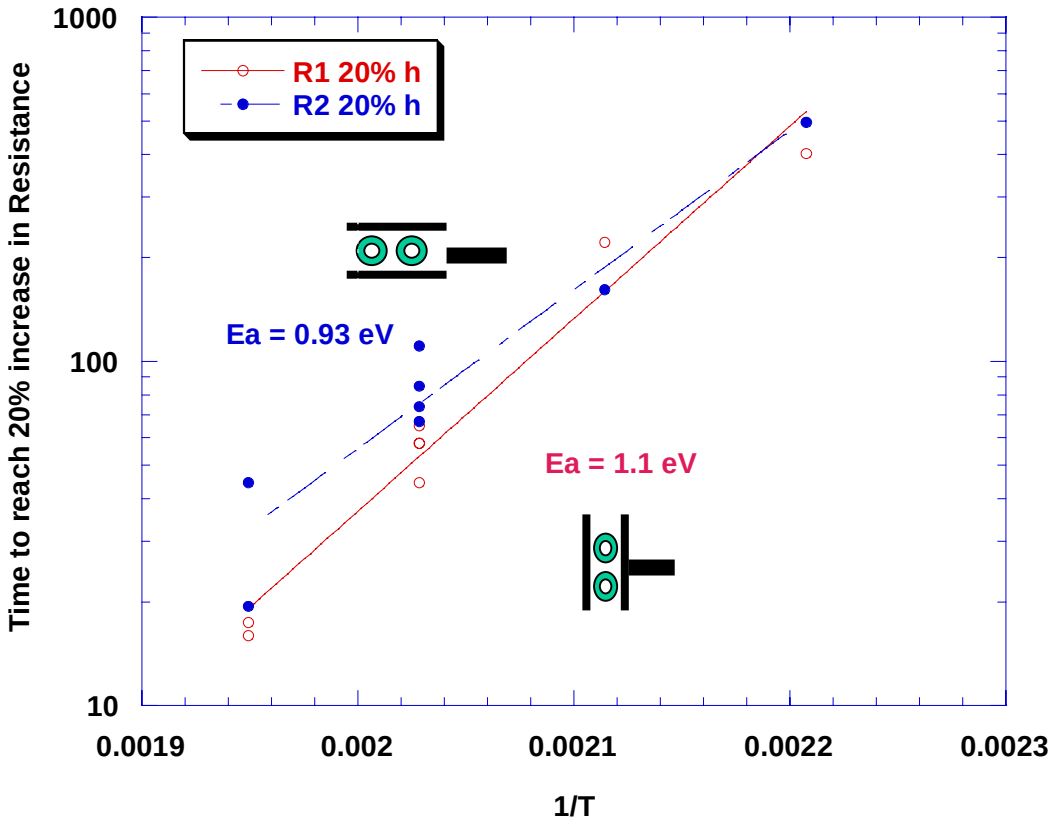






Connections were reversed to ensure that failure is only at one of the two vias

Al:Cu activation energy for electromigration:



Similar activation energies were obtained for the perpendicular and co-linear geometries, however, our measurements show that perpendicular vias have a higher probability of failing sooner. This is reflected in a different (smaller) pre-exponential factor in the Arrhenius curve.

Fit with Black's equation,

$$t = A\, j^{-n}\, e^{Ea/kT}$$

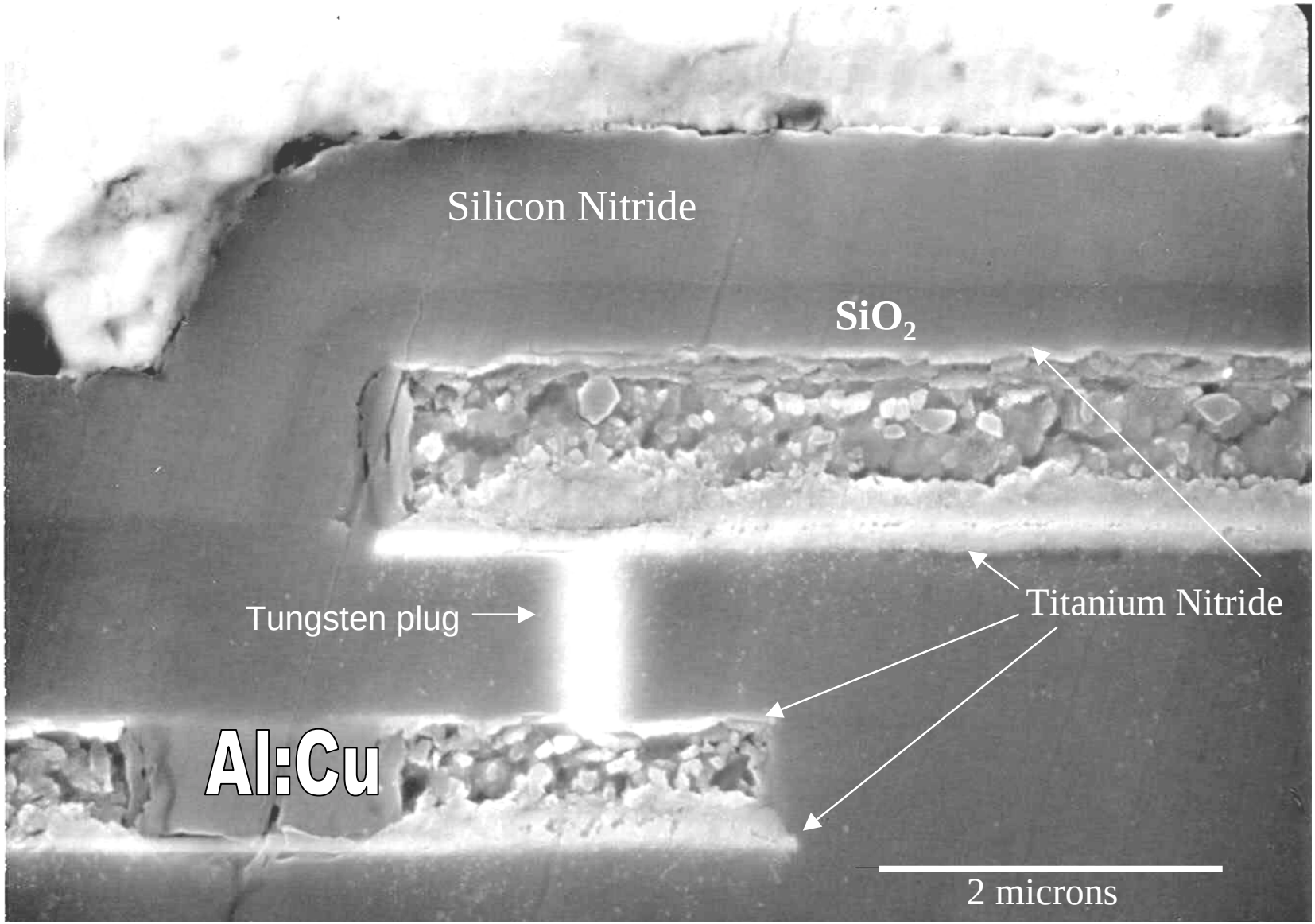
t is time to reach failure (20% degradation)

j is current density

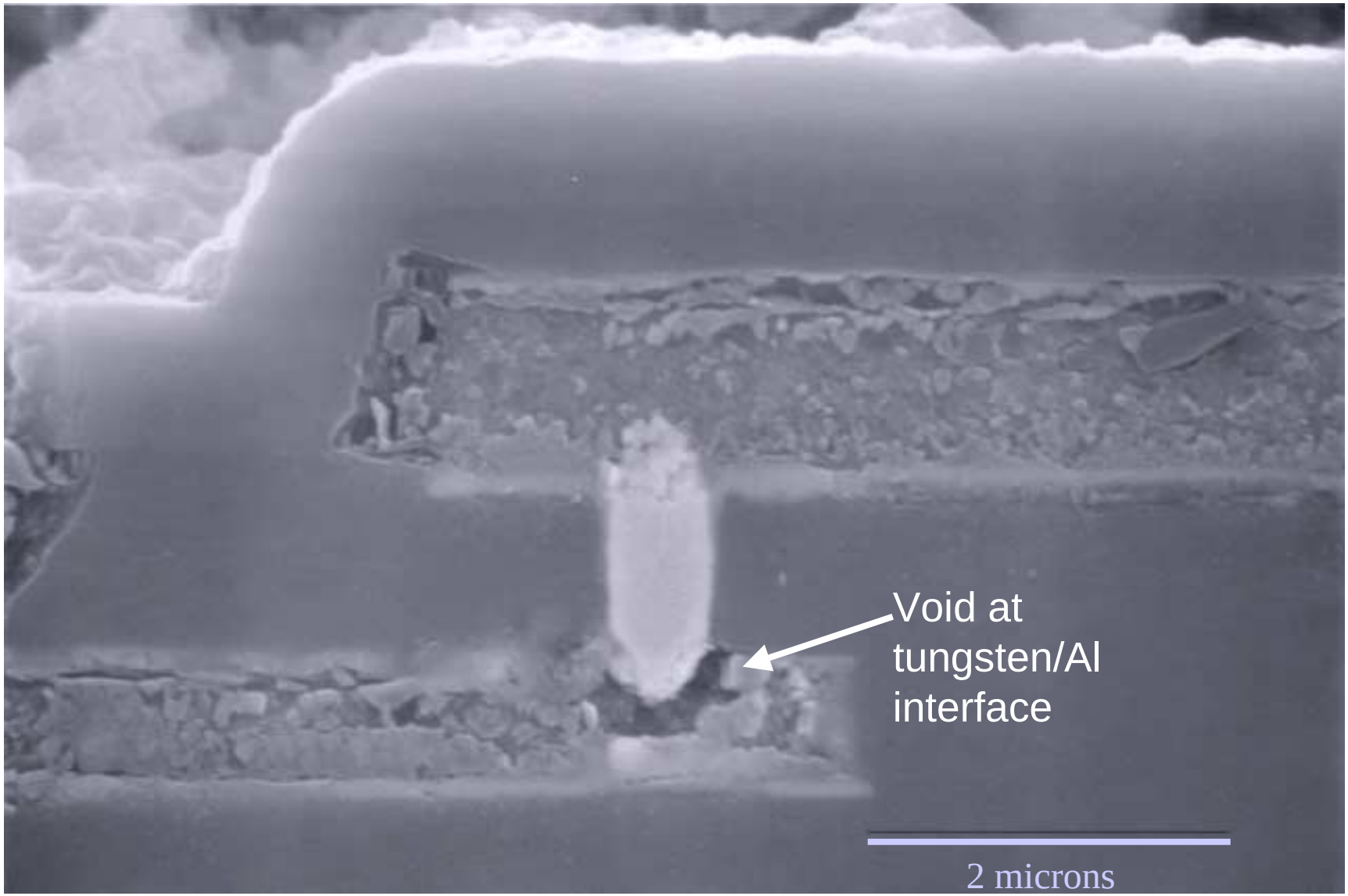
k is Boltzman's constant

Ea is activation energy (in eV)

T is temperature



Cross sectional SEM image of a “good” structure prior to EM testing, which shows one of the Tungsten plugs.

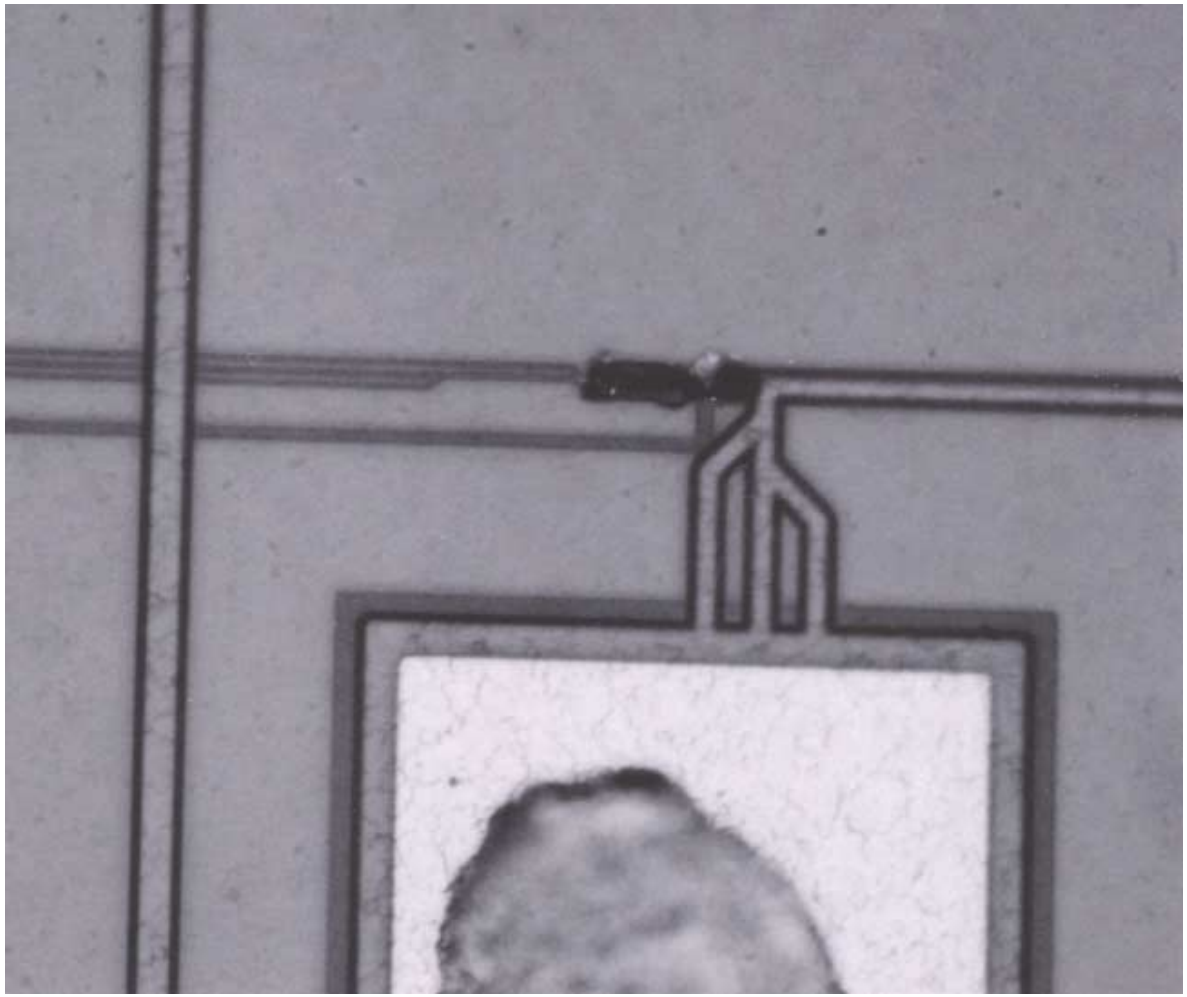


Cross-sectional SEM image of voided area at Tungsten/Al:Cu interface. Void was formed from electromigration testing at 240 C and structure failed catastrophically (open circuit).

Summary of data for Al:Cu electromigration experiments – black and blue indicates measurement done in pairs. R1 is connected so perpendicular via fails, R2 is connected to fail with parallel via.

Sample #	Via failure = or ⊥	Current (mA)	Current density (A/cm2)	T (C)	Initial R at test T	Time to degrade 10%	Time to degrade 20%	Time100% failure (open)	Comments	Failure mode
43 (Greg)	R to L	8	1.6 x 106	220	22.2	65 h	80 h			
117 (Greg)	L to R	8	"	220	21.9	> 90 h	> 90 h		Some degrad.	
150	R to L	10	2 x 106	220	24	34 h	35 h		In Series	
117	L to R	10		220	23	> 70 h	> 70 h		No degrad.	
92	none	20	4 x 106	220	21.5	> 500 h	> 500 h	No R change	No via	ESD zapped
131	none	20	"	220	21.6	> 500 h	> 500 h	No R increase	No via	ESD zapped
45 (R1)	⊥	10 and 20	2 and 4	220	23.1	50 h (10mA)	**58 h**	315 h	EBIC (Ron)	Via failure
58 (R2)	=	10 and 20	X 106	220	22.7	80 h (10mA)	**85 h**	362 h		
14 (R1)	⊥	20	4 x 106	220	24.8	63 h	**65 h**	127 h	In ESD bag	Via open
141 (R2)	=	20	"	220	24.4	110 h	**111 h**	157 h	In ESD bag	Via open
33 (R1)	⊥	20	"	240	25.1	8.5 h	**17.5**	37.5 h	In ESD box	Via open
150 (R2)	=	20	"	240	26.4	23.5 h	**44.5 h**	57.5 h	In ESD box	Via open
31 (R1)	⊥	20	"	200	23.7	105.5 h	**222 h**	347 h	In ESD box	Via open
297 (R2)	=	20	"	200	23.8	28 h	**162 h**	290 h	In ESD box	Via open
180 (R1)	⊥	20	"	180	23.2	43 h	**403 h**	663 h	In ESD box	Via open
185 (R2)	=	20	"	180	22.7	290 h	**497 h**	773 h	In ESD box	Via open
6 (R1)	⊥	20	"	240	25.3	12.7 h	**16 h**	47	In ESD box	Via open
35 (R2)	=	20	"	240	25.1	6.4 h	**19.5 h**	48 h	In ESD box	Via open
95 (R1)	⊥	20	"	200	24.5	14.4 h	**14.4 h**	377 h	In ESD box	Both to 35 Ohms
283 (R2)	=	20	"	200	23.5	70 h	**70 h**	256 h	In ESD box	(not open)
63 (R1)	⊥	20	"	220	24.0	10 h	**58 h**	161 h	In ESD bag	Open circuit
326 (R2)	=	20	"	220	24.7	31 h	**74 h**	108 h	In ESD box	Open circuit
262 (R1)	⊥	20	"	220	24.3	15.7	**44.5**	103	In ESD box	40 ohms
284 (R2)	=	20	"	220	24.2	10	**67**	103.5	In ESD box	40 ohms
44 (R1)	⊥	10	2 x 106	240	24.7	29	**222**	325	In ESD box	open
158 (R2)	=	10	"	240	25.3	32	**179**	413	In ESD box	open

Problems (1): High ESD (electrostatic discharge) sensitivity. Damage often seen in dry winter days

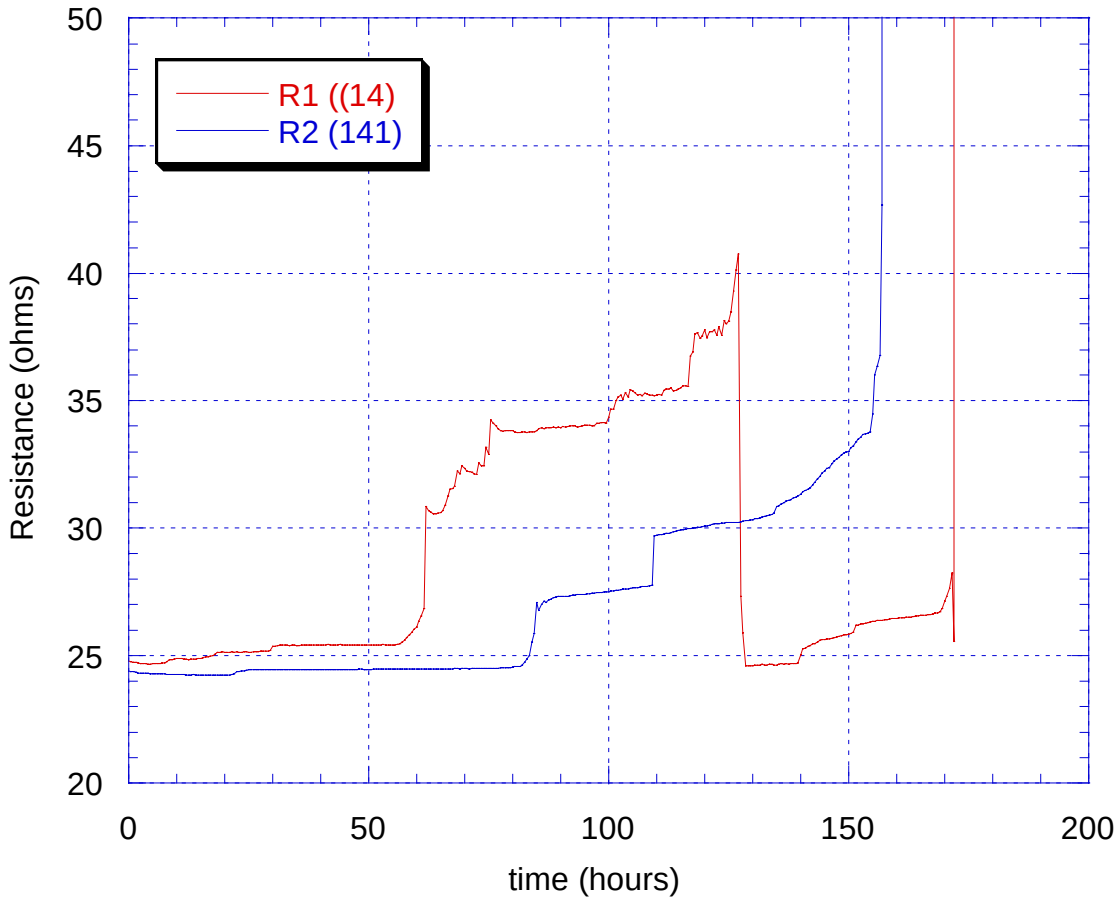


Solution:

1. Use appropriate ESD precautions during test structure handling (according to the JPL Standard procedures for handling ESD sensitive samples)

2. Store structures in ESD bags or boxes in between tests or after testing and prior to cross-sectioning.

Problem (2): Ultrahigh current densities in thinning areas can cause arcing with localized melting of metals and partial structure “repair”. This is undesirable for cross-sectional studies since this process might mask “real” (meaning electromigration induced) degradation mechanism.



Curve for R1 (red) shows a case of localized metallization “self-repair” due to melting of metals at ultra-high current densities after Al conductor thinning due to electromigration induced voiding.

Test can be stopped earlier, before circuit is completely open.

Summary of observations

- We find sharp steps in the Resistance vs. time curves (for the co-linear geometry).
- Times to failure (or 20% degradation) have the expected Arrhenius dependence.
- Activation energies obtained from Arrhenius plots are 1 eV - high for Al conductors.
- EBIC (electron beam induced conductivity) is a useful technique to locate failure, but it works best if line is open.
- Perpendicular geometry is more likely to fail earlier than structures with co-linear (parallel) geometry (as seen in 8 out of 10 test pairs).
- Failure is due to void formation at the Al:Cu/W interface near cathode.