Test Synopsis – 2/6/04

A Comparative Study of Heavy Ion and Proton Induced Bit Error Sensitivity and Complex Burst Error Modes in Commercially Available High Speed SiGe BiCMOS

By

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ABSTRACT

We compare heavy ion and proton SEE data on commercial SiGe technologies from IBM's 7HP process and Jazz Semiconductor's Jazz-120 process at data rates from 50 Mpbs to 12.4 Gbps. Burst error trends correlate with both data rate and particle LET.

Introduction

In previous years, we and other authors, have conducted several investigations showing, on the one hand, very encouraging total ionizing dose (TID) results in the 1st, 2nd and 3rd generations of IBM's BiCMOS processes (known as 5HP, 6HP and 7 HP respectively) [1 and references therein]. However, over recent years the demonstration of sensitivity to single event effects has arisen as a key concern for some applications [2-8]. These concerns were first demonstrated experimentally in [2] in the 5HP version of the process with half micron drawn feature sizes, and more recently in [3] which included charge collection and modeling results implying that the electrically active substrate was an important factor. Additional modeling studies and an increasing understanding of the role of the substrate are expanded on in [4-8]. To date, there has not been a successful demonstration of SEE hardening in SiGe, hovever the technology continues to advance and grow in importance to the satellite community.

Our study has three primary contributions to furthering the understanding of commercially available SiGe technology. First, we step back from the high speed HBT oriented investigations covered in [1-8] to look carefully at the CMOS used in IBM's 5HP BiCMOS product family. To date, these are the first investigations to report on the latchup and SEU characteristics of this key aspect of 5HP CMOS. Next, we provide a detailed comparison of IBM's 7HP HBT logic with its commercially competitive counterpart from Jazz Semiconductor. For this comparison, identical 127 bit shift register circuits have been fabricated and tested to the same heavy ion and proton environments using exactly the same test equipment for both tests. The remainder of this summary will provide highlights of these studies, and also introduce new data providing insights into the evolution of complex error signatures that appear to be common to both families of high speed SiGe.

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SEE Performance of 5HP CMOS

Our test circuit was designed and packaged at the Mayo Foundation's Special Purpose Processor Development Group's laboratory facilities in Rocnester MN. The test vehicle was processed at IBM's commercial facilities in Burlington, VT, and the Mayo design was incorporated into a multiuser mask set through the services of MOSIS [9]. The process version available through MOSIS is known as 5AM, and differs only in the details of the top level metal from the 5HP CMOS process. The process uses a 0.5 micron drawn minimum feature size.

A 127 bit serial shift register was designed using a standard master-slave flip flop architecture. The test set shown as figure 1 incorporated a commercial bit error rate test set (BERT) which operates from 7 Mega bits per second (Mbps) to 1 Giga bit per second (Gbps). Amplifiers and bias tees converted the CML levels from the BERT pattern generator to proper CMOS levels to drive the differential data and differential clock inputs of the CMOS DUT. In the absence of particles, the circuit operated error free under broadband conditions from 10 Mbps to 670 Mbps. This upper limit was common to the 3 DUTs we examined, and closely matches the limiting data rate expected from circuit simulations using SPICE.

One significant motivation for this test concerned the possibility of single event latchup (SEL). No evidence of any form of latchup was seen even after fluences exceeding 10^8 ions/cm^2 of Xe with LET > 53 MeV cm^2/mg.

Bit errors were seen, and the data of figure 2 show an onset threshold LET of 18 MeV cm^2/mg with a saturated device cross-section of 10^{-4} cm^2 *when the circuit was operated at a data rate of 10 Mbps.* Comparison with the data of figure 3 show a pronounced increase in the saturated cross-section and a very dramatic reduction in onset LET for the highest

data rate of 670 Mbps. The full paper will describe the details of the trend with data rate, but we note this is the most dramatic dependence of threshold LET that we have seen. Also, we note that this digital register showed no noticeable change in performance after exposure to 2 Mrad(Si) of proton dose, and those data will be described in the full paper.

SEE Comparison of IBM's 7HP with Jazz-120 SiGe

Both test articles were designed and packaged by the Mayo Foundation. Again, the architecture was a 127 serial data register suing a standard master-slave flip flop. The IBM 7HP process has been previously described [1], and uses a 0.17 micron minimum feature size SiGe HBT resulting in a F_t of 120 GHz. The Jazz-120 also uses both deep and shallow trench isolation with the same minimum feature size, but with a slightly higher F_t of 150 GHz.

The test set used for both DUT types is shown as Figure 4. We used a 7-bit linear feedback shift register to provide a 127 bit pseudorandom sequence [described in 2] for differential inputs to the DUT. The commercially available Anritsu pattern detector was programmed to recognize the expected 127 bit sequence, and provide full error reporting, including the number of errors per error event and their positions in the bit stream. The upper limit of this unit of 12.5 Gbps limited the test capability for both the IBM and Jazz DUT types, and scope eye diagrams suggested the devices would perform to > 15 Gbps.

Figure 5 presents the device level error event cross-section for the IBM 7HP HBT register, and it is characterized by both a low threshold LET and a high saturated cross-section. We also note the anomalous behavior with incidence angle at low LETs which has also been reported in other 5HP and 7 HP circuits [1 and 2]. Data were acquired at each LET for at least seven data rates covering the range from 50 Mbps to 12.4 Gbps. These results are summarized in figure 6, and there is a remarkable lack of dependence on the event cross-section with data rate over this range. Note however, that the event cross-section tells only a portion of the story. In Figure 7 we examine the average errors per error event as it trends with data rate 4 different LETs. Clearly, at the lower data rates, most errors are only single bit errors even at high LETs. But, there is a strong trend towards longer error bursts when an event corresponds to high data rate. This is especially so with high LET particles. We believe these are the first data reported which describe this complex error behavior, and it obviously has consequences for error correcting algorithms.

Figure 8 presents the proton sensitivity for the 7HP SiGe register, and we note part to part similarity as well as close agreement between the 28 and 63 MeV data points.

Figures 9, 10, and 11 present the results of the Jazz-120 HBT circuit tests. We note a strikingly similar response in all aspects of the SEE response relative to the IBM 7HP data. Interestingly, even the anomalous behavior at high angles with low LETs is seen in figure 9, and is possibly more pronounced than in the IBM data. Also, figure 11 shows similar, but possibly more enhanced sensitivity to the burst error characteristics seen in the IBM devices.

In the full paper, we intend to fully develop the description of the burst nature of errors. We recognize that more bits are effected when either high data rates or high LETs are involved, and intuitively this suggest a time constant associated with "flushing" the ion deposited charge from the circuit. Figure 12 reveals a more complex picture and shows that the numbers of errors in a burst are not uniformly distributed. In the paper, we will explore the implications for origin of the errors as either hits to the clock distribution circuitry, or register elements in the data path.

References

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[9] http://www.mosis.org/Products/menu-products.html

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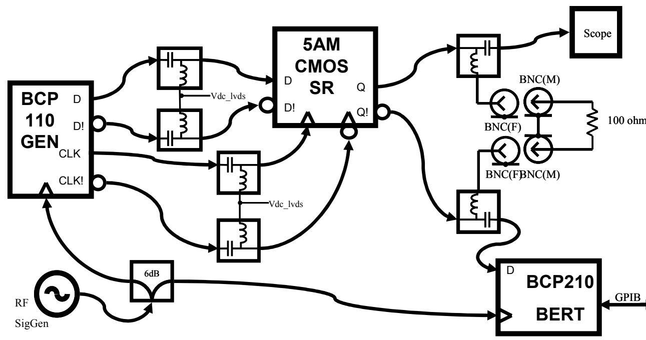

Figure 1. A commercial bit error rate test (BERT) set from Broadband Communications Products (BCP) generated the data stream to the IBM 5AM CMOS Device under test (DUT) and captured errors at data rates from 10 Mbps to 670 Mbps.

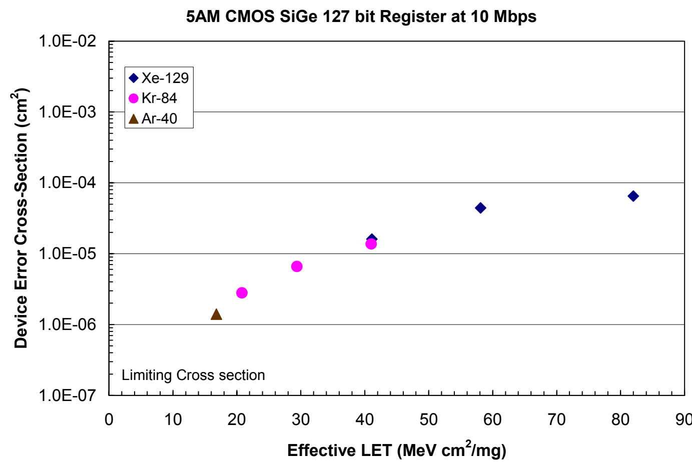

Figure 2. At low data rates, the 5AM CMOS 127 bit shift register exhibits sensitivity to Ar-40 ions only at grazing incidence with effective LET of 17 MeV cm^2/mg.

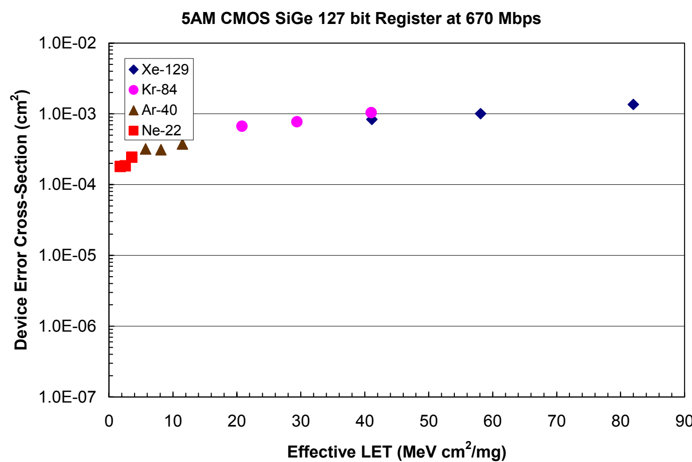

Figure 3. At the highest data rate tested of 670 Mbps, the saturated cross-section has increaded by 10x and the threshold LET is significantly suppressed. In the full paper, we will also present proton upset data corresponding to this data rate dependence.

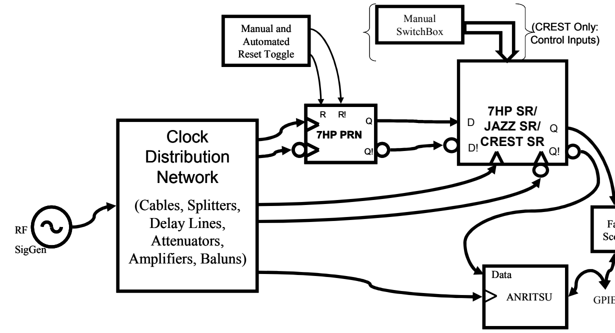

Figure 4. A commercial bit error rate test (BERT) detector from Anritsu received the data stream to the IBM 7 HP HBT DUT and captured errors at data rates from 50 Mbps to 12.4 Gbps. A 7HP PRN data source supplied the IMB and Jazz setups.

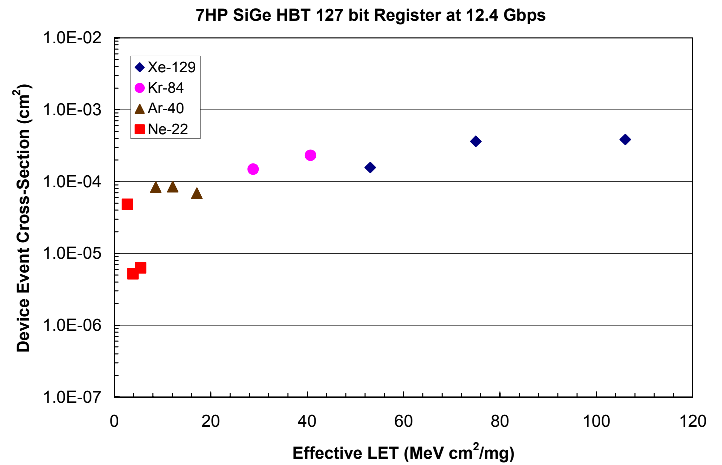

Figure 5. The 7HP 127 bit serial register showed relatively high saturated cross section as well as low threshold LET, indicating a definite sensitivity to soft errors. Note the cross-section is per event, and many events involved more than one bit in error.

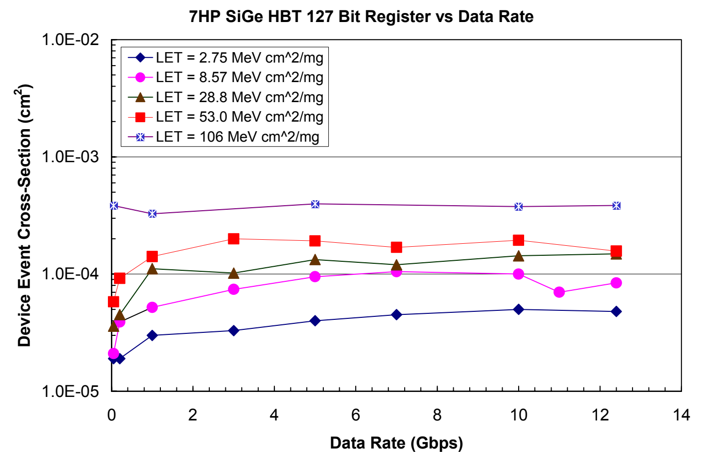

Figure 6. The IBM 7HP register showed a remarkably weak event cross section dependence on data rate irrespective of effective LET.

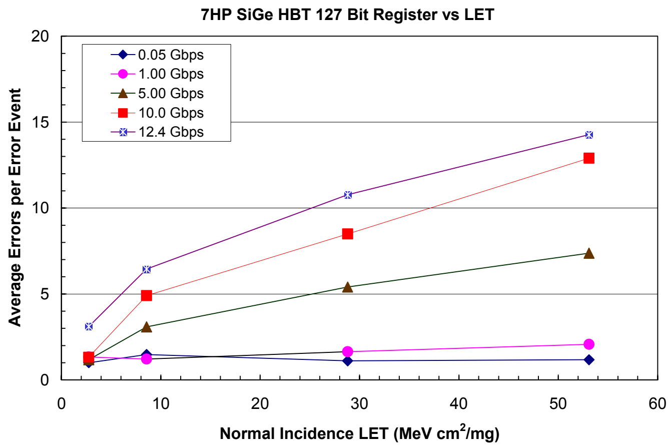

Figure 7. For the IBM 7HP register, the average number of errors per error event tended up with both data rate and with particle LET. This is consistent with the circuit requiring a finite interval (or bit periods) to dissipate a given amount of deposited charge.

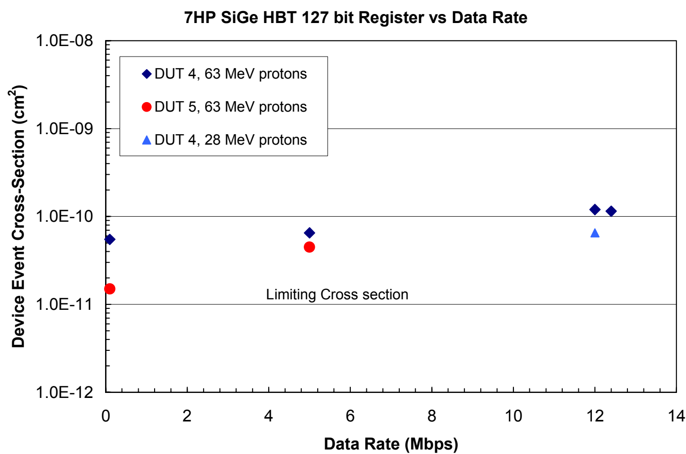

Figure 8. Proton data reveal negligible device to device variation in sensitivity, and the 28 MeV data is only slightly lower than the 63 MeV results.

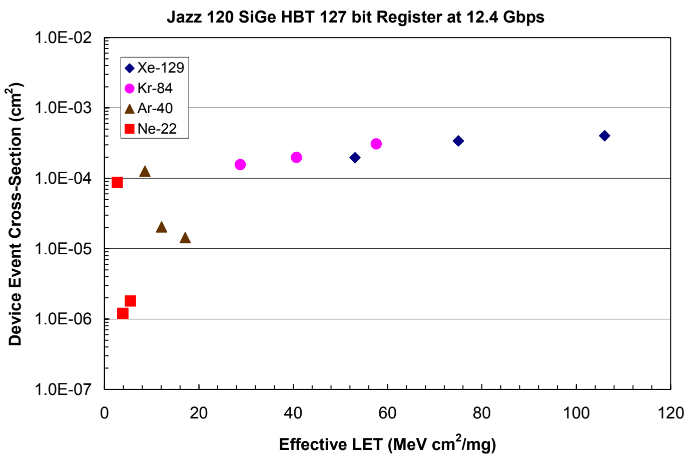

Figure 9. The Jazz-120 127 bit serial register showed relatively high saturated cross section as well as low threshold LET, indicating a definite sensitivity to soft errors. Note the cross-section is per event, and many events involved more than one bit in error. These results are very similar to the IBM 7HP data of Fig. 5.

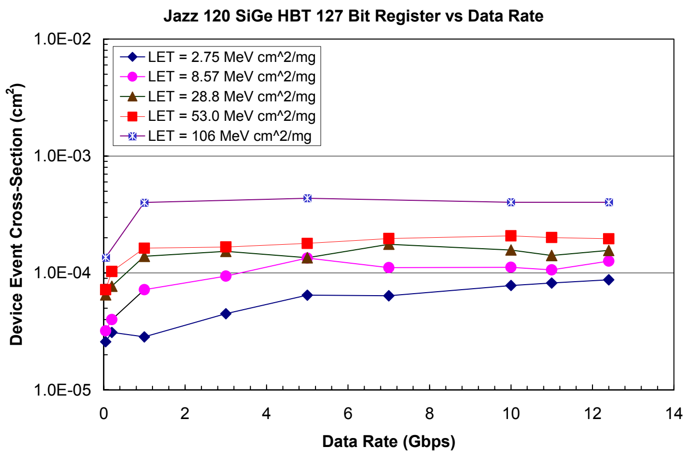

Figure 10. The Jazz-120 register showed a remarkably weak event cross section dependence on data rate irrespective of effective LET, as did the IBM results of Figure 6.

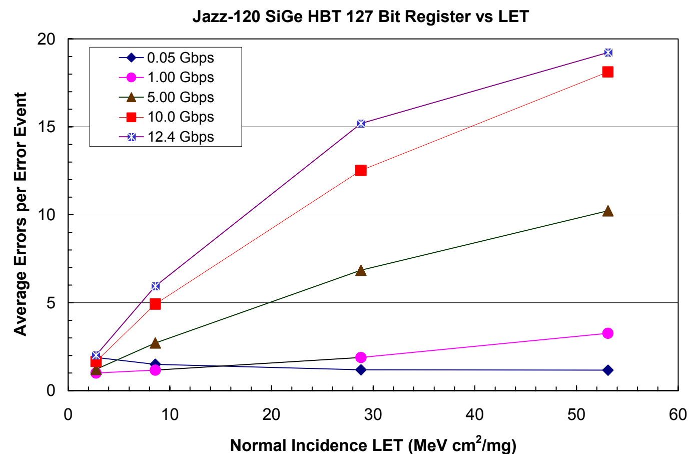

Figure 11. For the Jazz-120 register, the average number of errors per error event tended up with both data rate and with particle LET with a slightly stronger trend than the IBM 7HP ciricuit. This is consistent with the circuit requiring a finite interval (or bit periods) to dissipate a given amount of deposited charge.

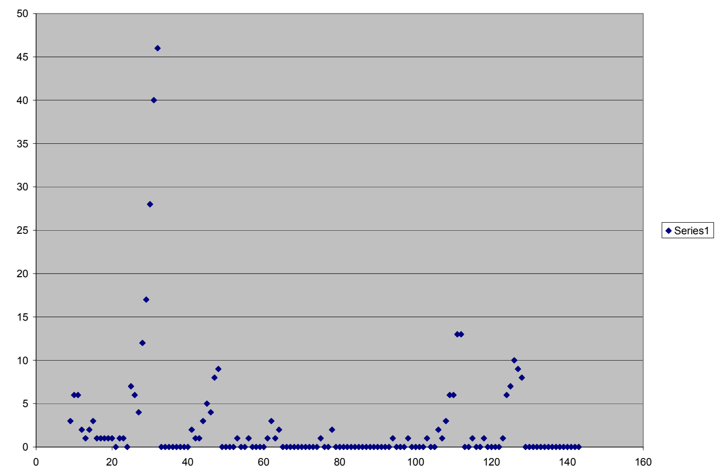

Figure 12. For errors lasting longer than a single bit, the durations did not vary randomly. This histogram indicates the occurrences of a given number of bits in error for a single error event.