USE OF PLASTIC ENCAPSULATED MICROCIRCUITS (PEMs) IN MILITARY EQUIPMENT

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Abstract

Plastic encapsulated microcircuits (PEM) are molded, potted, or coated semiconductor die or hybrid integrated circuits in which the encapsulant or coating is in direct contact with the die, leadframe and/or signal traces, interconnects, and barrier layers of the device. Hermetically sealed microcircuits (HSM) have a sealed cavity and the die, leadframe and/or signal traces, interconnects, and barrier layers are not in contact with the metal and/or ceramic package. PEMs are a subset of plastic encapsulated microelectronics, but these terms are used interchangeably in most cases.

Changes to the military procurement process have increased the use of commercial off-the-shelf (COTS) items and have resulted in the use or proposed use of PEMs instead of HSMs or in place of HSMs in military equipment. The purpose of this paper is to identify issues which must be addressed when determining whether the use of PEMs is acceptable in the desired application in military equipment. Issues discussed include size, weight, cost, availability, performance, tolerance to shock and vibration, outgassing, thermal resistance, reliability, storage, Parts Control Program Plan (PCPP), assembly and repair, and conformal coating.

APPLICABLE DOCUMENTS

Government documents:[1]

SPECIFICATIONS:

MIL-H-38534: Hybrid Microcircuits, General Specification for (Superseded by MIL-PRF-38534)

MIL-PRF-38534: Hybrid Microcircuits, General Specification for (Superseded MIL-H-38534)

MIL-I-38535: Integrated Circuits (Microcircuits) Manufacturing, General Requirements for (Superseded by MIL-PRF-38535)

MIL-PRF-38535: Integrated Circuits (Microcircuits) Manufacturing, General Specification for (Superseded MIL-I-38535)

MIL-I-46058: Insulating Compound, Electrical (for Coating Printed Circuit Assemblies)

STANDARDS:

MIL-STD-1835: Interface Standard for Microcircuit Case Outlines

MIL-STD-883: Test Methods and Procedures for Microelectronics

OTHER PUBLICATIONS:

MIL-HDBK-103: Handbook for List of Standard Microcircuit Drawings

MIL-HDBK-179: Microcircuit Acquisition Handbook

QML-38534: Qualified Manufacturers List of Custom Hybrid Microcircuits Qualified Under Military Specification MIL-H-38534 Custom Hybrid Microcircuits, General Requirements for

QML-38535: Qualified Manufacturers List of Advanced Microcircuits Qualified Under Military Specification MIL-I-38535 Microcircuits Manufacturing, General Requirements for

[1] For copies of Government documents: Standardization Documents Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.

Non-Government documents:

STANDARDS:

JOINT STANDARDS:

ANSI/EIA/IPC/J-STD-001: Requirements for Soldered Electrical and Electronic Assemblies

AUTOMOTIVE ELECTRONICS COUNCIL:[2]

CDF-AEC-Q100: Stress Test Qualification for Automotive - Grade Integrated Circuits

CDF-AEC-Q101: Stress Test Qualification for Automotive Grade Discrete Semiconductors

CDF-AEC-Q200: Stress Test Qualification for Automotive - Grade Passive Components

ELECTRONIC INDUSTRIES ASSOCIATION:[3]

EIA JESD-22: Reliability Test Methods for Packaged Devices

EIA JESD-22-A101: JESD-22 Test Method A101, Steady State Temperature Humidity Bias Life Test

EIA JESD-22-A102: JESD-22 Test Method A102, Accelerated Moisture Resistance - Unbiased Autoclave

EIA JESD-22-A104: JESD-22 Test Method A104, Temperature Cycling

EIA JESD-22-A108: JESD-22 Test Method A108, Bias Life

EIA JESD-22-A110: JESD-22 Test Method A110, Highly Accelerated Temperature and Humidity Stress Test (HAST)

[2] For copies of Automotive Electronics Council documents: Automotive Electronics Council, Delco Electronics, 1800 East Lincoln Road M-3, Kokomo, IN 46904-9005.

[3] For copies of Electronics Industries Association documents: Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.

EIA JESD-22-A112: JESD-22 Test Method A112, Moisture Induced Stress Sensitivity for Plastic Surface Mount Devices

EIA JESD-30: Descriptive Designation System for Semiconductor Device Packages

EIA JESD-47: Stress Test Driven Qualification of Integrated Circuits

EIA JEP-95: Registered and Standard Outlines for Solid State and Related Products

INTERCONNECTIONS PACKAGING CIRCUITRY:[4]

ANSI/IPC-D-275: Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies

ANSI/IPC-R-700: Suggested Guidelines for Modification, Rework and Repair of Printed Boards and Assemblies

ANSI/IPC-SM-786: Recommended Procedure for Handling of Moisture Sensitive Plastic IC Packages

IPC-CC-830: Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

BACKGROUND

The PATRIOT (Phased Array TRacking to Intercept Of Target) system started without any PEMs because of the need for high Mean Time Between Failure (MTBF) times due to a high operating rate and long periods of storage for spare parts and for the missile. Growth programs and acquisition streamlining, i.e., cost, have required a "relook" at the use of PEMs. Present low operating rates have allowed PEMs to be incorporated into ground equipment, but not in the missile due to long periods of dormant environment and low operating hours. Currently the PATRIOT system is deployed in environments ranging from hot and humid to cool and wet. Since the PATRIOT system uses external air to cool equipment, the fact that PEMs "breath" and HSMs do not "breath" is a concern for operational and storage environments, especially since there is a lack of storage data for normal, dry-packed, and nitrogen stored PEMs and for conformal coated PEMs on assemblies. One can foresee the increased usage of PEMs as we move into the 21st century when performance requirements rather than Technical Data Packages (TDP) will define end items.

[4] For copies of Interconnections Packaging Circuitry documents: IPC, 7380 North Lincoln Avenue, Lincolnwood, IL 60646-1705.

PEM ISSUES

Size: For the same style package, PEMs and HSMs will be about the same size. However, some PEMs are available in smaller footprint packages such as small-outline packages, shrink small-outline packages, and thin small-outline packages. See MIL-STD-1835, EIA JEP-95, and EIA JESD-30 for case outlines.

Use of small footprint PEMs allows a higher device packing density on a printed wiring board (PWB) and can result in reduced signal trace lengths which will decrease propagation delays and help alleviate problems of high edge-rate (low rise and fall times) signals on long traces.

Weight: PEMs generally weigh about half as much as the same style HSM package, e.g., a 14-lead plastic dual in-line package (PDIP) weighs about one gram versus about two grams for a 14-lead ceramic dual in-line package (CERDIP).[5] If given devices can be PEM or HSM, vibration and shock analysis and testing must address the use of each package type.

Cost: Low complexity PEMs, e.g., buffers, drivers, counters, etc., are about one-half the cost of commercial HSMs and about one-quarter the cost of military HSMs. High complexity PEMs, e.g., microprocessors, digital signal processors, gate arrays, etc., are about one-quarter the cost of commercial HSMs and about one-eighth the cost of military HSMs. However, the additional cost of special environmental and electrical testing requirements, storage, thermal design, post assembly inspection, reduced operational and storage reliability impact to spares procurement, and obsolescence impact due to shorter life cycles for PEMs can offset the expected cost savings of PEMs and could result in a higher life cycle cost as compared to HSMs.

Availability: PEMs are more widely available in different packages and functions than HSMs and have shorter lead and after receipt of order times. However, since PEMs have a shorter life cycle than HSMs and the life cycle is usually compressed for more complex devices because of vendors trying to keep up with technology advances and customer requests and requirements, near future obsolescence of PEMs must be addressed and solutions agreed upon by design and cost personnel prior to preliminary design review.

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[5] "Plastic Encapsulated Microelectronics," *1.2.1 Size and Weight.* CALCE EPRC. Online. Available: http://spezia.eng.umd.edu/general/demos/pem/chap1/1_1_1.html#sizeand. [8 August 1997].

Performance: The performance of microcircuits per vendor or Government documentation is based on a given operating environment specified as a case temperature (T_C) and/or an ambient temperature (T_A) range and may include, especially for PEMs, the maximum relative humidity (RH) levels for different temperatures. The performance of a part outside its specified operating temperature range may be acceptable, though probably degraded, but will not be guaranteed by the vendor and will most likely void the part guarantee or warranty. Storage temperatures must also be addressed to assure that part damage does not occur.

Typical military T_A operating ranges are -45.6C to 49C or -32C to 49C and T_A storage ranges are -45.6C to 71C or -33C to 71C. Discrete components such as microcircuits usually have a low temperature requirement the same as the low temperature for storage, e.g., -45.6C or -33C, and have a high temperature requirement enough above the high temperature for operation, but no less than the high temperature for storage, e.g., 71C, plus the difference between the T_A and T_C temperatures to account for operational heating of the component, assembly, and heat transfer media. The standard military HSM T_A range is -55C to 125C. Some other non-typical HSM T_A ranges that might be encountered are -45.6C to 85C, -45.6C to 71C, -40C to 85C, and -33C to 71C. MIL-PRF-38535 and MIL-STD-883 (references MIL-PRF-38535) HSMs shall have a T_A range of -55C to 125C per MIL-PRF-38535[6] unless otherwise specified in the device documentation, e.g., a DSCC SMD document – not a AMCOM document, or if a contractor prepared document with a different T_A range is approved by the acquiring activity, e.g., AMCOM. The standard industrial T_A range for microcircuits is -40C to 85C and for automotive microcircuits the T_A range for Grade 1 is -40C to 125C, Grade 2 is -40C to 105C, and Grade 3 is -40C to 85C.

Tolerance to shock and vibration: PEMs are more mechanically rugged and have a high tolerance to shock and vibration as compared to HSMs since PEM die and bonding wires are not free to move within the encapsulant.

[6] MIL-PRF-38535D Amendment 1, 15 April 1996, Appendix A, Section 30.2 Item requirements.

Outgassing: Experimental results from a NASA report[7] which evaluated 21 PEMs in a variety of packages from 12 different manufacturers demonstrated that outgassing was below the 1.0% total mass loss and 0.1% collected volatile condensable material requirements for NASA space flight use. The study did not evaluate the effects of long term storage and stated that the effects of parameters such as molding compound moisture content and storage conditions should be studied in correlation with outgassing data to address the suitability of PEMs in space flight applications. The recommendation would also apply to the use of PEMs in military equipment.

Thermal resistance: The baseline junction-to-case thermal resistance (θ_{JC}) for standard HSMs can be found in MIL-STD-1835 and the θ_{JC} and/or junction-to-ambient thermal resistance (θ_{JA}) for non-standard packages must be specified by the part documentation. The part documentation must always be checked first even if the package style is known since the θ_{JC} for the part and package to be used may be different than the baseline θ_{JC} listed in MIL-STD-1835. The MIL-STD-1835 package case outline list table has a note which lists the θ_{JC} to be used for large dies.[8] The concern is that for the same style package a PEM will have a greater thermal resistance than a HSM, e.g., θ_{JC} = 28C/W for a 16-pin CERDIP and θ_{JC} = 37C/W for a 16-pin PDIP – a 32% increase from the HSM CERDIP to the PEM PDIP. Any increase in thermal resistance for a given part at a given power dissipation will increase the die junction temperature (T_J). A small increase in T_J will result in a minor increase in mean time between failures (MTBF) whereas a high power dissipating device will have a large increase in T_J and will result in a major increase in MTBF. The difference between the two MTBFs will be greater for a PEM than for a HSM due to the increased θ_{JC} for the PEM. Heat sinks are a viable option for high power devices, especially PEMs, and use of such will increase the cost of an assembly and could result in increased board pitch (board-to-board spacing) for the next higher assembly. Use of PEMs in place of HSMs will require a higher capacity thermal removal system to achieve the same assembly MTBFs and the system MTBF will increase slightly due to the added thermal removal hardware. Design personnel will have problems calculating the MTBF for parts that do not have the thermal resistance specified in the part

[7] Robert Savage, Electronic Packaging and Research Branch, Goddard Space Flight Center. Abstract: "Outgassing Properties of PEMs." Online. Available: http://arioch.gsfc.nasa.gov/eee_links/vol_02/no_01/eee2-1o.htm. [8 August 1997].

[8] MIL-STD-1835B, 3 September 1996, TABLE VI Package case outline list, θ_{JC} Column, Note 2/, 'The "base-line" values shown are worst case (MEAN + 2σ) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11C/W; chip carrier, 10C/W; flat pack, 10C/W; pin grid array, 10C/W.'

documentation. This is the case for some Defense Electronics Supply Center (DESC) standardized military drawings (SMDs) for PEM parts.[9]

The following thermal resistance and temperature equations are useful for reference:

Variables used in thermal resistance and temperature equations:

θ_{CA}: Case-to-Ambient thermal resistance
θ_{CS}: Case-to-Sink thermal resistance
θ_{JA}: Junction-to-Ambient thermal resistance
θ_{JC}: Junction-to-Case thermal resistance
θ_{SA}: Sink-to-Ambient thermal resistance
T_A: Ambient Temperature
T_C: Case Temperature
T_J: Junction Temperature
T_S: Sink Temperature
W: power dissipated by device in Watts

Thermal resistance and temperature equations:

$\theta_{JA} = (\theta_{JC} + \theta_{CA})$
$\theta_{JC} = (\theta_{JA} - \theta_{CA})$
$\theta_{CA} = (\theta_{JA} - \theta_{JC})$
$T_J = (T_A + (W*\theta_{JA})) = (T_C + (W*\theta_{JC}))$

Additional thermal resistance and temperature equations apply if a heat sink is used:

$\theta_{CA} = (\theta_{CS} + \theta_{SA})$
$\theta_{CS} = (\theta_{CA} - \theta_{SA}$
$\theta_{SA} = (\theta_{CA} - \theta_{CS})$
$T_J = (T_S + (W*\theta_{JS}))$

[9] DESC SMD-5962-95551, revision "-", case outline "X," DESC SMD-5962-95640, revision "B", case outlines "X" and "Y," and DESC SMD-5962-96790, revision "-", case outline "X."

Reliability: Long term operating and storage reliability of PEMs with different functions in multiple package styles from multiple vendors is not yet available. A five year PEM long term storage program was started in July 1994 by Rome Laboratory and AMCOM,[10] but only includes 300 complimentary metal oxide semiconductor generic type CD4011 devices in a 14-pin PDIP from each of five suppliers. Long term storage reliability data for PEMs is needed for parts stored and transported for repair use and for parylene conformal coated PEM containing assemblies (see Conformal coating) stored and transported for repair use and as installed in spared major end items. Long term operating reliability data for PEMs is needed for parylene conformal coated PEM containing assemblies (see Conformal coating) installed and functioning in major end items.

Storage: For production, repair, and for spares use, dehydrate bake PEMs (typically, 24 hours at 125C) to assure that the total absorbed moisture level is less than 0.05% of the total package weight and place in dry-pack packaging (desiccant and moisture indicator card in package), or nitrogen storage. A total absorbed moisture level of 0.11% of the total package weight is a recommended maximum limit (see ANSI/IPC-SM-786).

Parts Control Program Plan (PCPP) for PEMs: A PCPP should be developed using MIL-HDBK-179 and the following paragraphs for guidance:

Use highest temperature range and highest qualified PEM available. DSCC SMD PEMs are preferred (see MIL-HDBK-103[11]), otherwise QML-38534,[12] QML-38535,[13] CDF-AEC-Q100, and EIA JESD-47 PEM suppliers should be considered. Do not post screen PEMs to an extended T_A range to meet system requirements, unless the extended temperature range is not more than 5C to 10C greater at either end of the range and only then if quality assurance and design personnel can determine that adequate performance, device reliability, and device yield exist for the electrical and temperature requirements placed on the PEM. Vendors that will deliver extended temperature range uprated parts may or may not guarantee long term performance of the parts.

Discrete semiconductors from CDF-AEC-Q101 suppliers and passive components from CDF-AEC-Q200 suppliers should be considered for use in encapsulated hybrid circuits.

Multiple source PEMs are preferred, i.e., parts are interchangeable.

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[10] Duane A. Gilmour. Abstract: "RL/MICOM PEM Storage Reliability Program." Online. Available: http://erd.rl.af.mil/ER-News/21/storage.html. [8 August 1997].

[11] MIL-HDBK-103: Online database and document downloads available via DSCC Internet Web Site. Online. Available: http://www.dscc.dla.mil/V/VQ. [8 August 1997].

[12] QML-38534: Online database and document downloads available via DSCC Internet Web Site. Online. Available: http://www.dscc.dla.mil/V/VQ. [8 August 1997].

[13] QML-38535: Online database and document downloads available via DSCC Internet Web Site. Online. Available: http://www.dscc.dla.mil/V/VQ. [8 August 1997].

PEMs which meet MIL-STD-883 die design and current loading requirements are preferred.

Document PEMs in enough detail to allow interchangeability between different vendors.

Part change notification of all proposed design changes is required for all vendors.

Establish a microcircuit and semiconductor receiving inspection program and perform non-destructive inspection, e.g., X-ray or CSAM, to check for cracks, voids, and delamination. Determine if parts should be tested at temperature extremes.

Quality assurance and design personnel must determine the impact to performance, production, testing, and reliability of a higher device packing density due to the use of small footprint PEMs which results in higher thermal density, more PWB signal layers, more PWB and component interconnections, including PWB via holes, and higher probability of on-board and off-board electromagnetic interference. Assure that PWB design standards such as ANSI/IPC-D-275[14] and thermal and electrical derating requirements are documented and followed.

Date code and vendor code marking of PEMs is required for traceability of failed parts and a failure reporting analysis and corrective action system should be implemented. Failure analysis personnel will have to become familiar with decapsulation procedures and equipment for different PEM packages.[15]

Review vendor device reliability data and quality control for acceptability. Determine minimum requirements for reliability characterization by performing tests such as high temperature operating life,[16] temperature humidity bias,[17] highly accelerated stress test,[18] autoclave,[19] and temperature cycling.[20]

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[14] ANSI/IPC-D-275: Use Class 3 for high reliability military equipment, Class 2 for non-tactical military equipment, and Class 1 for general/consumer/COTS equipment.

[15] Martin L. Winsemius, Director of Engineering, B&G International. "PEM Decapsulation Forecast." Online. 29 August 1996. Available: http://spezia.eng.umd.edu/general/PEMs/pem1.html. [8 August 1997].

[16] MIL-STD-883 Method 1005, EIA JESD-22-A108, or equivalent; 150C T_A for 408 hours, or 125C T_A for 1008 hours (T_J not to exceed 175C).

[17] EIA JESD-22-A101, or equivalent; 185C/85%RH/1000 hours.

[18] EIA JESD-22-A110, or equivalent; 130C/85%RH/72 hours.

[19] EIA JESD-22-A102, or equivalent; 121C/15 pounds per square in gauge/196 hours.

[20] MIL-STD-883 Method 1010, EIA JESD-22-A104, or equivalent; -65C/150C/500 cycles, or -50C/150C/1000 cycles.

Assembly and repair: For assembly and repair, including spared items, PWB assembly standards such as ANSI/EIA/IPC/J-STD-001[21] and PWB repair standards such as ANSI/IPC-R-700[22] should be used. Forming leads of non-surface mount components to be soldered as surface mount device leads should be used with extreme caution for assembly and repair of military equipment. The non-standard lead forming required by this mounting technique induces undesired stresses at the lead to body interface of HSMs and PEMs and could contribute to latent solder, lead, and body failures for HSMs and PEMs.

Assure that PWB signal trace cross sections are controlled during the etching process for critical impedance traces since small differences in etchback can greatly impact the impedance of small cross section traces. Problems with etchback may require changes to the dielectric separation and trace widths of the problem traces and PWB computer aided design parameters may have to be revised to ensure all traces meet design requirements.

Control dry-pack and nitrogen storage to assembly time for PEMs. Moisture induced stress sensitivity classification of PEMs per ANSI/IPC-SM-786 is shown in the following table. EIA JESD-22-A112 can also be used as a guide. A typical PEM would be rated as a Class 4 device and Class 6 must be assumed if the classification level of a PEM is not known.

Moisture Sensitivity Classification Level of PEMs	Floor Life (Out of Bag)
1	Unlimited at ≤ 30C/90% RH (Relative Humidity)
2	1 Year at ≤ 30C/60% RH
3	1 Week at ≤ 30C/60% RH
4	72 Hours at ≤ 30C/60% RH
5	24 to 71 Hours at ≤ 30C/60% RH (Specified on Label)
6	6 Hours at ≤ 30C/60% RH

Control solder preheat ramp time since rapid vaporization of trapped moisture in a PEM can result in delamination at various material interfaces, package deformation, e.g., "doming" or "popcorning," and venting through cracks in the epoxy molding compound and material interfaces. An audible venting is also referred to as "popcorning." Delamination is a reliability problem since the device may meet performance requirements after assembly, but contaminants such as fluxes and cleaning residues can enter the package through cracks and voids and may be augmented by capillary action and can

[21] ANSI/EIA/IPC/J-STD-001: Use Class 3 for high reliability military equipment, Class 2 for non-tactical military equipment, and Class 1 for general/consumer/COTS equipment.
[22] ANSI/IPC-R-700: Use Class 3 for high reliability military equipment, Class 2 for non-tactical military equipment, and Class 1 for general/consumer/COTS equipment.

contribute to latent corrosion induced failures. Delamination at the material interfaces can affect the thermal paths in the package and result in an increased die temperature thereby lowering the MTBF of the device. High temperature soldering operations typically range from 230C to 260C or even as high as 300C and the maximum lead temperature for soldering depends on the package and die used and ranges from about 260C to 300C for either 10 seconds or 60 seconds. Therefore, a typical soldering setup would limit the lead temperature to 260C for 10 seconds to assure the parts most sensitive to lead temperature are not harmed. Additional PEM stresses can result from soldering operations since soldering temperatures are above the typical 155C to 165C glass transition temperature of most epoxy molding compounds and result in dramatic increases of the epoxy molding compound temperature coefficient of expansion and in material leaching, particularly from the flame retardants.[23] MIL-HDBK-179 states that some questions remain regarding toxic fumes liberated from packages exposed to excessive temperatures.[24]

After assembly, perform quality conformance inspection tests. Testing must include non-destructive inspection, e.g., X-ray or CSAM, to check for cracks, voids, and delaminations and electrical testing to assure that all performance requirements are met. Latent corrosion and delamination failures can still occur even if the assembly passes all quality conformance inspections. Some testing should be reserved and some repeated after dehydration bake and conformal coating (see following paragraph). Quality assurance and design personnel should determine the most beneficial assembly and testing flow for each assembly and if testing at temperature extremes is required.

Dehydrate bake assembly (typically, 24 hours at 125C) to assure that the total absorbed moisture level in the PEMs is less than 0.05% of the total package weight. A total absorbed moisture level of 0.11% of the total package weight is a recommended maximum limit (see ANSI/IPC-SM-786). After baking, apply a parylene conformal coating (see Conformal coating). The assembly should be placed in dry-pack packaging (desiccant and moisture indicator card in package), or nitrogen storage if application of the conformal coating is to be delayed more than the amount of time allowed per the highest moisture sensitivity classification level of the PEMs used.

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[23] William L. Schultz and Sheldon Gottesfeld, Harris Semiconductor. "Reliability Considerations for Using Plastic-Encapsulated Microcircuits in Military Applications," *Applications Envelope for PEMs*. Online. 1994. Available: http://rel.semi.harris.com/docs/rel/PEM/Mil_plas_13.html#HEADING12. [8 August 1997].

[24] MIL-HDBK-179A, 20 July 1995, Section 6.4 Plastic Encapsulated Microcircuits (PEMs), paragraph 6, page 26.

Conformal coating: Moisture ingression in PEMs can be reduced by the application of a MIL-I-46058 or IPC-CC-830 conformal coating. MIL-I-46058 coating types are AR (Acrylic Resin), ER (Epoxy Resin), SR (Silicone Resin), UR (polyUrethane Resin), and XY (paraXYlylene (parylene)). Urethane and parylene coatings have low moisture permeability with parylene being preferred due to its lower moisture permeability and its ability to cover sharp edges and transitions and to penetrate into PWB and PEM pinholes and cracks.[25] MIL-I-46058 coating thickness for types AR, ER, and UR is 0.002" ± 0.001" (accuracy of ± 0.0005"), for type SR is 0.005" ± 0.003" (accuracy of ± 0.0005"), and for type XY is 0.0006" ± 0.0001" (optically measured with a typical accuracy of ± 5%). Typical thickness for UR is 0.003" ± 0.002" and for XY is 0.001" ± 0.0005" (typical maximum thickness is 0.003").

At 25C, the thermal conductivity, 10^{-4} calorie/centimeter/C, of parylene is 2.0, epoxy is 4.0-5.0, silicon is 3.5-7.5, and urethane is 5.0, i.e., the thermal conductivity of parylene coating is two to four times less than epoxy, silicone, and urethane resin coatings.[26] Since the thickness of parylene coatings are usually one-quarter to one-half as thick as standard coatings the effective thermal resistance as compared to standard coatings may be about the same, but must be addressed for each use.

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[25] Nick Virmani, NASA Electronic Packaging and Processes Branch. "Understanding The Effectiveness of Parylene Coatings in The Protection of Plastic Encapsulated Microcircuits and Assemblies From Moisture Initiated Failure Mechanisms." Online. 31 March 1995. Available: http://arioch.gsfc.nasa.gov/312/parylene/pems.html. [8 August 1997].

[26] Nick Virmani, NASA Electronic Packaging and Processes Branch. "Understanding The Effectiveness of Parylene Coatings in The Protection of Plastic Encapsulated Microcircuits and Assemblies From Moisture Initiated Failure Mechanisms," *Table 5: Thermal Properties of Parylene C.* Online. Available: http://arioch.gsfc.nasa.gov/312/parylene/nv-tab5.gif. [8 August 1997].

SUMMARY

MIL-HDBK-179 can be used for guidance in the selection of microcircuits for military equipment and the use of PEMs must be addressed on a case-by-case basis. Characterization of PEM types and vendors must be done to support the unique military environment over long periods of time. More standardization for PEMs is required, i.e., industry standard drawings comparable to SMD drawings are needed. Use of PEMs in military equipment must address the issues stated within this paper and particular attention should be given to storage requirements for production and repair facilities and assembly/repair environments, and operating and storage environments for fielded equipment. The primary concern is moisture ingression in PEMs and the resultant problems that occur during storage, assembly, and operation of the affected parts. Use of a conformal coating, especially a parylene conformal coating, on assemblies which use PEMs can lower moisture ingression to more acceptable levels. Substitution of PEMs in place of HSMs must also take into account the higher thermal resistance of PEMs versus HSMs and the resulting change to the junction temperature which affects thermal derating and reliability calculations.

ABBREVIATIONS AND ACRONYMS

θ_{CS}: Case-to-Sink thermal resistance
θ_{CA}: Case-to-Ambient thermal resistance
θ_{JA}: Junction-to-Ambient thermal resistance
θ_{JC}: Junction-to-Case thermal resistance
θ_{SA}: Sink-to-Ambient thermal resistance
AEC: Automotive Electronics Council
AMCOM: Aviation and Missile Command (formerly MICOM)
ANSI: American National Standards Institute
ARO: After Receipt of Order
C: Centigrade/Celsius, degrees
CALCE: Computer Aided Life Cycle Engineering EPRC, University of Maryland[27]
CERDIP: CERamic Dual In-line Package
COTS: Commercial Off-The-Shelf
CSAM: C-mode Scanning Acoustic Microscope
DESC: Defense Electronics Supply Center (now DSCC)
DSCC: Defense Supply Center Columbus (formerly DESC)
DSP: Digital Signal Processor
EIA: Electronic Industries Association
EPRC: CALCE Electronic Packaging Research Center, University of Maryland[28]

[27] University of Maryland CALCE EPRC Internet Web Site. Online. Available: http://www.calce.umd.edu. [8 August 1997].

HAST: Highly Accelerated Stress Test
HSM: Hermetically Sealed Microcircuit
IIPEC: Institute for Interconnecting and Packaging Electronic Circuits
IPC: Interconnections Packaging Circuitry (see IIPEC)
JEDEC: Joint Electronic Device Engineering Council of the EIA
JEP: EIA JEDEC Publication
JESD: EIA JEDEC Standard
J-STD: Joint Standard
LCC: Life Cycle Cost
MICOM: Missile Command, United States Army (now AMCOM)
MTBF: Mean Time Between Failure
NASA: National Aeronautics and Space Administration
PAC-3: PATRIOT Advanced Capability-3
PATRIOT: Phased Array TRacking to Intercept Of Target
PCPP: Parts Control Program Plan
PDIP: Plastic Dual In-line Package
PDR: Preliminary Design Review
PED: Plastic Encapsulated Device
PEM: Plastic Encapsulated Microcircuit/Microelectronic
PSIG: Pounds per Square Inch Gauge
PUB: Publication
PWB: Printed Wiring Board
RH: Relative Humidity
RL: Rome Laboratory[29]
SMD: Standardized Military Drawing
T_A: Ambient Temperature
T_C: Case Temperature
T_J: Junction Temperature

[28] University of Maryland CALCE EPRC Internet Web Site. Online. Available: http://www.calce.umd.edu. [8 August 1997].
[29] Rome Laboratory Internet Web Site. Online. Available: http://erd.rl.af.mil. [8 August 1997].