

ELECTRONIC DESIGN

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Close The Information Gap On IC-Package Reliability

Before Engineers Can Take Advantage Of Advanced IC Packages, They Must Have A Clear Understanding Of Their Relative Merits.

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To date, surface-mount packages, whether J-lead or gull wing, have been key enablers in the drive to reduce the overall size of electronic systems and devices. Despite the maturity of this technology however, increasing pressure to enhance reliability, increase functionality, and reduce size while lowering costs has kept researchers and designers permanently at the drawing board.

The current answers to these challenges are surface-mount (SMT), package options that can be loosely divided into two groups: ball-grid arrays (BGAs) and chip-scale packages (CSPs). While both of these technologies have been around for a number of years, their relatively high cost has relegated them to only the most space-constrained applications. Now, the pressure many designers face to reduce system dimensions has brought about a gradual migration toward these newer packages.

Unfortunately, other major obstacles to the adoption of these technologies still exist. The very nature of these packages means that reliability is questionable and that conventional testing and rework methods no longer apply. Also, the competitive nature of the high-end IC business is such

that many package/IC houses are loathe to divulge the exact failure rates of their package design. As a result, mistakes will be repeated, thereby slowing progress. In addition, the plethora of package options causes some confusion for designers who must choose from among them. Their decision is further hampered by the limited time they have to perform extended reliability and performance testing, thanks to ever-present time-to-market pressure.

As a result of all this, the Jet Propulsion Laboratory (JPL), Pasadena, Calif., undertook the task of performing extended, independent, performance and reliability testing of SMT packages, using the two categories outlined above (regular SMT BGAs and CSPs). Working for NASA, JPL is one of the few facilities that can independently test the devices over a long period of time without time-to-market pressures. While still a work-in-progress, test results are available, along with information on lessons learned from the design, manufacturing, inspection, and reliability of these assemblies.

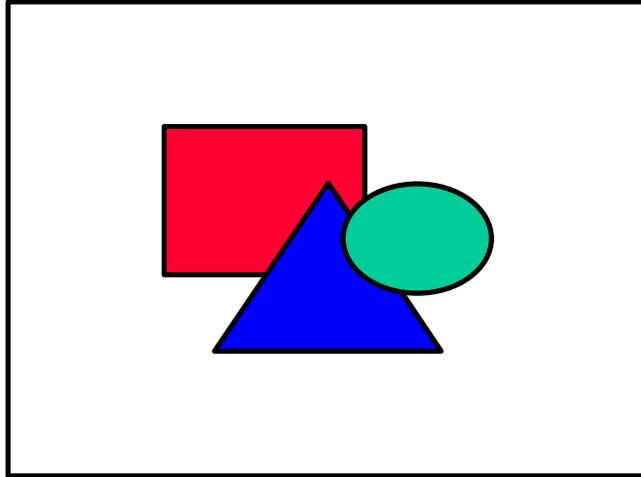
A review of the board-level reliability of CSP assembly and the projected values for specific environmental conditions were extracted from the data. These findings offer valuable information on package robustness, and provide a better understanding of the challenges associated with the implementation of SMT technology, particularly with the new, advanced, miniature CSPs.

Miniaturization Trends

SMT electronic packages are mounted directly onto the board surface, as opposed to the insertion of leads into plated through-holes (PTHs). While SMT come in several different package styles, they can generally be divided into two categories: those with terminations of leads on the periphery of the component on two or four sides, called peripheral-array packages (PAPs), and those with terminations (either pads or solder bumps) over much of the bottom of the component, called area-array packages (AAPs). PAPs have less potential for significant size reduction with increased I/O counts, compared to AAPs. The BGAs from the latter category are now the mainstay alternative to PAPs. For example, the CSP version of the two-sided PAP is the lead-on-chip (LOC) package, and the versions for AAPs are micro- (or mini-) BGA packages, which generally use eutectic solder balls.

Another level of miniaturization is accomplished by directly attaching the bare die to the printed wiring board (PWB). The direct flip-chip on board (FCOB) is the ultimate miniaturization level, achieving a die-to-PWB footprint ratio of nearly 70%. In FCOBs, solder bumps are permanently attached to the face of bare die, and the flip side is mounted on the PWB. In chip-on-board packages, with about 50% use-of-area efficiency, the pads of the wire-bonded die are used for second-level wire bonding onto the PWB.

Projections regarding the use of these packages are significantly different, with the numbers dependent on the market source. One projection from the British Packaging Association (BPA), U.K., is shown in **Figure 1**.



1. Projections regarding the use of the many available package options are significantly different. What is clear, however, is that user demands for higher speed and more functionality will help advanced packages, such as BGAs and CSPs, to steadily encroach upon the well-established DIP's market share. In addition, the projection for BGAs indicates that perhaps these packages were only an interim solution; the stepping stone for the industry's wider acceptance of flip-chips and CSPs.

Several trends are apparent. The dual-in-line package (DIP) shows the most reduction in use, decreasing from 16 billion in 1996 to about five billion over 10 years (roughly one billion fewer per year). In contrast, the use of surface-mountable packages including quad flat packages (QFPs) is expected to increase in the next decade. The increase for plastic QFPs is forecast to be from seven to 18 billion within the first five years, and will almost plateau with an increase of only two billion for another five years. Within 10 years, the flip-chip-on-board package (FCOB) is forecast to increase from five to 13 billion.

The rate of increase in the use of CSP and flip-chip packages is the same. Both are projected to reach up to six billion production units by the year 2006. In contrast, the expected increase for BGAs for the next 10 years is minimal, reaching a total production demand of only 1.5 billion. The projection for BGAs suggests that these packages were only an interim solution, that the devices are a stepping stone for the industry's wider acceptance of flip-chip and chip-scale packages that better meet the demands for denser and lighter miniaturized applications.

System Approach

To meet the mission requirements or to bring a product into market successfully, many factors must be considered. Concurrent engineering approaches, which consider multifaceted areas of technology and the interaction among the various engineering disciplines, are key to meeting these objectives. Areas that must be included are:

- * Design for manufacturability
- * Design for testability
- * Design for quality and reliability

A similar approach could be used when a subsystem of electronic assemblies is being investigated. The internal JPL teaming arrangement for SMT technology evaluation, as well as the industry-wide consortium of BGA and MicrotypeBGA follow the same idea of a concurrent-engineering approach. This approach has been extended here to include various aspects of electronic attachment, including manufacturing and design, for reliability from conventional SMT packages to emerging CSPs.

Attachment Approaches

To connect I/O signals from the package to a subsystem of electronic hardware, the package is attached to a printed wiring board (PWB). The attachment can be accomplished by various techniques, including insertion, plated-through hole, surface mounting, and adhesive bonding. Here, we will focus on soldering.

Generally, packages are attached by soldering the leads (castellation or endcaps for leadless packages, balls for grid arrays) to the PWB. In the SMT application, solder has both electrical and mechanical functions. As a result, damage to the solder could easily affect the functional integrity of the system. Therefore, an analysis of the defects that cause changes, either in mechanical or electrical system characteristics, is critical.

The most common damage found in solder joints is induced by thermocycling--differences in thermal expansion of package and PWB materials. This is especially true for eutectic solder (63 Sn/37 Pb) which creeps at room temperature. Creepage generally occurs at temperatures above one-half the absolute melting temperature ($T/T_m > 0.5$). This value is 0.65 at room temperature for eutectic solder. Creepage and stress relaxation are the main causes of cycling damage. The primary source of damage in package attachment is caused when the system temperature changes. Damage to solder joints is most often caused by stress induced by the global coefficient of thermal expansion (CTE) differences between the package and board, and local CTE differences between solder attachments to components and the PWB. The package and board can also have temperature gradients through the thickness and at surface areas.

Reducing CTE differences between the component and the PWB reduces cycling damages, but the ideal condition depends on the thermal conditions of the components, the PWB, and the solder. An ideal condition could be the selection of PWB materials which have a slightly higher CTE than the components. This is based on the assumption that the global CTE is generally dominant, and that the component is hotter than the PWB.

There are other approaches that can be taken to help reduce damage to solder joints. Underfill application is a common technique which has been widely used for either the direct attachment of a chip to a board, or when package leads are not robust. Other, less-conventional approaches are aimed at absorbing CTE mismatches between the die and board, either internally or externally. These methods use strain-absorbing mechanisms, which reduce stresses on the solder-joint interconnect. These approaches have a tendency to introduce their own unique damage, because the weakest link is now transferred from the solder joint to other areas of the attachment system.

Conventional SMT

The program at JPL focused on the use of SMT for high-reliability, ultra -low-volume spacecraft

electronics, as used in the NASA community. Various aspects of the technology were investigated and documented, including an initial survey and research on the design, modeling, manufacturing, test, and deployment (aging) cycles. Findings from the survey and reliability results for conventional packages are discussed here:

- * Coplanarity is extremely critical for leaded packages.
- * The assembly defects most reported by the QA SMT survey are: insufficient solder, no solder, and poor wetting.
- * Dewetting is the single most important feature that an inspector should flag.
- * Paste qualification tests, inspection following the paste print, part placement, and after-solder-reflow inspections are critical to assure joint integrity.
- * Manufacturing analysis tools such as Design of Experiment (DOE) and Statistical Process Control (SPC) are generally used to track solder defects and defect type and location. Generally, there is no formal method of tying these defects back to the manufacturing procedures.

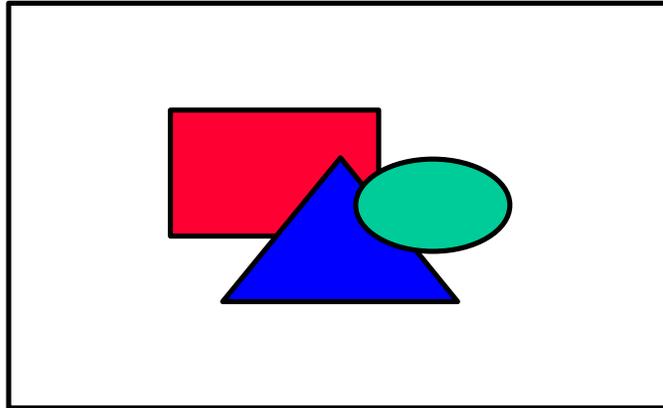
JPL concludes that the leading causes of SMT rejects are solderability and solder-paste deposition problems.

SMA Reliability Evaluation

The surface-mount assembly (SMA) test vehicles involved the use of a single ceramic component, with a 0.050-in. pitch, soldered to an epoxy-fiberglass, FR-4 board. LCCs, J-lead cerquads, and gull-wing cerquads were the SMT components. Test vehicles were subjected to a thermal-cycle profile with long duration to ensure near-complete creeping. This long-duration cycle started at 25°C, with a decrease rate of 2°C/min. to -55°C, and with an oven-dwell setting of 45 min. The temperature was increased to 100°C at a rate of 2°C/min., with an oven-dwell setting of 45 min., followed by a decrease in temperature to 25°C. The duration of each cycle was 246 min.

SMA Test Results

The cycles-to-failure for 68-, 28-, and 20-pin LCC assemblies are ranked from low to high, and failure-distribution percentiles are approximated using a median plotting position [$F_i = (i - 0.3)/(n + 0.4)$] (**Fig. 2**). As expected, there was a large spread in cycles-to-failure due to the common variances associated with materials and manufacturing conditions. These parameters include solder-joint volume, quality of joint, and device location. The first failure for the 68-pin LCCs was detected at 53 cycles, while the last sample failed after 139, with 93 average cycles. The 28-pin LCCs failed at much higher cycles in the range of 352 to 908, with 660 average cycles. The 20-pin cycles-to-failure were in the same range as for those of 28-pins, and failed within 573 to 863, averaging 674 cycles.



2. The cycles-to-failure for 68-, 28-, and 20-pin LCC package assemblies are ranked from low to high, and failure-distribution percentiles are approximated for each using a median plotting position [$F_i = (i-0.3)/(n+0.4)$]. As expected, there was a large spread in cycles-to-failure due to the common variances associated with materials and manufacturing conditions, including solder-joint volume, quality of joint, and location.

If only distances to neutral points (DNPs) are to be considered, then it should be noted that the cycles-to-failure is directly proportional to the DNP. With this in mind, then it would be reasonable to assume that the 20-pin LCCs, which have a shorter DNP than the 28-pin devices, should have failed at higher cycles. However, cycles-to-failure is also inversely proportional to the effective solder-fillet height. The solder-fillet heights for 20- and 28-pin LCCs were 0.021 and 0.033 in., respectively. The lower height for a 20-pin LCC results in higher shear strain for the same CTE-mismatch displacement. The difference in part sizes could have been offset by the difference in the fillet heights.

All 68-pin gull-wing assemblies failed at much higher cycles. Assemblies with Kovar-alloy leads failed between 1720 cycles and about 3750 cycles (*Fig. 2, again*). Gull wings with Alloy 42 leads failed at higher cycles. The testing of the J-leads still continues, and as of March 1998, has reached more than 5000 cycles. This includes several hundred -55° to 125°C cycles. Most of the J-leads have now failed, and are being checked for failure locations.

BGA Technology

To address the many common quality and reliability issues of BGAs, JPL organized a consortium with sixteen members in early 1995. The diverse membership, including individuals from the military, commercial, academia, and infrastructure sectors, permits a concurrent engineering approach to resolve many challenging technical issues.

BGA is an important technology for higher pin counts, without the attendant handling and processing problems of the peripheral leaded packages. BGAs also are robust during processing due to their higher pitch (0.050 in., typical), better lead rigidity, and self-alignment characteristics during reflow.

A BGA's solder joints cannot be inspected and reworked using conventional methods, and the devices are not well-characterized for multiple, double-sided-assembly processing methods. In high-reliability SMT assembly applications, such as space and defense, the visual inspection of

solder joints has been standard practice and a key factor in providing confidence in solder-joint reliability.

Test-Vehicle Configuration

The two test-vehicle assembly types were plastic (PBGA) and ceramic (CBGA) packages. Both FR-4 and polyimide PWBs with six 0.062-in.-thick layers, were used.

Plastic packages covered the range from overmolded pad-array carriers (OMPACs) to SuperBGAs (SBGAs). They included:

- * Two peripheral SBGAs (352 and 560 I/Os)
- * A peripheral OMPAC (352 I/Os) and PBGAs (352 and 256 I/Os)
- * A depopulated, full-array PBGA (313 I/Os)
- * A 256-pin QFP with a 0.4-mm pitch

In an SBGA, the die is directly attached to an oversize copper plate. This design is intended to provide better heat dissipation than standard PBGAs. The solder balls for plastic packages were eutectic (63 Sn/37 Pb).

Ceramic packages with 625 and 361 I/Os were also included in our evaluation. Ceramic solder balls (90 Pb/10 Sn) with 0.035-in. diameters have a high melting temperature. They were attached to the ceramic substrate with eutectic solder (63 Sn/37 Pb). At reflow, package-side eutectic solder and PWB-side eutectic paste are reflowed to provide the electro-mechanical interconnects.

The plastic packages had dummy and daisy-chain patterns, with the daisy chains on the PWB designed to allow the monitoring of critical solder-joint regions. Most packages had four daisy-chain patterns, 560-I/O units had five, and the QFP had one.

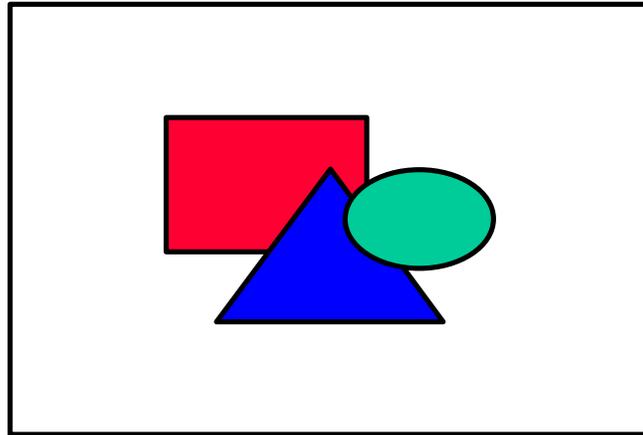
Thermal Cycling Of BGAs

Two significantly different thermal cycle profiles were used at two facilities. The cycle A condition ranged from -30° to 100°C, and had an increase/decrease heating rate of 2°C and a dwell of about 20 min. at the high temperature. This ensured near-complete creeping. The duration of each cycle was 82 min. The cycle B condition ranged from -55° to 125°C. It also could be considered a thermal shock because it used a three-region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear, and varied between 10° to 15°C/min., with dwells at extreme temperatures of about 20 min. The total cycle lasted approximately 68 min. BGA test vehicles were continuously monitored through a LabView system at both facilities.

The criteria for an open solder joint, as specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life. In several instances, a few non-consecutive early interruptions were not followed by additional interruptions until significantly later stages of cycling. This occurred more frequently with plastic packages.

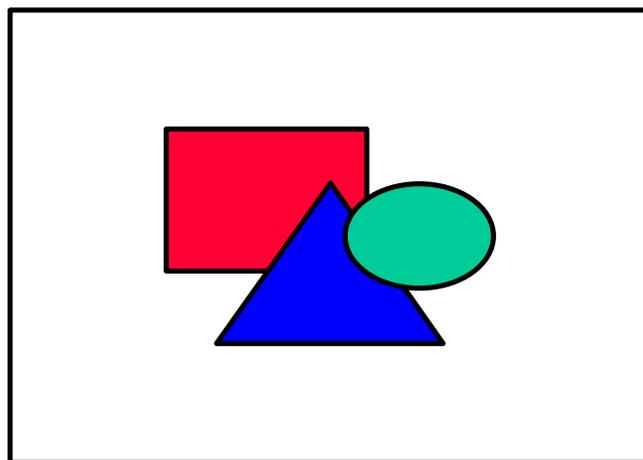
Damage Monitoring

Both board- and package-interface cracking were observed with an increasing number of cycles (*Fig. 3a and b*). Failure under the A-cycle conditions were generally from the PWB. In the case of the B-cycle conditions, failures came from the package sites. Failure-mechanism differences could be explained by global or local stress conditions. Modeling indicates that the high-stress regions shifted from the board to the packages when stress conditions changed from the global to local. The A cycling, with slow heat/cooling ramping, allowed the system to reach a uniform temperature. Damage could therefore indicate a global stress condition. Damage during the B cycle, with rapid heat/cooling, could indicate a local stress condition.



3. The cross-section of failure sites for the CBGA 625 after 350 cycles shows both board (a) and package (b) interface cracking. Failure-mechanism differences could be explained by global-or local-stress conditions. Modeling indicates that the high-stress regions shifted from the board to the package when conditions changed from global to local.

Among the plastic packages, the PBGA 313, with depopulated full-array balls, was the first to fail under both the B and A thermal-cycling conditions. Various cross-sections of this package's solder balls from corner to the center at 4682 A cycles are shown in **Figure 4**. These photos represent the balls under the die where most damage occurs due to local CTE mismatches. Photos, with and without voids, were also included for comparative analysis.



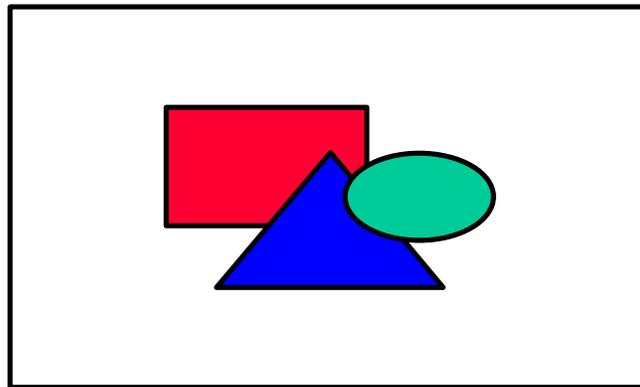
4. Among the plastic packages tested, the PBGA 313, with depopulated full-array solder

balls, was the first to fail under both B and A thermal-cycling conditions. After the completion of 4682 cycles, the balls under the die see most of the damage due to local CTE mismatches. Voids appear to have concentrated at the package interface under the die.

Voids appear to have concentrated at the package interface under the die. Cracking propagation occurred at package or board interfaces for sections with or without voids. The sections with voids were opens, as indicated by the seepage of mounting materials into voids. Except for the interface-connecting cracks, there appeared to be no crack propagation among the voids.

BGA Thermal Cycling Results

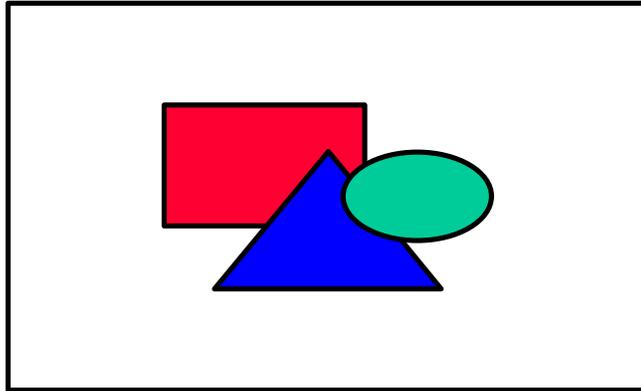
Cycles to first failure for PBGA 313 and SBGA 352 subjected to B cycling for assemblies on polyimide and FR-4 PWBs can be seen in **Figure 5**. The most current PBGA 313 assemblies that failed under cycle-A conditions are also included in the plots for comparison. These assemblies include those reflowed with low, standard, and high solder-paste levels.



5. A graph of cycles versus cumulative failure percentages for first failure of PBGA 313 and SBGA 352 packages subjected to B cycling for assemblies on polyimide and FR-4 PWBs shows their relative advantages. The most current PBGA 313 assemblies that failed under cycle-A conditions are also included in the plots for comparison. These assemblies include those reflowed with low, standard, and high solder-paste levels.

Why CSPs?

Defined as packages that are up to 1.2 to 1.5 times larger than the perimeter or the area of the die, CSPs combine the small size and performance of the bare die or flip-chip, with the advantages of standard die packages. The technology competes with bare-die assemblies, and is now at the stage that BGAs were about two years ago. Many manufacturers now refer to the CSP as a miniature version of the previous generation. There are two types of CSPs: those with flex or rigid interposers, and those based on wafer-level molding and assembly redistribution (*Fig. 6*).



6. Defined as packages that are up to 1.2 to 1.5 times larger than the perimeter or the area of the die, CSPs come in two types--those with a flex or rigid interposer, and those based on wafer-level molding and assembly redistribution.

The CSP packaging accomplishes many purposes, including:

- * Provision of solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes.
- * Redistribution of the tight pitch of the die to the pitch level within the norm of PWB fabrication. The small size of CSPs does not allow significant redistribution, and the current, cost-effective, PWB fabrication limits full adoption of the technology, especially for high I/O counts.
- * Protection of the die from physical and alpha radiation damages, and dissipation of thermal energy.
- * Overall simplification of die-functionality testing.

Self-Alignment

CSPs can be categorized into grid arrays and leads (or no leads). The mini- (fine-pitch) grid arrays can accommodate higher pin counts, and, as in the case of BGAs, they have self-alignment (centering) characteristics. For BGAs, the ease of package placement requirements has been widely published as one of their attributes. This feature reduces the number of solder-joint defects to lower levels than conventional SMT packages. Grid CSPs have self-alignment characteristics, but there is disagreement on the best offset limits.

Reliability Of SMTs And CSPs

For comparison, projected cycles-to-failure for low-count CSPs as well as SMT assemblies were gathered from literature, and projected from a modified Coffin-Manson relationship. Board reliabilities of most CSP packages were found to be comparable or better than their LCC counterparts. These packages, however, are not as robust as leaded packages, including the popular gull wing and J-lead versions of these.

Lessons And Recommendations

Conventional SMT

- * CTE differences between the package and board are the key factors affecting solder-joint failure by thermal cycling. Creep and stress relaxation are main causes of cycling damages.
- * Package size and CTE, as well as the CTE absorption capability (e.g., leaded springiness versus no lead) are key factors that define solder-joint reliability.
- * The leadless ceramic packages with 68 terminations showed the lowest cycles-to-failure, followed by 28 and 20 terminations.
- * Both 68-pin QFPs and J-leads showed an order of magnitude higher number of cycles-to-failure than the leadless packages.
- * Solder volume affects joint reliability, and must be controlled during the manufacturing process prior to part placement.
- * The leadless packages with 20 and 28 terminations showed the same range of cycles-to-failure. The 28-termination version had higher solder volume (stand off). Cycles-to-failure increases with solder volume, but decreases with package size.
- * J-leads showed higher cycles-to-failure than QFPs.
- * QFPs with Alloy 42 lead materials showed higher cycles-to-failure than those with the Kovar materials.
- * Lead planarity requirements for fine-pitch packages are much more stringent than for plastic or ceramic BGAs.
- * Solder joints with signs of dewetting must be rejected.

BGA packages and assembly

- * BGA ball planarities were dependent on package type, but irrespective of package type, decreased as the size decreased.
- * Ceramic packages showed lower warpage and were more coplanar than their PBGA counterparts. Numerous ceramic packages had tilted solder balls.
- * Solder-ball planarities were significantly higher for plastic than for ceramic packages.
- * PBGAs are more robust in accommodating package nonplanarity than ceramic packages; PBGA balls collapse during reflow processes, whereas CBGAs do not.
- * Solder volume controls for ceramic BGA packages are more critical than for plastic BGA packages.
- * The BGA assembly void levels were the same as those generally observed by industry (less than 20%).
- * BGAs were robust in assembly, compared to the 256-pin, fine-pitch, 0.4-mm QFPs. All QFPs

showed bridging to some degree, and had to be reworked.

- * Voids can be introduced if an improper reflow profile is used for a specific solder paste. Dwell temperature and time are two key factors that affect void levels.

- * Voids for plastic BGAs were much higher, and generally concentrated at the package interface.

- * Rosin mildly activated (RMA) and water-soluble reflow profiles evaluated in this study were significantly different and optimized separately for the applications.

- * Ceramic BGAs failed much earlier than their plastic counterparts due to their much larger CTE mismatch on FR-4/polyimide boards.

- * Cycles-to-electrical-failure for ceramic BGAs depended on many parameters including cycling temperature range and package size (I/Os).

- * Ceramic packages with 625 I/Os were the first to show signs of failure among the ceramic (CBGA 625 and CBGA 361) and plastic packages (SBGA 560, SBGA 352, OMPAC 352, and PBGA 256) when cycled to different temperature ranges.

- * Joint failure mechanisms for assemblies exposed to two cycling ranges at two facilities were different.

- * Ceramic assemblies cycled in the range of -30°C to 100°C showed cracking initially at both interconnections, with final separation generally from the board side through the eutectic solder. The board-side joints showed signs of pin-hole formation prior to cracking and complete joint failure.

- * The failure mechanisms for ceramic BGAs that were cycled in the range of -30° to 100°C were similar to those reported in literature for 0° to 100°C thermal cycles.

- * Ceramic and plastic BGAs showed different failure mechanisms, as evidenced from the total number of electrical interruptions with more cycles.

- * The CBGA's first electrical interruption (open) was followed by consecutive additional interruptions, whereas the PBGA's was not followed by additional interruptions until a much higher number of cycles.

- * The PBGAs with 313 I/Os, depopulated full arrays, were first among the PBGAs to fail within both cycling ranges.

- * The 352 SBGA, with no solder balls under the die, showed much higher cycles-to-failure than the PBGA 313.

- * For cycles with a 125°C maximum temperature, plastic package assemblies (PBGA 313 and SBGA 352 on polyimide) generally failed at a higher number of cycles than those on FR-4.

CSP assembly reliability

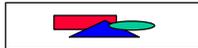
- * The board-level reliabilities of most CSP packages are comparable to, or better than LCCs with similar I/O counts. These packages, however, are not as robust as leaded packages, including gull

wing and J-leads.

* Grid BGAs and CSPs align themselves during the reflow process and, therefore, some misalignment is acceptable. Acceptable misalignment depends mainly upon package type, size, ball material, and weight.

Dr. Reza Ghaffarian has nearly 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering disciplines. At JPL, Reza supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored over 50 technical papers, and has numerous patentable innovations. He received his M.S. in Electrical Engineering in 1979, and his Ph.D. in engineering in 1982 from UCLA.

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