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PLASTIC ENCAPSULATED MICROCIRCUIT (PEM)
DERATING, STORAGE AND QUALIFICATION REPORT

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1.0 **INTRODUCTION**

Plastic Encapsulated Microcircuits (PEMs) have been a consideration for military/space use for about thirty years. Early in the development of PEMs, silicon and the epoxy molding compounds (EMCs) had several shortcomings and left a lot to be desired from reliability point of view. Moisture, which is present in most military/space applications, had a devastating impact on the early PEMs due to the impurities in the EMCs. These failures did not originate from an electrical standpoint (die level) but were chemical or mechanical in nature. The typical failure mechanism seemed to revolve around Kirkendall voiding (see Fig. 1). Kirkendall voiding, or purple plague, is the formation of voids in wire bonds caused by the intermetallic formation between the gold bond wires and the aluminum bond pads. This intermetallic formation between gold and aluminum is significantly accelerated in the presence of an encapsulant contaminant, such as certain halides (chlorine, bromine, fluorine), moisture and elevated temperatures. This voiding is normally considered an end of life failure mechanism. Other random failure mechanisms occur and are usually lot or manufacturer dependent. These failures are detailed later in this report. In PEMs process improvements, EMCs have evolved over time. This evolution has made PEMs more reliable; however, reliability is still a concern, when considering usage of PEMs in military/space systems.

This report will review general derating storage and qualification guidelines for PEM devices. Also included in this report is some test data (from 1996-1999) that Naval Surface Weapons Center (NSWC) Crane, Indiana, has completed on some PEM lots [1].

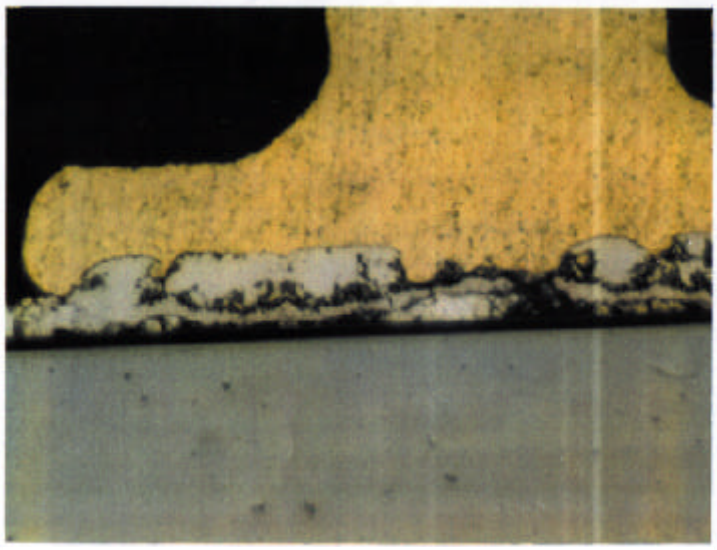

Figure 1. A sample of Kirkendall voiding

2.0 DERATING GUIDELINES

Derating is the method of reducing stress and/or making numerical allowances for functional degradation in microcircuit performance. Commercial parts used in military/space applications may need to be derated more conservatively than military parts. The microcircuits must meet the performance and reliability criteria established for their application when used in military/space applications. When using microcircuits of different temperature ranges, reliability levels, and performance characteristics, it is crucial to derate them properly. Two methods of derating are: (1) by reducing heat and electrical stress, and (2) by compensating for functional loss. Heat and electrical stress derating are applied to the voltage, current, and power stresses of the microcircuit. Functional loss and/or performance degradation over the part's life requires a degree of parametric derating. Derating should be applied knowledgeably and only enough to improve reliability, and only once throughout the application cycle. The severity of an application and its environment may require an additional degree of derating.

Tables 1 through 5 detail the type (technology-product), package (hermetic or plastic), deration parameters, and maximum allowable limits (percentage and/or temperature) of operation (in specific environment) for the microcircuits.

Table 1. Digital MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment		
Digital	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
MOS	Hermetic	Supply Voltage	/3	/3	/3
		Frequency	90%	90%	90%
		Output Current	90%	85%	80%
		Fanout	100%	90%	90%
		Junction Temperature (T_J)	125°C	110°C	100°C
	Plastic 1/	Supply Voltage	/3	/3	
		Frequency	90%	80%	
		Output Current	90%	80%	
		Fanout	100%	90%	
		Junction Temperature (T_J)	90°C	85°C	
	Plastic 2/	Supply Voltage	/3		
		Frequency	80%		
		Output Current	70%		
		Fanout	80%		
		Junction Temperature (T_J)	70°C		
Bipolar	Hermetic	Supply Voltage	/3	/3	/3
		Frequency	100%	90%	85%
		Output Current	90%	85%	80%
		Fanout	90%	85%	80%
		Junction Temperature (T_J)	125°C	110°C	100°C

Table 1 (Cont). Digital MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment		
Digital	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
	Plastic 1/	Supply Voltage	/3	/3	
		Frequency	100%	90%	
		Output Current	90%	80%	
		Fanout	90%	80%	
		Junction Temperature (T_J)	90°C	85°C	
	Plastic 2/	Supply Voltage	/3		
		Frequency	75%		
		Output Current	70%		
		Fanout	70%		
		Junction Temperature (T_J)	70°C		

Table 2. Linear MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment		
Linear	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
MOS	Hermetic	Supply Voltage	/3	/3	/3
		Input Voltage	80%	80%	70%
		Frequency	90%	90%	90%
		Output Current	90%	85%	80%
		Fanout	100%	90%	90%
		Junction Temperature (T_J)	125°C	110°C	100°C
	Plastic 1/	Supply Voltage	/3	/3	
		Input Voltage	80%	70%	
		Frequency	90%	80%	
		Output Current	90%	80%	
		Fanout	100%	90%	
		Junction Temperature (T_J)	90°C	85°C	
	Plastic 2/	Supply Voltage	/3		
		Input Voltage	60%		
		Frequency	80%		
		Output Current	70%		
		Fanout	80%		
		Junction Temperature (T_J)	70°C		
Bipolar	Hermetic	Supply Voltage	/3	/3	/3
		Input Voltage	80%	80%	70%
		Frequency	100%	90%	85%
		Output Current	90%	85%	80%
		Fanout	90%	85%	80%
		Junction Temperature (T_J)	125°C	110°C	100°C

Table 2 (Cont). Linear MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment		
Linear	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
	Plastic 1/	Supply Voltage	/3	/3	
		Input Voltage	80%	70%	
		Frequency	100%	90%	
		Output Current	90%	80%	
		Fanout	90%	80%	
		Junction Temperature (T_J)	90°C	85°C	
	Plastic 2/	Supply Voltage	/3		
		Input Voltage	60%		
		Frequency	75%		
		Output Current	70%		
		Fanout	70%		
		Junction Temperature (T_J)	70°C		

Table 3. Microprocessor MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment		
Microprocessor	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
MOS	Hermetic	Supply Voltage	/3	/3	/3
		Frequency	90%	90%	90%
		Output Current	90%	85%	80%
		Fanout	100%	90%	90%
		Junction Temperature (T_J)	125°C	110°C	100°C
	Plastic 1/	Supply Voltage	/3	/3	
		Frequency	90%	80%	
		Output Current	90%	80%	
		Fanout	100%	85%	
		Junction Temperature (T_J)	85°C	75°C	
	Plastic 2/	Supply Voltage	/3		
		Frequency	80%		
		Output Current	70%		
		Fanout	80%		
		Junction Temperature (T_J)	70°C		
Bipolar	Hermetic	Supply Voltage	/3	/3	/3
		Frequency	90%	80%	75%
		Output Current	80%	75%	70%
		Fanout	80%	75%	70%
		Junction Temperature (T_J)	125°C	110°C	100°C

Table 3 (Cont). Microprocessor MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment		
Microprocessor	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
	Plastic 1/	Supply Voltage	/3	/3	
		Frequency	80%	90%	
		Output Current	75%	80%	
		Fanout	75%	80%	
		Junction Temperature (T_J)	85°C	75°C	
	Plastic 2/	Supply Voltage	/3		
		Frequency	75%		
		Output Current	70%		
		Fanout	70%		
		Junction Temperature (T_J)	70°C		

Table 4. Microcircuit Memory MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment		
Memory	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
MOS	Hermetic	Supply Voltage	/3	/3	/3
		Frequency	100%	90%	90%
		Output Current	90%	85%	80%
		Junction Temperature (T_J)	125°C	110°C	100°C
	Plastic 1/	Supply Voltage	/3	/3	
		Frequency	100%	90%	
		Output Current	90%	80%	
		Junction Temperature (T_J)	90°C	85°C	
	Plastic 2/	Supply Voltage	/3		
		Frequency	80%		
		Output Current	70%		
		Junction Temperature (T_J)	70°C		
Bipolar	Hermetic	Supply Voltage	/3	/3	/3
		Frequency	100%	100%	90%
		Output Current	90%	85%	80%
		Junction Temperature (T_J)	125°C	110°C	100°C
	Plastic 1/	Supply Voltage	/3	/3	
		Frequency	100%	95%	
		Output Current	90%	80%	
		Junction Temperature (T_J)	90°C	85°C	
	Plastic 2/	Supply Voltage	/3		
		Frequency	80%		
		Output Current	70%		
		Junction Temperature (T_J)	70°C		

Table 5. GaAs Microcircuit Derating Guidelines

Type			Environment		
GaAs	**Package**	**Derating Parameter**	**Protected**	**Normal**	**Severe**
Digital	Hermetic	Channel Temperature	150°C	125°C	90°C
	Plastic 1/	Channel Temperature	125°C	90°C	
	Plastic 2/	Channel Temperature	90°C		

Notes for Tables 1-5
1/ Plastic packaged microcircuit with heat dissipation mechanisms (e.g. thermal fillers, thermal conductivity plate or a type of metal substrate) built-in.
2/ Low-power plastic packaged microcircuits with no heat dissipation mechanism other than through the leads.
3/ The supply voltage must be kept within the microcircuit specification sheets minimum and maximum limit.

3.0 STORAGE

PEM Moisture Sensitivity

Moisture inside a PEM turns to steam and expands rapidly when the package is exposed to the high temperature of vapor phase reflow, infrared soldering, or if the package is submerged in molten solder or wave solder. Under certain conditions, the pressure from this expanding moisture can cause internal delamination of the plastic from the chip and/or lead frame, internal cracks that do not extend to the outside of the package, bond damage, wire necking, bond lifting, thin film cracking, or cratering beneath the bonds. In the most severe case, the stress can result in external package cracks. This is commonly referred to as the “popcorn” phenomenon because the internal stress causes the package to bulge and often crack with an audible “pop”. Surface Mount Devices (SMDs) are more susceptible to this problem than the through-hole parts, because they are exposed to higher temperatures during reflow soldering. A reason for this phenomenon is that the soldering operation must occur on the same side of the boards as the SMD. For the through-hole parts, the soldering operation occurs under the board, which shields the parts form the chip or mount pad interface to the outside package surface, which has been identified as a critical factor in determining moisture sensitivity. Test method JESD22-A112-A, “Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices”, and JEP113A, “Symbols and Labels for Moisture Sensitive Devices”, can be used to assist in selecting and designing for PEMs applications. Inspection for post reflow soldering, often includes acoustic microscopy IAW JEDEC-STD-035,to help detect visually unseen, internal delamination occurring as a result of “popcorning" conditions.

All PEMs have a moisture sensitivity level, which are levels 1 through 6 (see JEP113A). Level 1 is the least sensitive to moisture and 6 the most. Through-hole PEMs are level 1-2, and surface-mount is usually a level 5-6. Even when the moisture sensitivity level is marked on the parts packaging, testing and/or monitoring should be performed. Test to JESD22-A112-A.

Evaluations have been performed on PEMs with sensitivity levels marked and they tested differently than the labeled level. A number of parts marked level 1 or 2 were actually level 6, following an evaluation of the parts. Unless level 6 is acceptable, testing-monitoring should be done until a level of confidence is met.

Microcircuit Storage

The discussion on storage needs to be separated into part storage and dormant application storage. Hermetically sealed microcircuits that were QPL, QML, or were military/space "Hi-Reliability" vintage, have been placed in storage for several years and used successfully. It has been proven that hermetically sealed parts can be stored as parts only, or in as application that sits dormant for years and then works. On the other hand, PEMs have not yet proven they can be stored for any given length of time. Commercial users do not normally store parts beyond a couple of months. Therefore, the military/space cannot rely on data from other industries to substantiate storage of PEMs. It has not been proven, but PEM part storage in a temperature controlled, clean and dry environment could probably be effective, for parts only, up to 7-8 years. The Navy uses PEMs in Sonobuoys that are stored for 5 years, and can be as long as 8 years. They allow a failure rate of 10%, which is not acceptable for most military/space applications.

4.0 PEM QUALIFICATION PLAN

The Component Engineering Branch from NSWC Crane along with NASA/GSFC, with inputs from private industry, has developed a PEMs qualification process that would be effective and cost efficient. The qualification test plan is outlined in Fig 2 and Fig 3. This qualification process involves an incoming inspection, construction analysis, preconditioning sequence (to simulate storage and assembly), and Highly Accelerated Stress Test (HAST). This process has been utilized in the PEM evaluation for TRIDENT Fire Control, TRIDENT Navigation, CEC, TACOM (Army Tank Command) and NAVSEA (parts derating document).

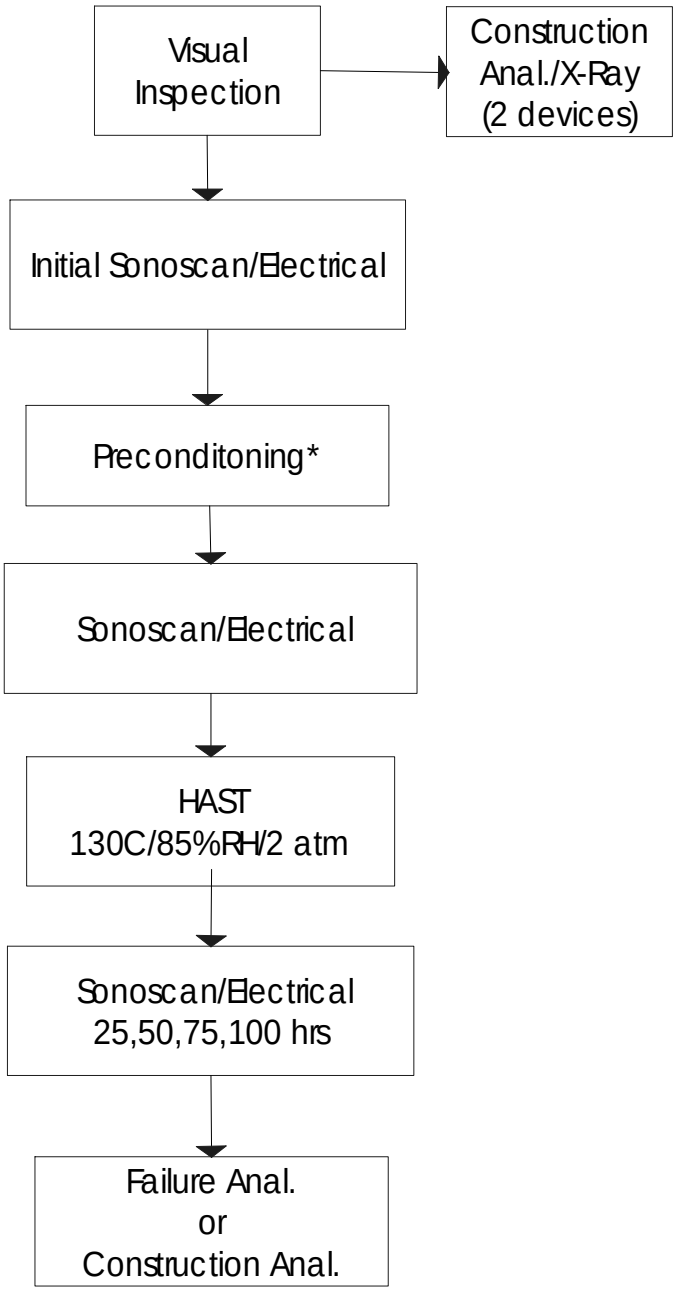

Figure 2. HAST qualification test flow

* Details of Preconditioning in Figure 3

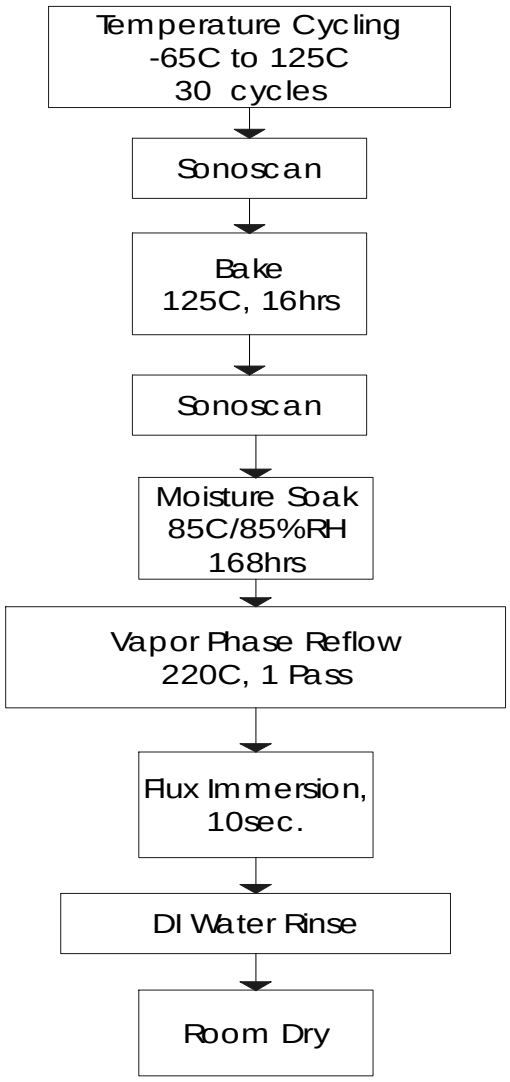

Figure 3. Preconditioning flow (Level 1 shown)

PEM LOTS EVALUATED

Table 6 represents the commercial components subjected to the PEM screening process shown in Figures 2 and 3. Several technologies with functionalities ranging from simple transistors to ASICs have been evaluated. Approximately, 64 component lots have been screened. Failures and/or other anomalies occurred in 19 of the lots. Chart 1 illustrates the PEM screening results based on the total number of lots tested. Table 7 details the failures and/or anomalies that were discovered. Out of the 19 lots in Table 7, eight part types were not recommended for use in military/space systems, and the remainder of the parts were considered to have some reliability risk. Two of the eight part types that were not recommended for use in military systems are special cases. The PLL clock driver supplied by manufacturer P and the VME Bus Interface supplied by manufacturer G are part types only supplied by these manufacturers. Therefore,

instead of a complete redesign, it was decided that these two part types be used even though there are known risks involved.

In PEMs applications, the package type and the manufacturer play an important part in determining the reliability of that part. For example, a part in a PLCC package is evaluated, passes electrically and exhibits acceptable construction practices. The results may not be true for the same part from the same manufacturer in a TQFP. PEM reliability is directly dependent on, but not limited to, the thickness of the encapsulant. Moisture sensitivity reliability concern is the key. If a PEM can stop, or at least slow down the ingress of moisture, the chances of it surviving in a military environment are much greater.

This qualification process does not only assess the component reliability in the system but also can determine the moisture sensitivity level of the component. The moisture sensitivity level is used by the assembler as a guideline for handling to reduce the possibility of component damage due to the combination of the ingress of moisture during storage and the extreme temperatures of the assembly process. There are six different moisture sensitivity levels, with level 1 not requiring special handling and level 6 requiring a 24-hour bake at 125°C prior to assembly. The preconditioning sequence of the PEM screening evaluation is beneficial in determining the moisture sensitivity level of a PEM. Examples of this concern are shown in the first two manufacturers "A" part types reported in Table 7.

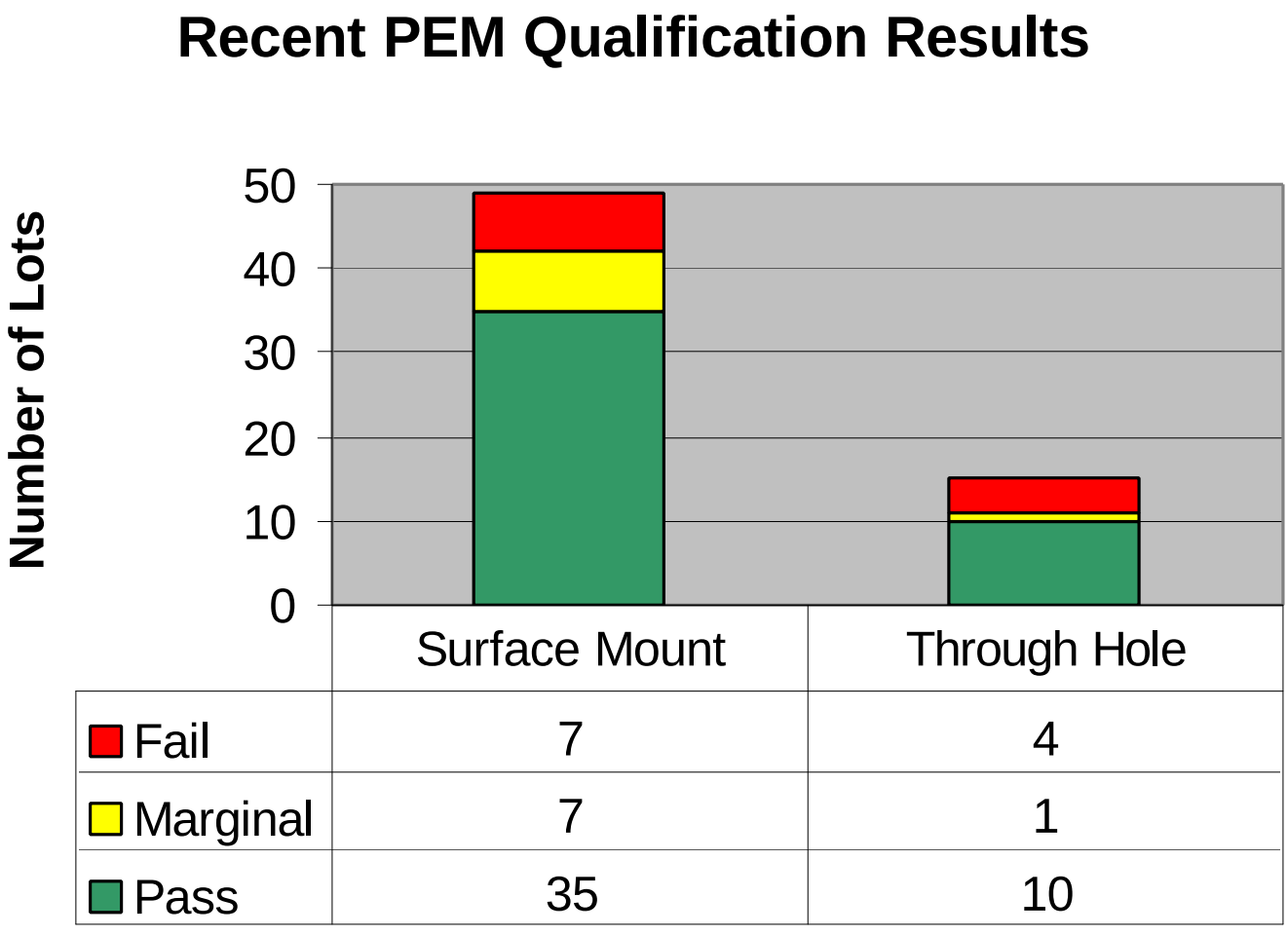

Chart 1. PEM Qualification Results

Table 6. Commercial parts subjected to PEM qualification

MANUFACTURER	COMPONENT FUNCTION	PACKAGE TYPE
A	FPGA	TQFP-144
A	FPGA	TQFP-208
A	FPGA	PLCC-84
B	Adjustable Regulator	TO-220
C	Line Driver/Receiver	SOIC-16
D	CMOS DDS Modulator	PLCC-44
E *	DC/DC Converter	POTTED RECTANGLE-4
F	Solid State Relay	DIP-6
G (4 Lots)	VME Bus Interface	TQFP-144
G	Bus Int. Logic Circuit	TQFP-64
G	Prog. Clock Buffer	PLCC-32
H *	DC/DC Converter	POTTED RECTANGLE-4
I	Timer	SOIC-8
J	Optocoupler	DIP-8
J	Solid State Relay	DIP-6
J (2 Lots)	High Speed Optocoupler	DIP-8
K	Flash Memory	TSOP-56
K	Flash Memory	SSOP-56
K	Embedded Processor	PLCC-84
K	Microcontroller	PLCC-84
L	MOSFET	SOT-23
L	Solid State Relay	DIP-6
M	Supervisory Circuit	SOIC-8
M	Adjustable Regulator	TO-220
N	Timer	SOIC-8
N	Line Driver/Receiver	SOIC-16
N	Supervisory Circuit	SOIC-8
N (2 Lots)	Supervisory Circuit	DIP-8
O	SCRAM	SOIC-16
P	Transistor	SOT-23
P	Line Driver/Receiver	SOIC-16
P (2 Lots)	PLL Clock Driver	PLCC-28
Q	Transistor	SOT-23
Q	Timer	SOIC-8
Q	Line Driver/Receiver	SOIC-16
Q	Peripheral Driver	SOIC-8
Q (2 Lots)	Neg. Adjust. Regulator	TO-220
Q	3-A Adjust. Regulator	TO-220
Q	Quad Peripheral Driver	DIP-16

Table 6 (Cont). Commercial parts subjected to PEM qualification

MANUFACTURER	COMPONENT FUNCTION	PACKAGE TYPE
R	Transistor	SOT-23
R	Timer	SOIC-8
R	MOSFET	SOT-23
R	Line Driver/Receiver	SOIC-16
R	16 Bit Transceiver	TSSOP-48
R	Octal Buffers/Drivers	SOIC-20
S	5V Positive Step-Down Integrated Switching Regulator	HORIZONTAL THROUGH HOLE MOUNT
T	Adjustable Regulator	TO-220
U	Timer	SOIC-8
V	Line Driver/Receiver	SOIC-16
W	Supervisory Circuit	SOIC-8
X	Solid State Relay	DIP-6
Y	Timer	SOIC-8
Y	Line Driver/Receiver	SOIC-16
Y	16 Bit Transceiver	TSSOP-48
Y	Peripheral Driver	SOIC-8
Y	Octal Buffers/Drivers	SOIC-20
Z *	DC/DC Converter	POTTED RECTANGLE-4

*Process altered from 100 hours of HAST to 1000 hours of 85 °C/85 % RH

Table 7. Failures and construction anomalies encountered during the PEM qualification process

Manufacturer	Component Function	Package Type	Comments
A	FPGA	PLCC-84	The proper moisture sensitivity level was determined to be a level 6 instead of level 1 as suggested by the manufacturer.
A	FPGA	TQFP-144	The proper moisture sensitivity level was determined to be a level 6 instead of level 1 as suggested by the manufacturer.
A	FPGA	TQFP-208	This particular part was considered a reliability risk due to poor wire bond strength caused by possible chlorine contamination (results after 100hrs of HAST).
G (4 Lots) *	VME Bus Interface	TQFP-144	Construction/Failure analysis discovered poor die attach problems due to the manufacturers use of a stamped die paddle instead of the more desirable/reliable etched die paddle.
J	High Speed Optocoupler	DIP-8	During the course of HAST testing ICCH failures occurred in several devices due to a metallic growth between the leads. The metallic growth was the result of incomplete cleaning of the flux in preconditioning. The failure analysis lab advised that these parts be used in a controlled, low humidity environment and to implement adequate package cleaning techniques to remove flux and residue.
K	Embedded Processor	PLCC-84	Post HAST construction analysis revealed lifted wire bonds after plastic encapsulation removal. Wire bond pulls resulted in the ball bonds measuring less than minimum acceptable amount of force. This type of bonding problem is due to contaminants in the encapsulant (Kirkendall Voiding).
M	Adjustable Regulator	TO-263	This particular part was considered a reliability risk due to poor wire bond strength caused by possible chlorine contamination (results after 100hrs of HAST).
P *	PLL Clock Driver	PLCC-28	The presence bromine and chlorine in the encapsulant of Lot 1 resulted in a classic case of Kirkendall voiding.
Q *	Quad Peripheral Driver	DIP-16	Wire bonding anomalies discovered during construction analysis (i.e. stray wires, bond-over- bonds, bond wires touching die or within one wire's diameter of the die)

Table 7 (con't). Failures and construction anomalies encountered during the PEM qualification process

Manufacturer	Component Function	Package Type	Comments
Q	Neg. Adjust. Regulator	TO-220	Long term reliability concerns exist due to the use of copper bond wires.
R *	transistor	SOT-23	The encapsulant had a low glass transition temperature and was very susceptible to the ingress of moisture, which in turn caused electrical overstress.
R *	MOSFET	SOT-23	Failed electrically due to high ESD sensitivity. Other manufacturers are not as susceptible to ESD damage.
S *	5V Positive Step-Down Integrated Switching Regulator	Horizontal through hole mount	Evidence of a poorly controlled soldering process was exhibited. The failures were traced back to the capacitors not having the mechanical strength and the moisture resistance characteristics suitable for the HAST conditions . The manufacturer has acknowledged these problems and is revising the assembly process.
V	Line Driver /Receiver	SOIC-16	Construction analysis revealed bond pad damage due to over-bonding.
X *	Solid State Relay	DIP-6	Poor packaging of these devices allowed the ingression of excessive amounts of moisture resulting in dendrite growths, which electrically short internal circuitry
Z *	DC/DC Converter	POTTED RECT.-4	All samples received failed initial electrical tests and exhibited poor construction quality.

*Not recommended for use in military systems applications

As mentioned previously, the typical failure mechanism of PEMs involve voiding. Other failure mechanisms do occur and three good examples are illustrated in Figures 4, 5 and 6. Figure 4 illustrates a cracked chip capacitor in the switching regulator supplied by manufacturer S after being subjected to 25 hours of biased HAST. The failure was traced back to the capacitors not having the mechanical strength and the moisture resistance characteristics suitable for the HAST environment.

Figure 4. Cracked chip capacitor

Figures 5 illustrates evidence (cracks in the encapsulant around the lead frame) of poor package integrity in the solid state relay supplied by manufacturer X. These cracks in the encapsulant, which were present in all of the parts supplied by manufacturer X, allowed moisture to be induced at an even more accelerated rate. The excessive amounts of moisture produced dendritic growths, which electrically shorted the internal circuitry as illustrated in Figure 6.

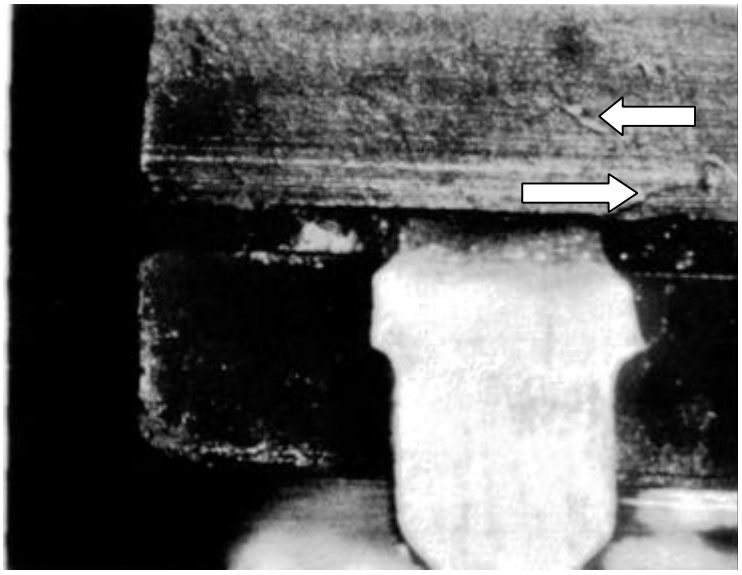

Figure 5. Plastic encapsulant cracks

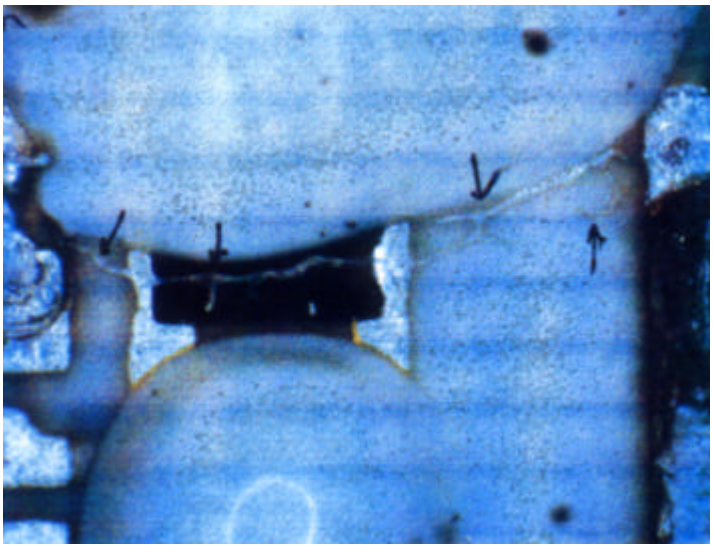

Figure 6. Internal dendritic growth

5.0 CONCLUSIONS

Cost and obsolescence issues are forcing the military/space hardware designers to move from military/space specific applications products to the use of commercial grade PEMs. PEMs are being used in military/space systems, but there needs to be a critical realization that commercial components are often manufactured using uniform, highly automated lines that produce quite reliable parts for use in a typical commercial/consumer application. But PEMs used in harsh military/space environment with their unique reliability requirements may cause intermittent and catastrophic failures. A large portion of failures are moisture related - water ingressing into the PEM and acting as a catalyst for corrosion on elements inside the package.

All epoxy materials used for encapsulation absorb moisture to some extent, causing corrosion inside the package. PEM manufacturers often use silicon nitride as a passivation layer on the surface of the die, but it does not always provide a crack or pinhole free conformal coating. Defects in the passivation layer and around bond pad edges can allow ionic contamination and moisture to enter, eventually degrading aluminum metallization traces or contaminating inter-layer dielectric. Corrosion can also attack the wire bond pad interface.

One of the critical factors concerning PEMs is that their reliability may be lot dependent. As an example, two lots of PLL clock drivers with different date codes supplied by manufacturer P were evaluated. One date code failed due to chlorine contamination in the encapsulant, whereas the other date code passed with no problems. Therefore it is recommended that in PEM applications, sample devices from each lot date code should be subjected to HAST qualification testing.

Maintaining multiple PEM component sources is advisable. Another example, to illustrate this point is the VME Bus Interface microcircuit supplied by manufacturer G. As referenced in Table 2, the VME Bus Interface has serious reliability risks, but manufacturer G is the sole manufacturer. This brings up the tradeoff between component reliability and the cost of board redesign. Designs, if practical or possible, should be developed around components supplied by multiple sources that are evaluated in advance.

Most PEMs can work well beyond their recommended operating conditions. However, if a space/military system requires optimum reliability and if PEMs are part of the implement plan, then PEM qualification is mandatory. The qualification test plan outlined in Fig. 2 and 3 is intended for use as a guideline. Additional qualification testing may be required on PEMs for some applications, such as total ionizing dose (TID) radiation and single event upset (SEU)/latchup testing to meet application specific requirements. For additional details, consult references provided for EIA/JEDEC test methods and guidelines for evaluation of PEMs [2]-[9].

References

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2. SSB-1, Guidelines for Using Plastic Encapsulated microcircuits and Semiconductors in Military, Aerospace and other rugged applications, available at JEDEC web site: http://www.jedec.org

3. JEDEC Test Method JESD-22-A112-A: Moisture Induced Stress Sensitivity for plastic Surface Mount devices.

4. JEDEC JEP 113A: Symbols and Labels for Moisture Sensitive Devices.

5. IPC/JEDEC J-STD-035: Acoustic Microscopy for Non-hermetic Encapsulated Elecronic Components

6. EIA JESD-22-A101 Test method: Temperature Humidity Bias Test

7. EIA JESD-22-A102 Test Method: Autoclave Test

8. EIA JESD-22-A110 Test Method: Highly Accelerated Stress Test (HAST)

9. EIA JESD-22-A113 Test Method: Preconditioning of surface Mount devices