

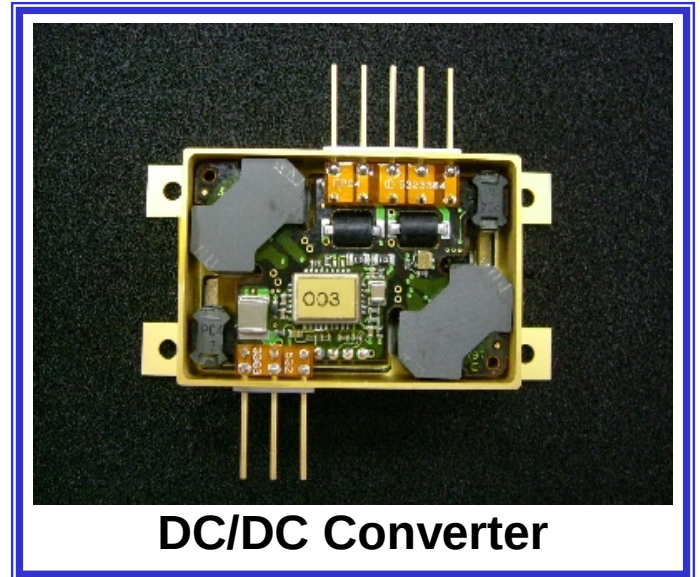
New DC/DC Converter for Space Applications

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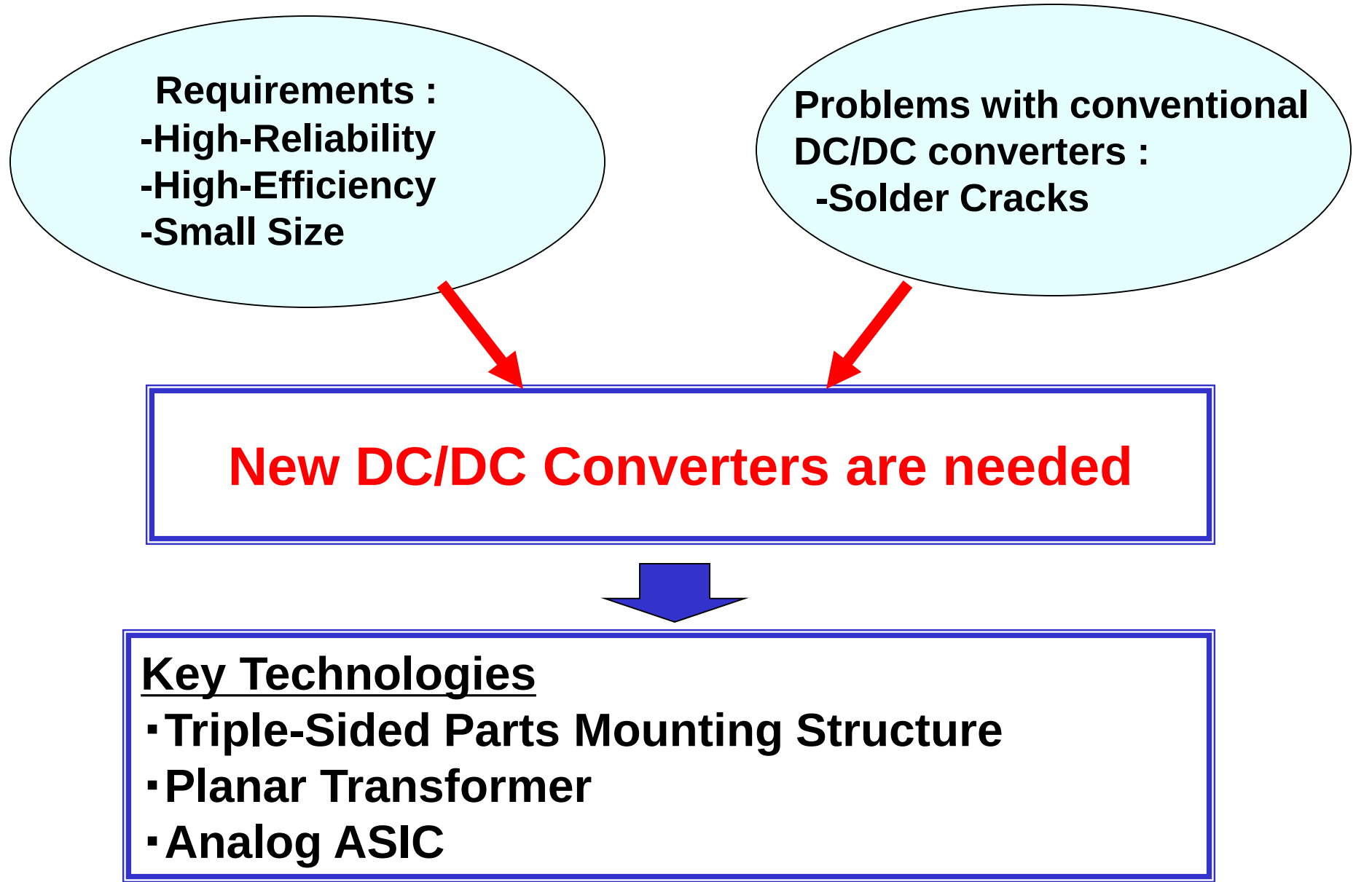
March 29-April 2, 2004

- **Background**
- **Overview**
 - Features
 - Structure
 - Functional Block Diagram
 - Key Elements
- **Detailed Data**
 - Electrical Test
 - Radiation Test for Critical Parts
 - Initial Environmental Test
- **Development Schedule**
- **Conclusion**



Requirements :
-High-Reliability
-High-Efficiency
-Small Size

**Problems with conventional
DC/DC converters :**
-Solder Cracks



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graph TD; A([Requirements :  
-High-Reliability  
-High-Efficiency  
-Small Size]) --> C[New DC/DC Converters are needed]; B([Problems with conventional  
DC/DC converters :  
-Solder Cracks]) --> C; C --> D[Key Technologies  
▪ Triple-Sided Parts Mounting Structure  
▪ Planar Transformer  
▪ Analog ASIC];
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New DC/DC Converters are needed

Key Technologies

- Triple-Sided Parts Mounting Structure
- Planar Transformer
- Analog ASIC

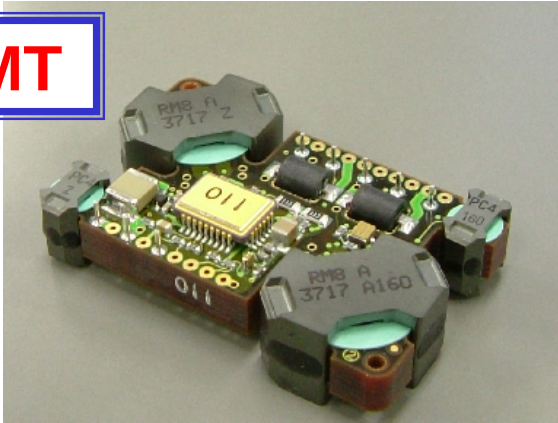
General

- **Input Voltage** : +26V to +55V
- **Dual Outputs** : $\pm 15V \pm 2\%$, 1.3A
- **Fixed Frequency** : 100kHz (typical.)
- **Efficiency** : up to 88%
- **Size** : 58mm(W) × 40mm(D) × 17mm(H)
- **Weight** : 150g MAX

Environment

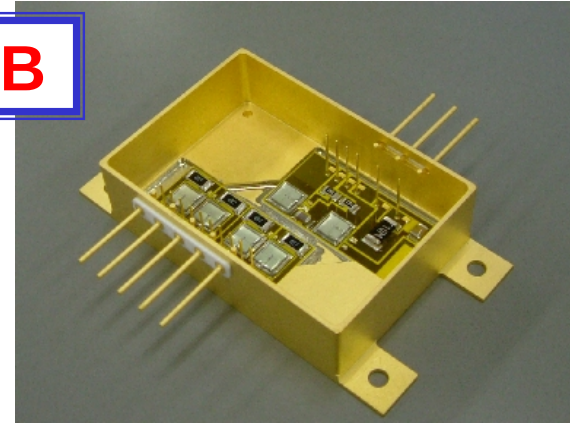
- **Operating Temperature** : -55°C to +125°C
- **Mechanical Shock** : 100G, 6ms
- **Vibration** : 20G, Sin, 20Hz-2kHz

SMT

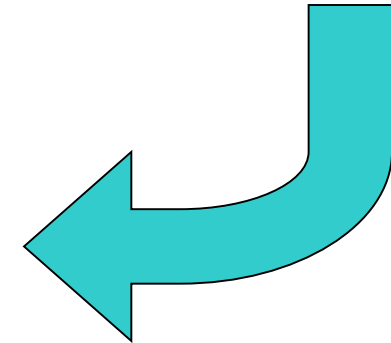
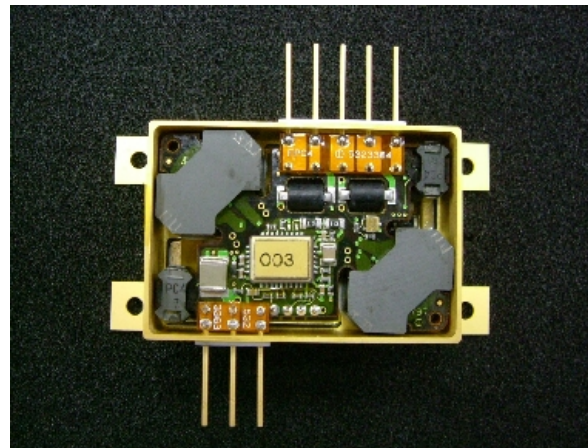
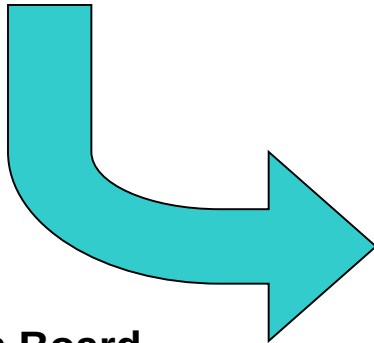


Planar Transformer with Parts

COB



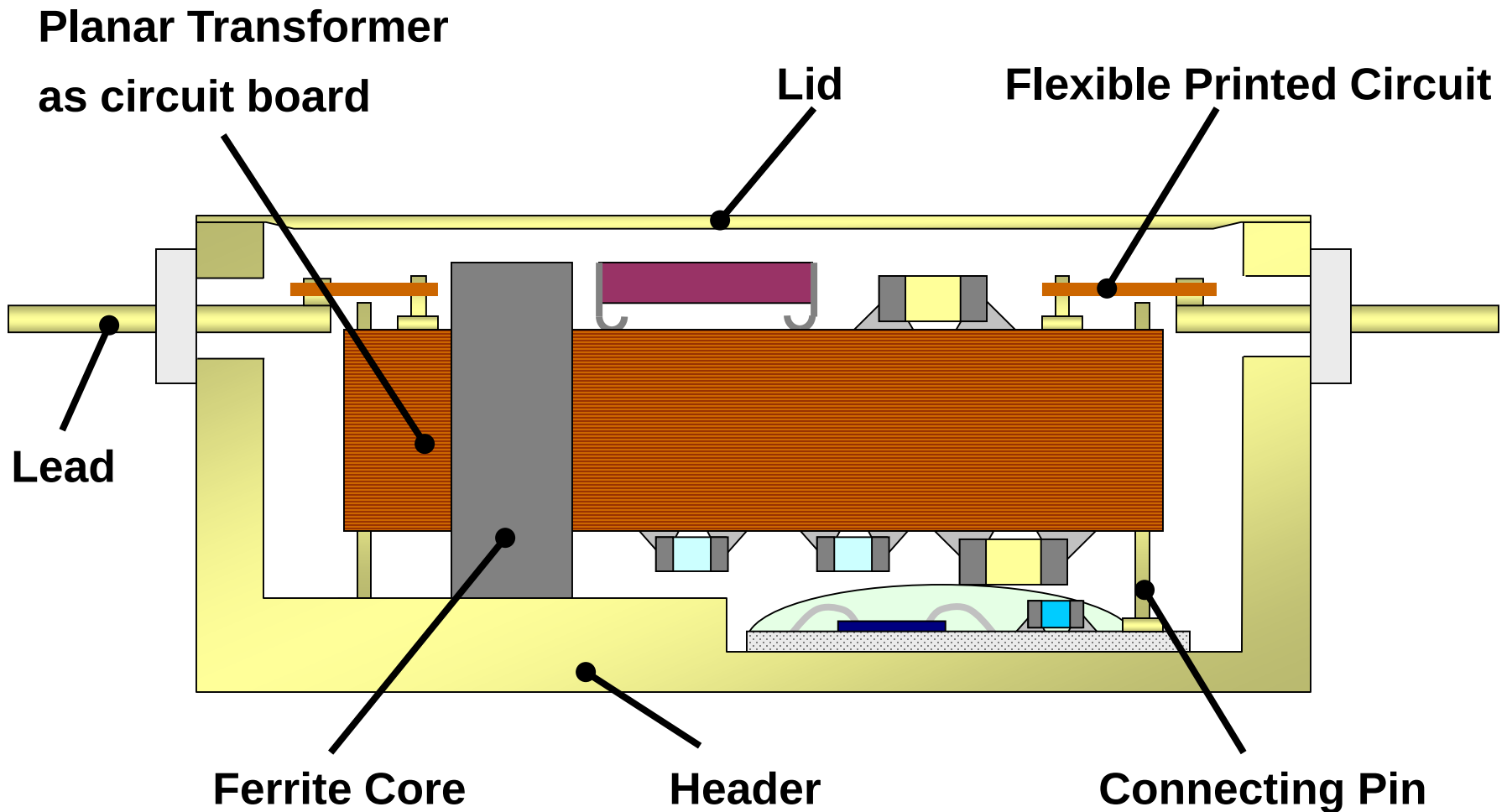
Header with Power Parts



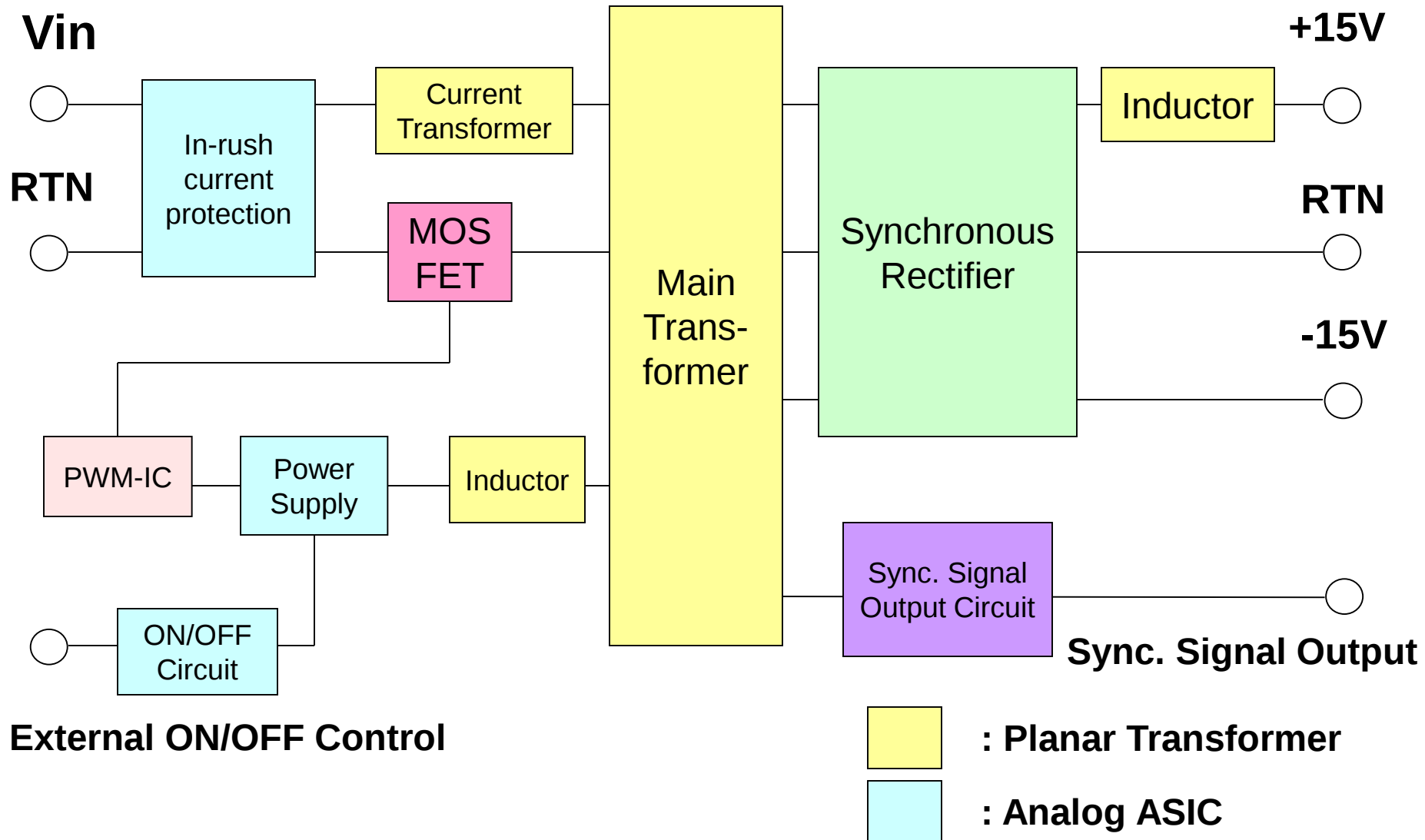
COB:Chip on Board
SMT:Surface Mount Technology

SMT + COB = Triple-Sided Parts Mounting Structure

Structure of DC/DC Converter (Cross Section)



Functional Block Diagram



1. Planar Transformer

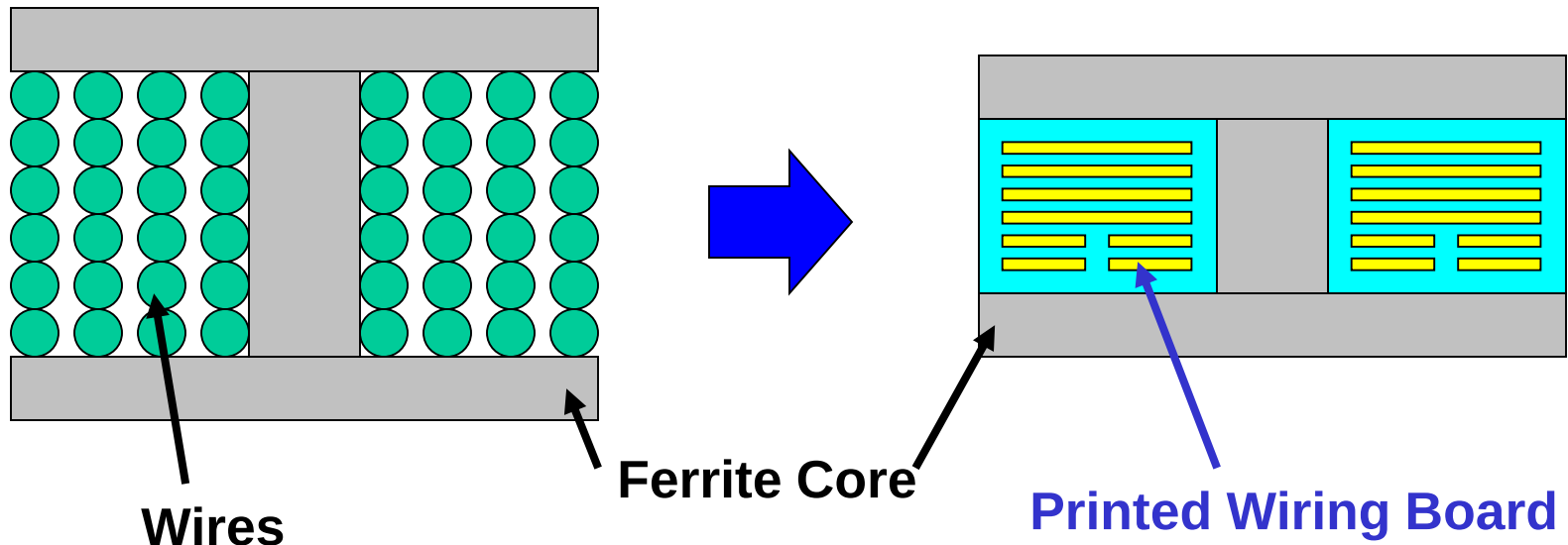
2. Analog ASIC

1-1. Concept of Planar Transformer

Replace wires with PWB stacks (32 layers)

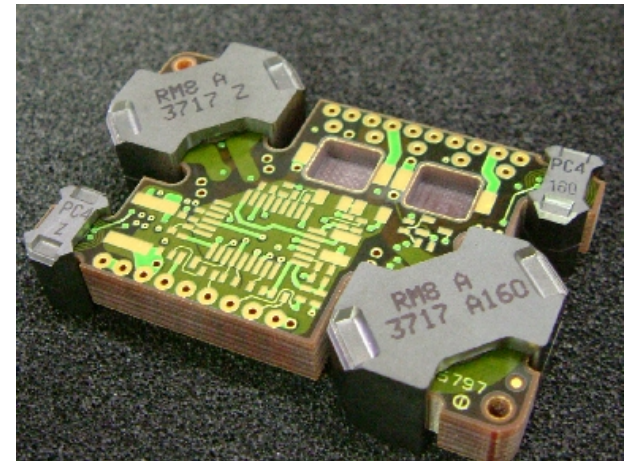
Wire-Wound Transformer

Planar Transformer

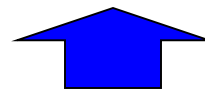


1-2.Feature of Planar Transformer

- No micro-soldering and wiring
- Circuit integration
- Double-sided parts mounting
- Uniform characteristics
- Good thermal conductivity
- Low height



Planar Transformer



Improve Reliability

- Vulnerable to cracks on micro-soldering area
- Vulnerable to scratches to Wires
- Characteristics not uniform
- Weak thermal conductivity



Conventional example

2-1. Analog ASIC

Features

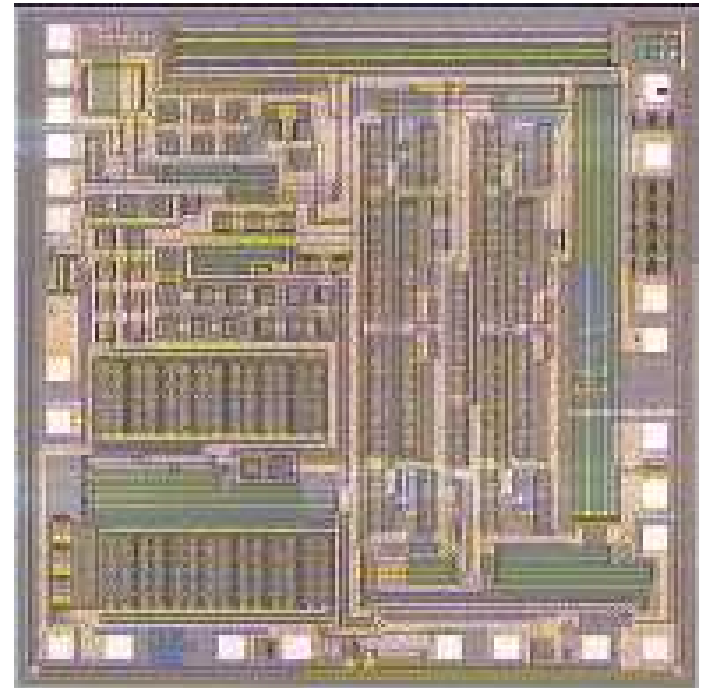
- 47 low loss devices
- Radiation-proof design

Functions

- Power supply to PWM-IC
- Overload and overvoltage protections
- External ON/OFF control

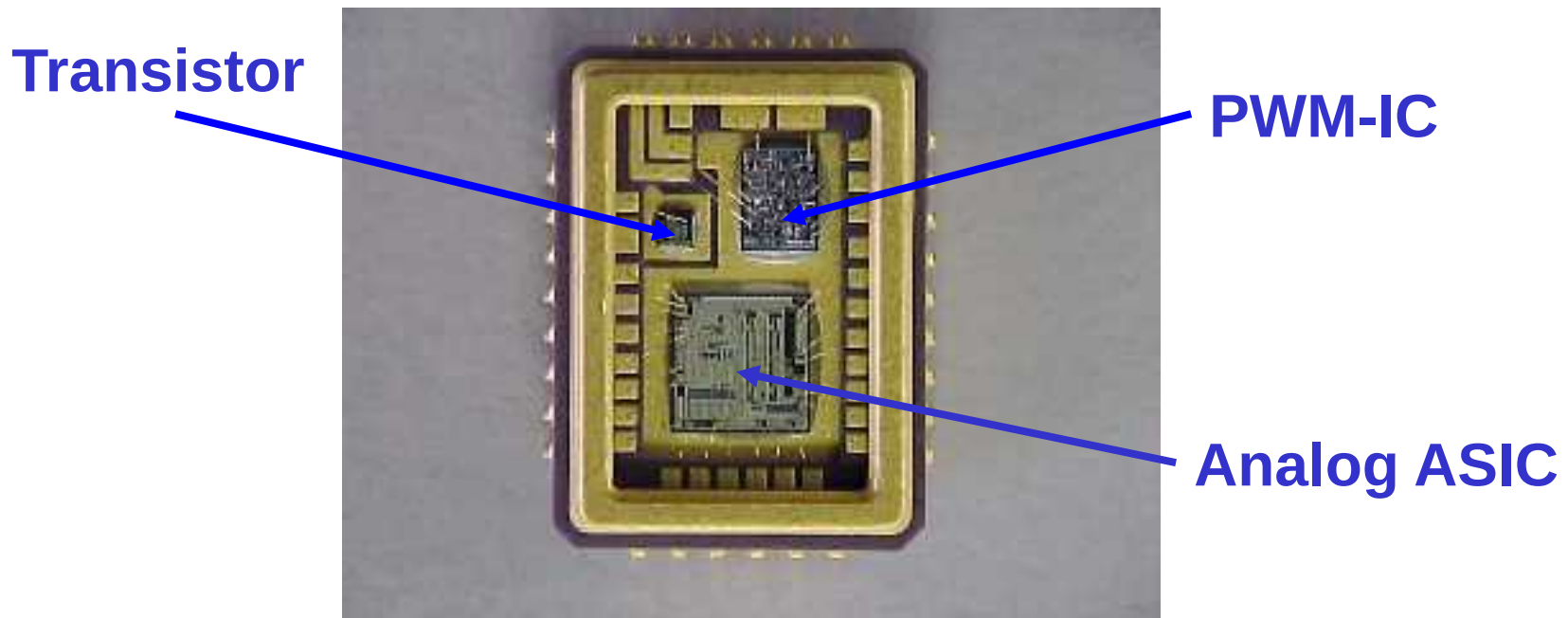
Effect

- 74% footprint reduction from equivalent discrete devices



2-2. Package of Analog ASIC

The Analog ASIC is packaged together with a Transistor and PWM-IC chip



Contribute to a miniaturization of DC/DC Converter

Characteristics

Electrical Characteristics

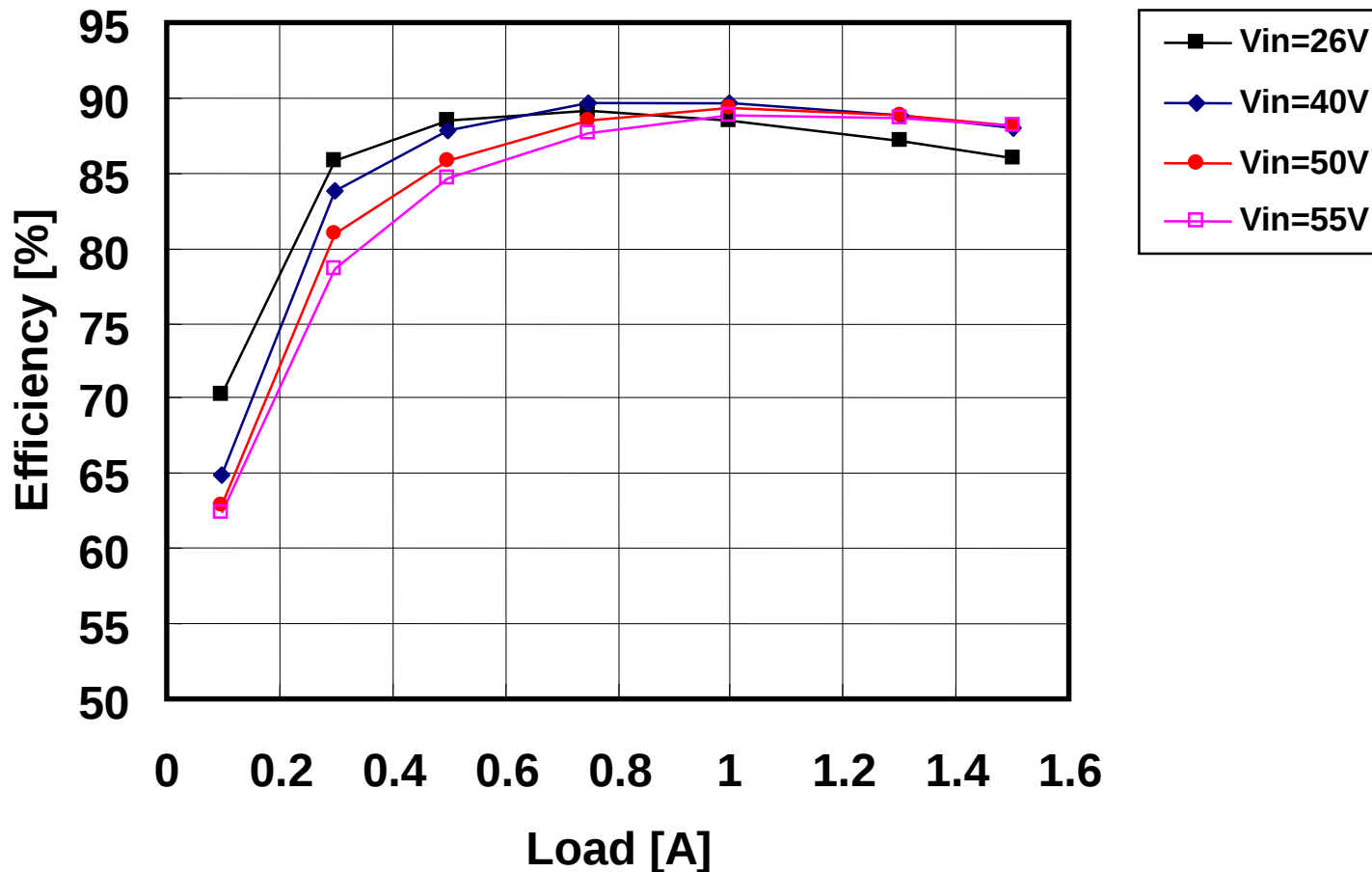
Parameter	Condition	MIN	TYP	MAX	UNITS
Input Voltage	Continuous	26	50	55	VDC
Output Voltage	—	±14.70	±15.00	±15.30	VDC
Output Current	Vin=26 to 55VDC	±0.3	±1.3	±1.5	A
Output Power	Vin=26 to 55VDC	—	39	45	W
Output Ripple Voltage	Vin=26 to 55VDC	—	80	150	mVpp
Line Regulation	Vin=26 to 55VDC	—	100	300	mV
Load Regulation	Iout=0.2A to 1.5A	—	100	300	mV
Efficiency	Vin=50V, Iout=1.3A	85	88	—	%

Other Characteristics

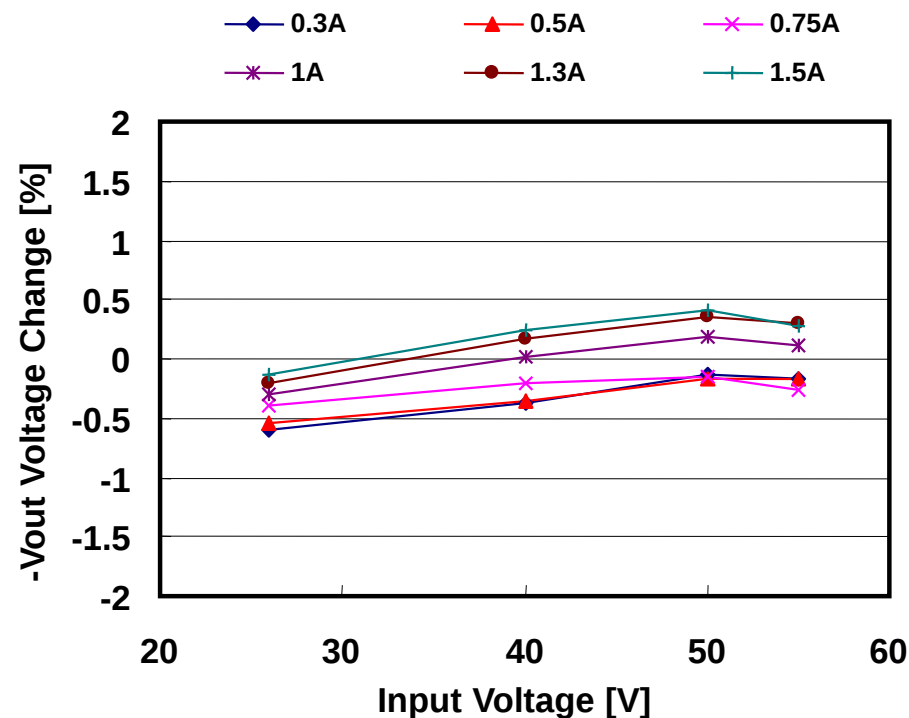
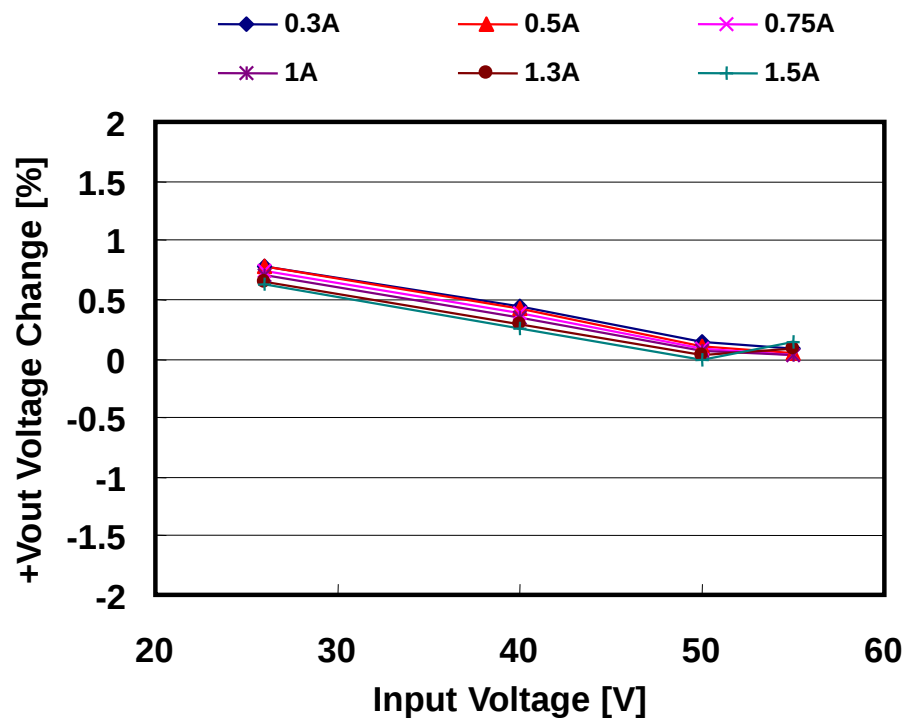
Description	Characteristics
Protection	Overload Protection Overvoltage Protection
Function	External ON/OFF Control Synchronous Signal Output
Isolation	500VDC (Input to Output)
Operation Frequency	100kHz Typical

Load versus Efficiency Characteristics

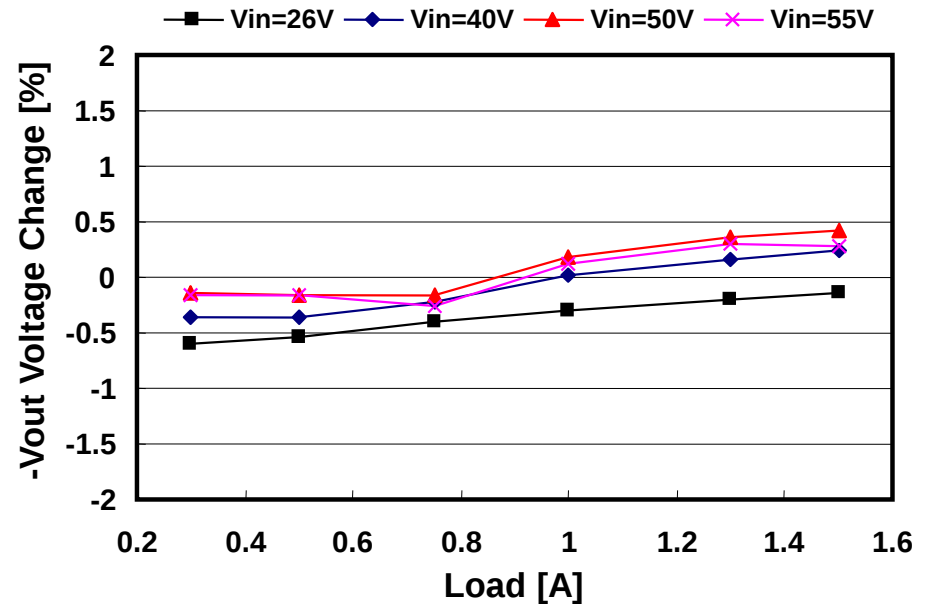
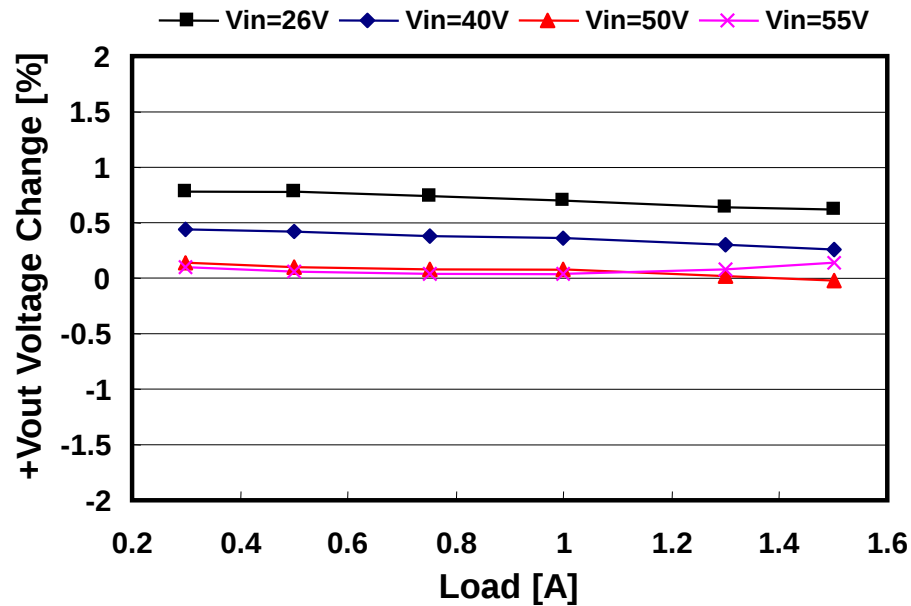
Test result shows efficiency of almost 88%



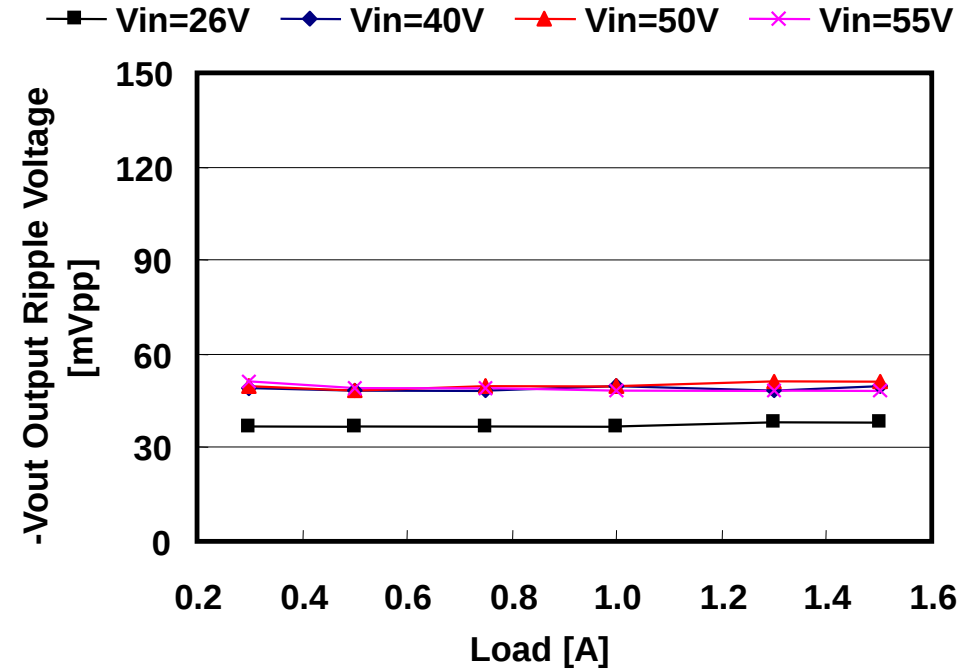
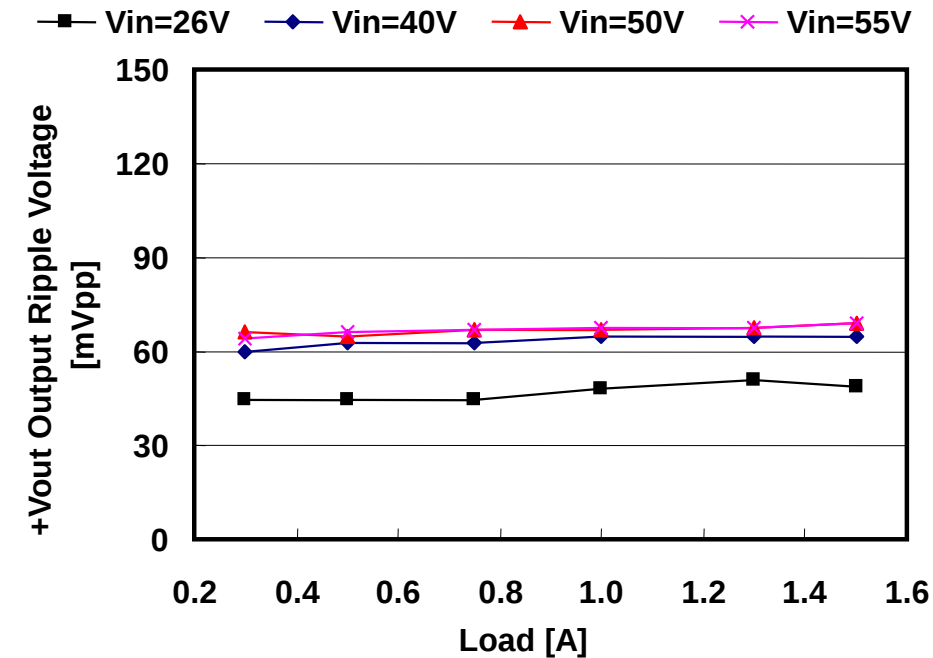
Line Regulation Characteristics



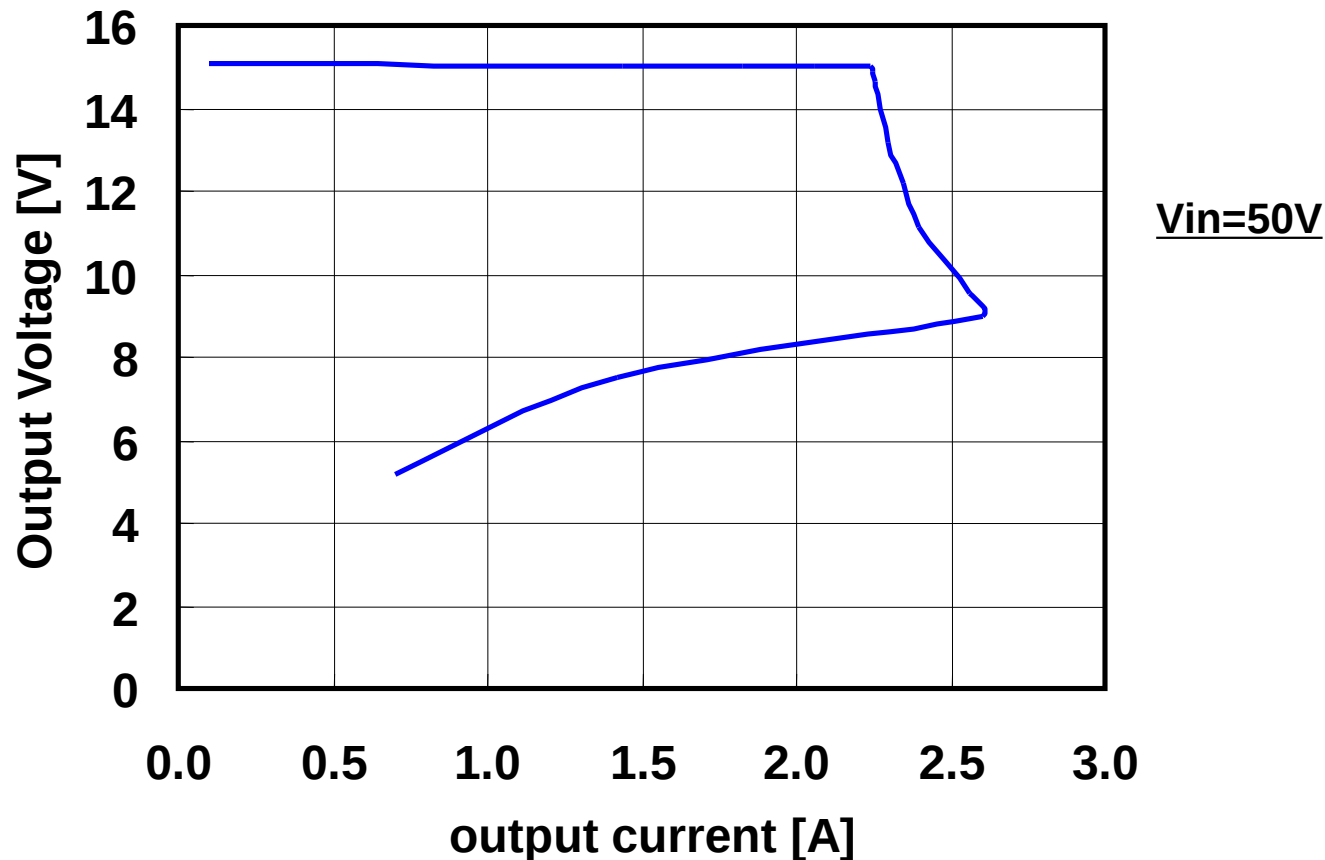
Load Regulation Characteristics



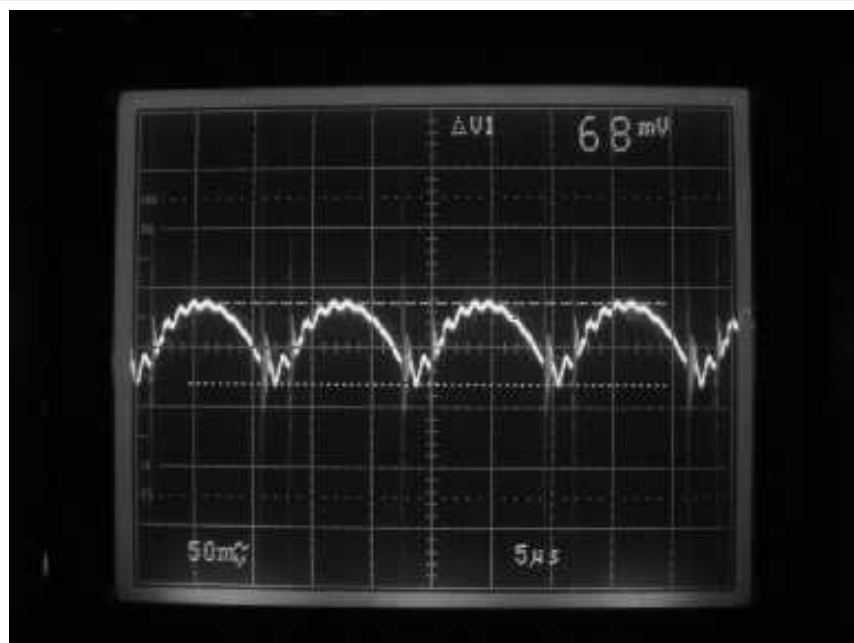
Output Ripple Voltage Characteristics



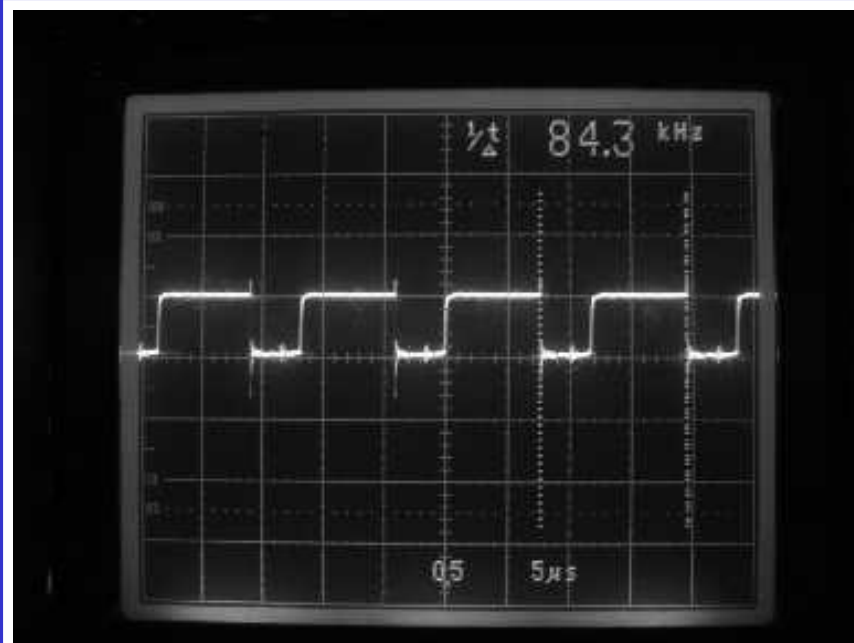
Overload Protection Characteristics



Waveform Photograph



Output Ripple
Vin=50V, Load=1.3A, Tc=25°C



Synchronous Signal
Vin=50V, Load=1.3A, Tc=25°C

Radiation Data

We have radiation data on the following five items

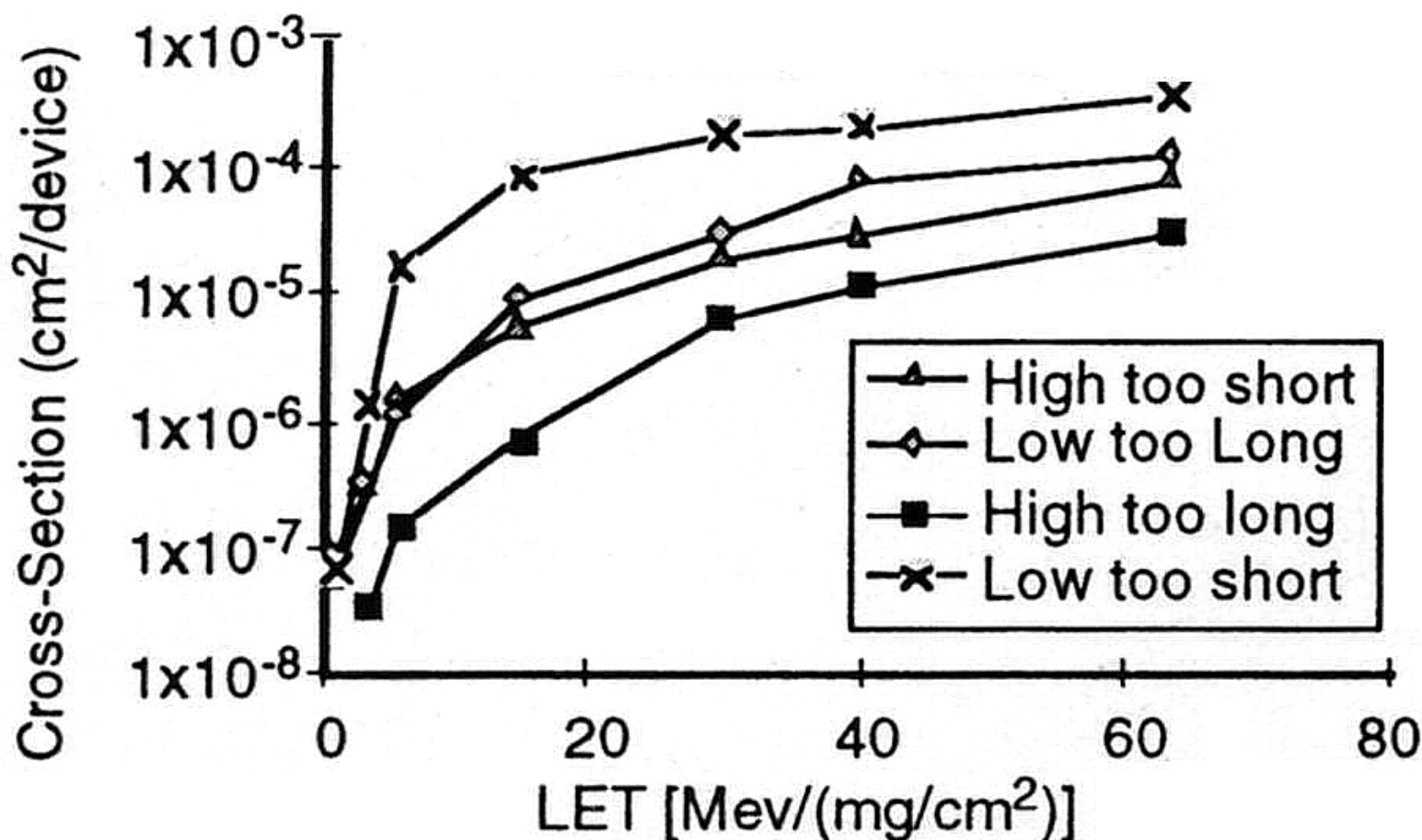
Device	SEE	TD
PWM-IC	○	○
Shunt Regulator	—	○
Optocoupler	—	○
Analog ASIC	○*	○*
Power MOSFET	○*	○*

***Radiation tests were performed by JAXA.**

SEE Sensitivity of PWM-IC

- **Latch-up is not expected in bipolar devices.**
- **SEU is observed on output pulses as follows:**
 - High too long**
 - Low too short**
 - High too short**
 - Low too long**
- **SEU will not affect DC/DC Converter outputs.**

SEU Test Data of PWM-IC



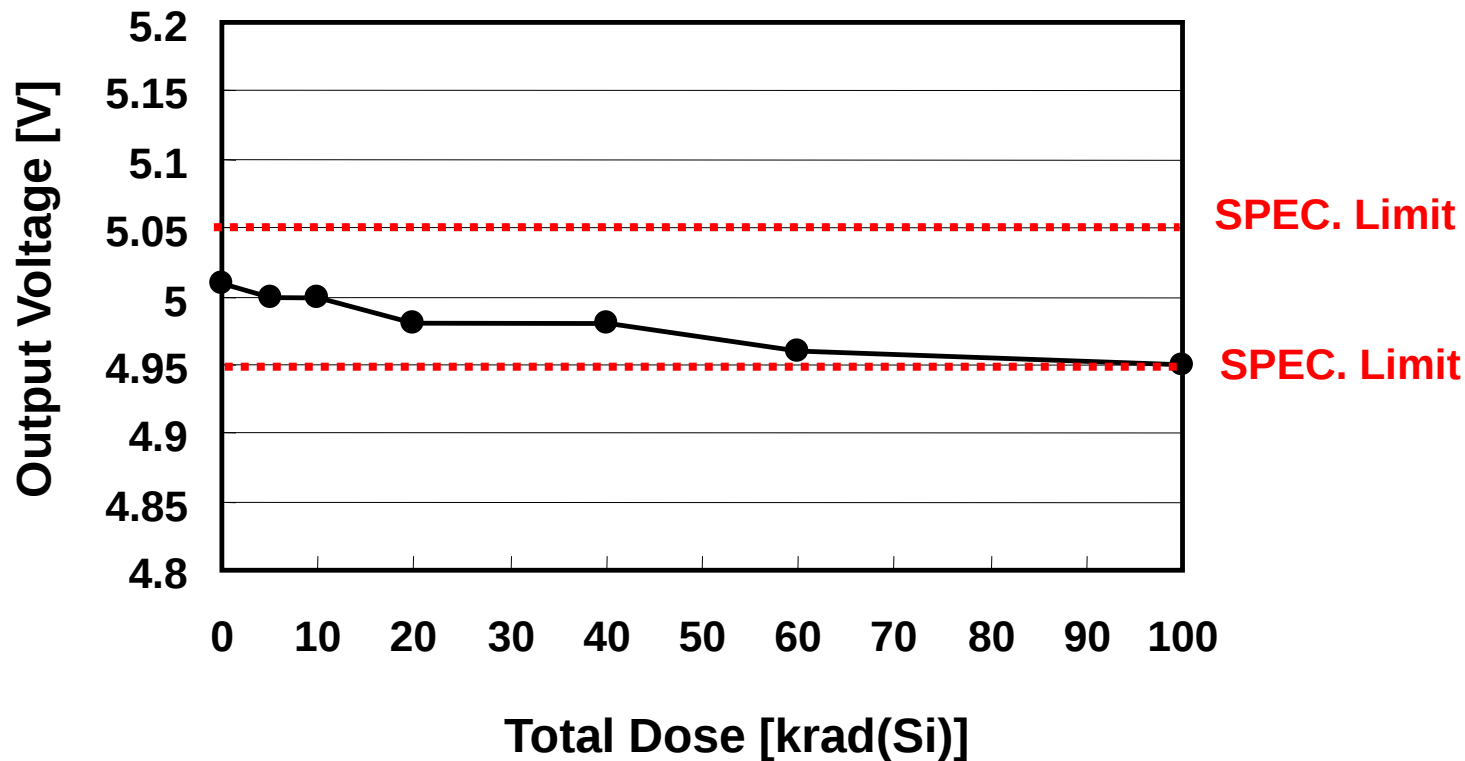
Ref.: "Single Event Effects in Pulse Width Modulation Controllers,"
IEEE Trans. Nucl. Sci., NS-43, No. 6 (December 1996)

Total Dose Sensitivity of PWM-IC

- **Radiation-sensitive parameters are:**
 - **Output Voltage in the Reference Section**
 - **Start Threshold in the Under-Voltage Lockout Section**
- **No significant radiation-sensitivities were observed in other test parameters.**

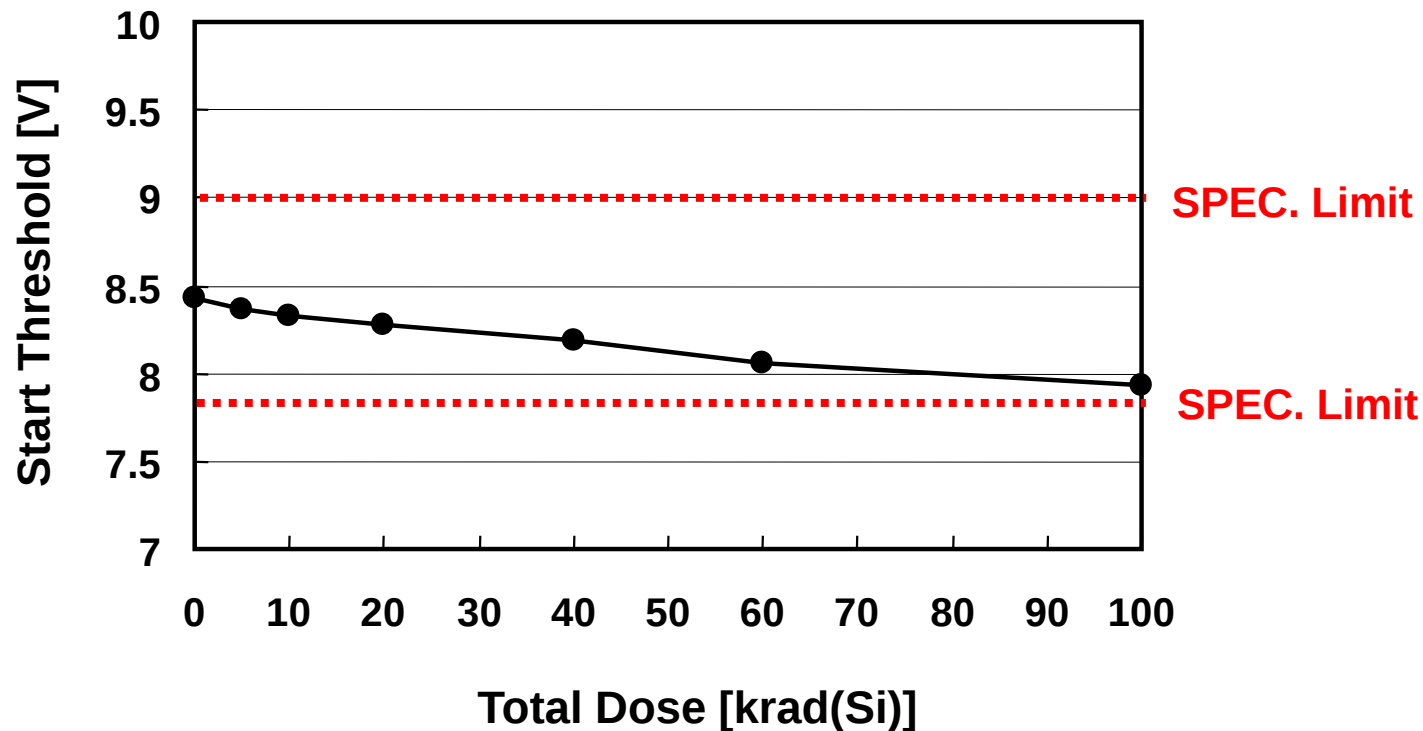
Total Dose Test Data1 of PWM-IC

The degradation is within spec.



Total Dose Test Data2 of PWM-IC

The degradation is within spec.



Total Dose Test Data of Shunt Regulator

No significant sensitivity to radiation

Parameter	Radiation Level, Rads(Si)					Pretest Spec
	0K	25K	50K	75K	100K	
VREF(V)@ VKA=VREF, IK=10mA	2.48756	2.48730	2.48722	2.48723	2.48702	2.400 Min 2.600 Max
IREF(μ A)@ IK=10mA, R1=10K Ω ,R2= ∞	1.40	1.59	1.69	1.76	1.83	8 Max
Ioff(μ A)@ VKA=12.5V, VREF=0V	0.020 (Note 1)	0.020	0.020	0.020	0.020	3 Max (Note 2)

NOTES:

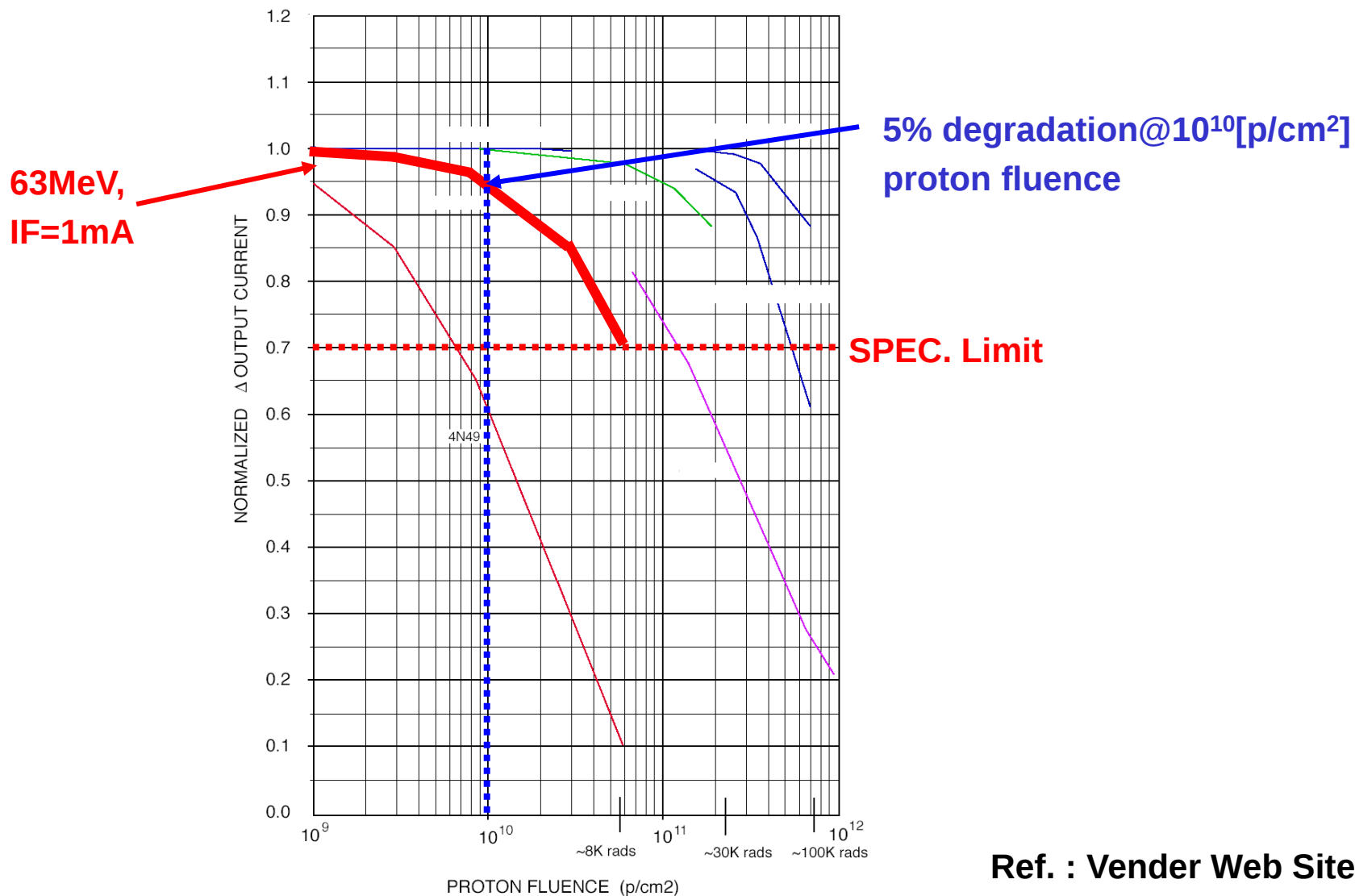
1. All Ioff measurements recorded 20Na, attributable to the fixture leakage.
2. At VKA=36.

Ref.: "TID Summary," Vertical Circuits,Inc.

Proton Radiation Sensitivity of Optocoupler

- **Radiation-sensitive parameter is CTR**
- **Electrical parameters are similar to 4N49 optocoupler but with much better CTR degradation characteristics against radiation exposure**
- **The degradation of output current is quite slight at proton radiation of 10^{10} particles/cm² (equivalent to about ten-year exposure)**

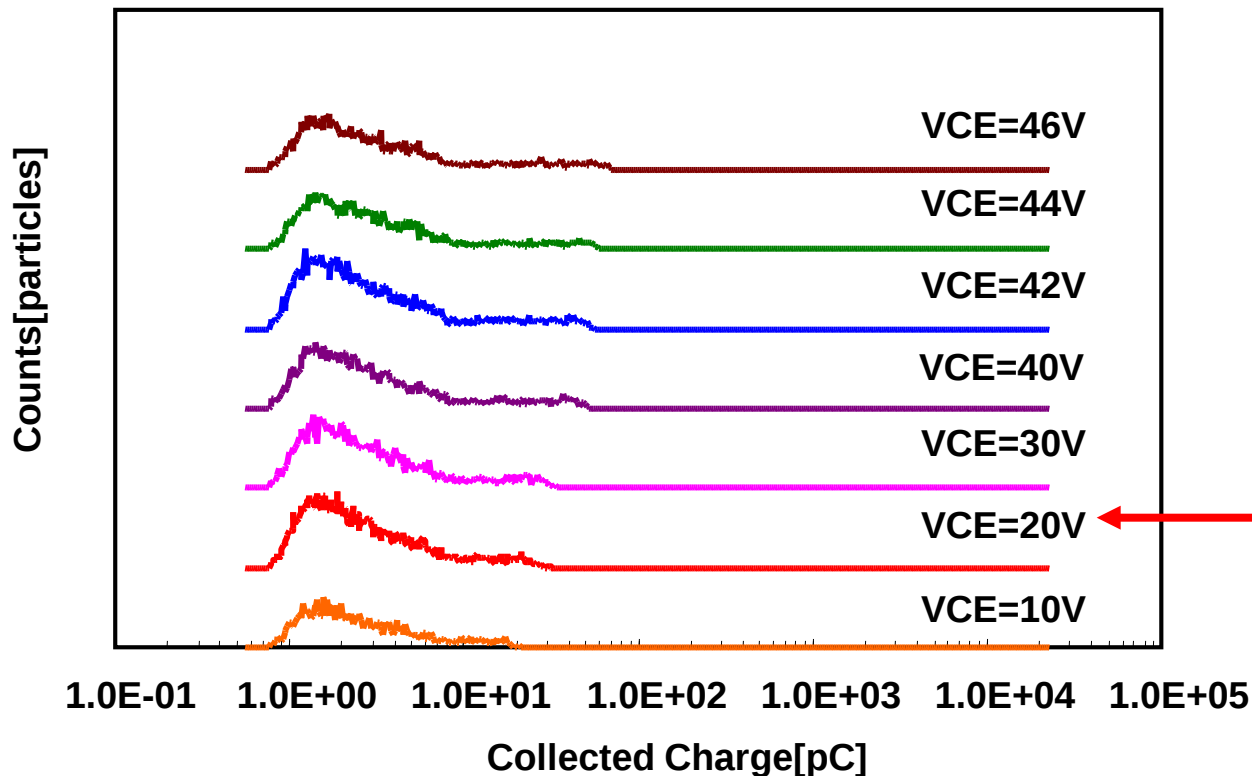
Proton Radiation Test Data of Optocoupler



SEB Test Result1 of Analog ASIC

SEB test result of Tr TEG used Analog ASIC

No SEB was observed up to $46V_{CE}$



Ion : $^{58}Ni^{18+}$

Energy: 250MeV

LET : 27.7MeV/(mg/cm²)

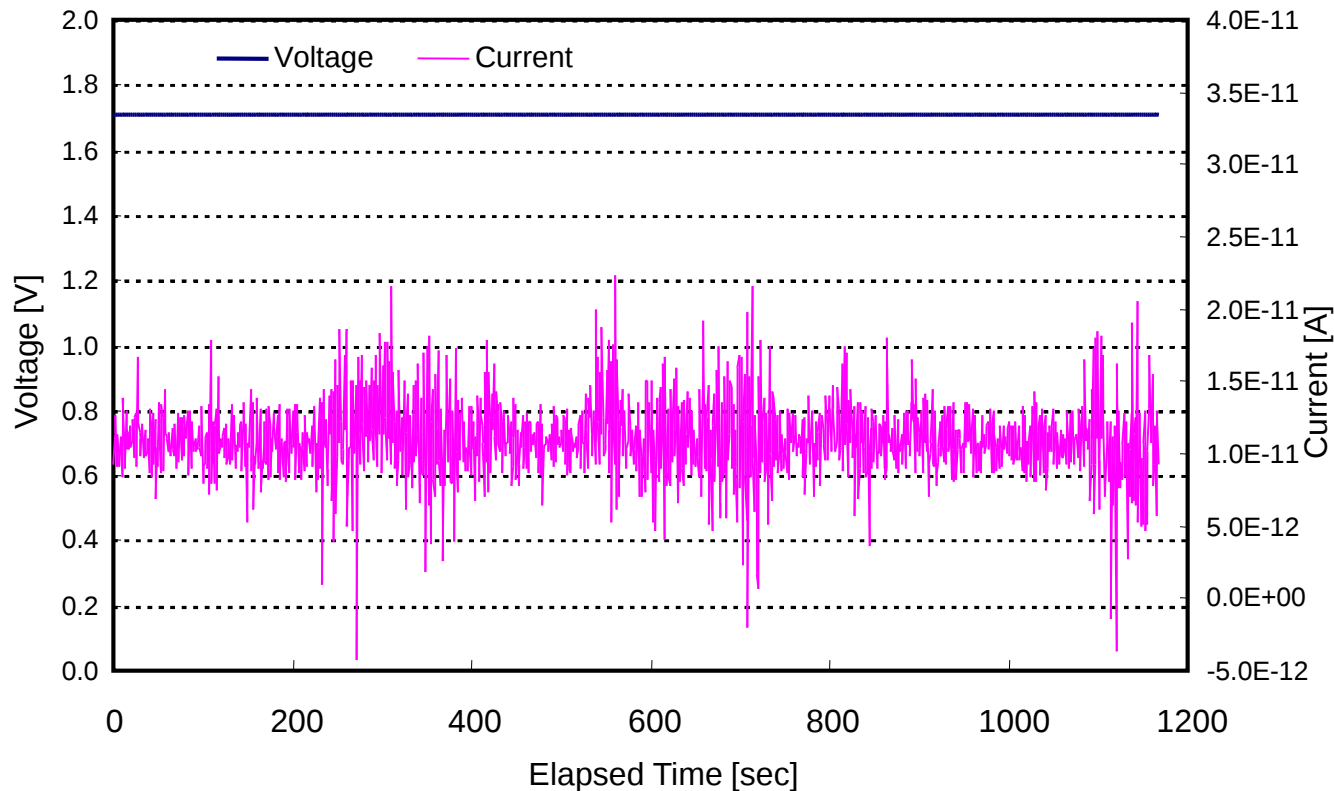
Range : 38.95 μ m

Max Operation
Voltage : 20V

SEB Test Result2 of Analog ASIC

SEB test result of Analog ASIC

No influence of radiation was observed



Ion : $^{58}\text{Ni}^{19+}$

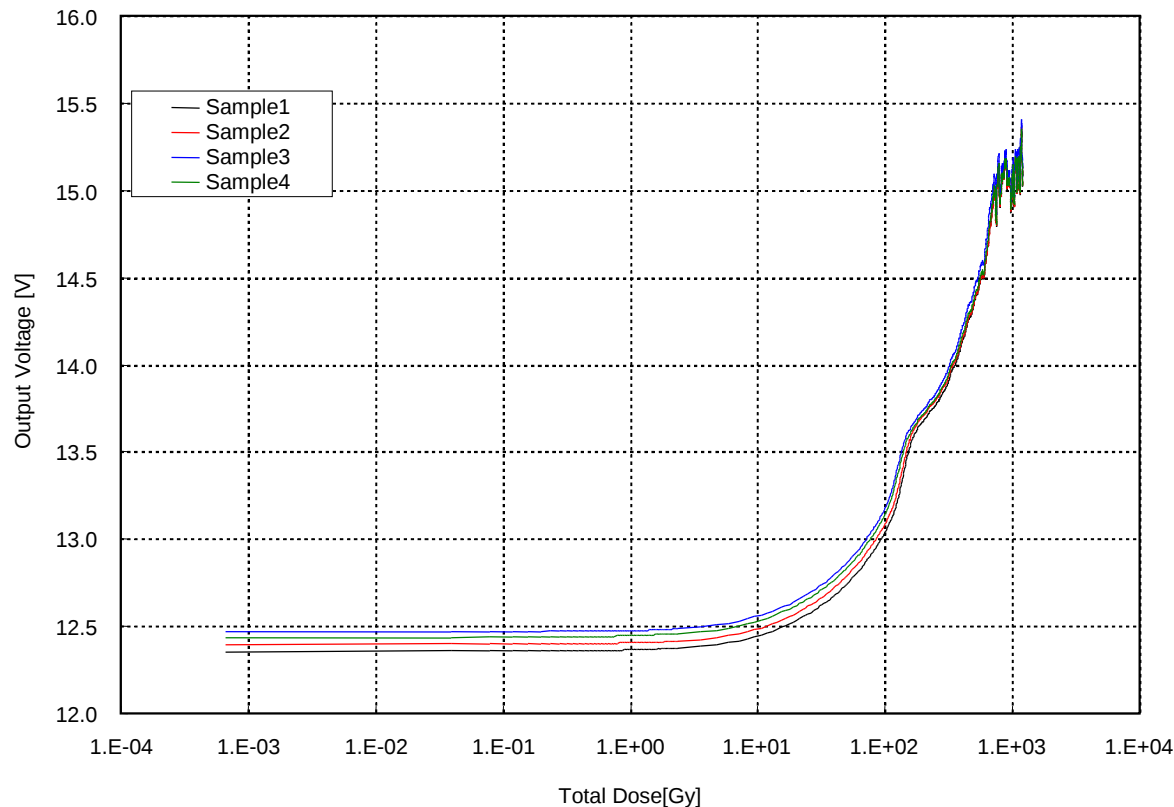
Energy: 381MeV

LET : 25.8MeV/(mg/cm²)

Range : 50.0 μm

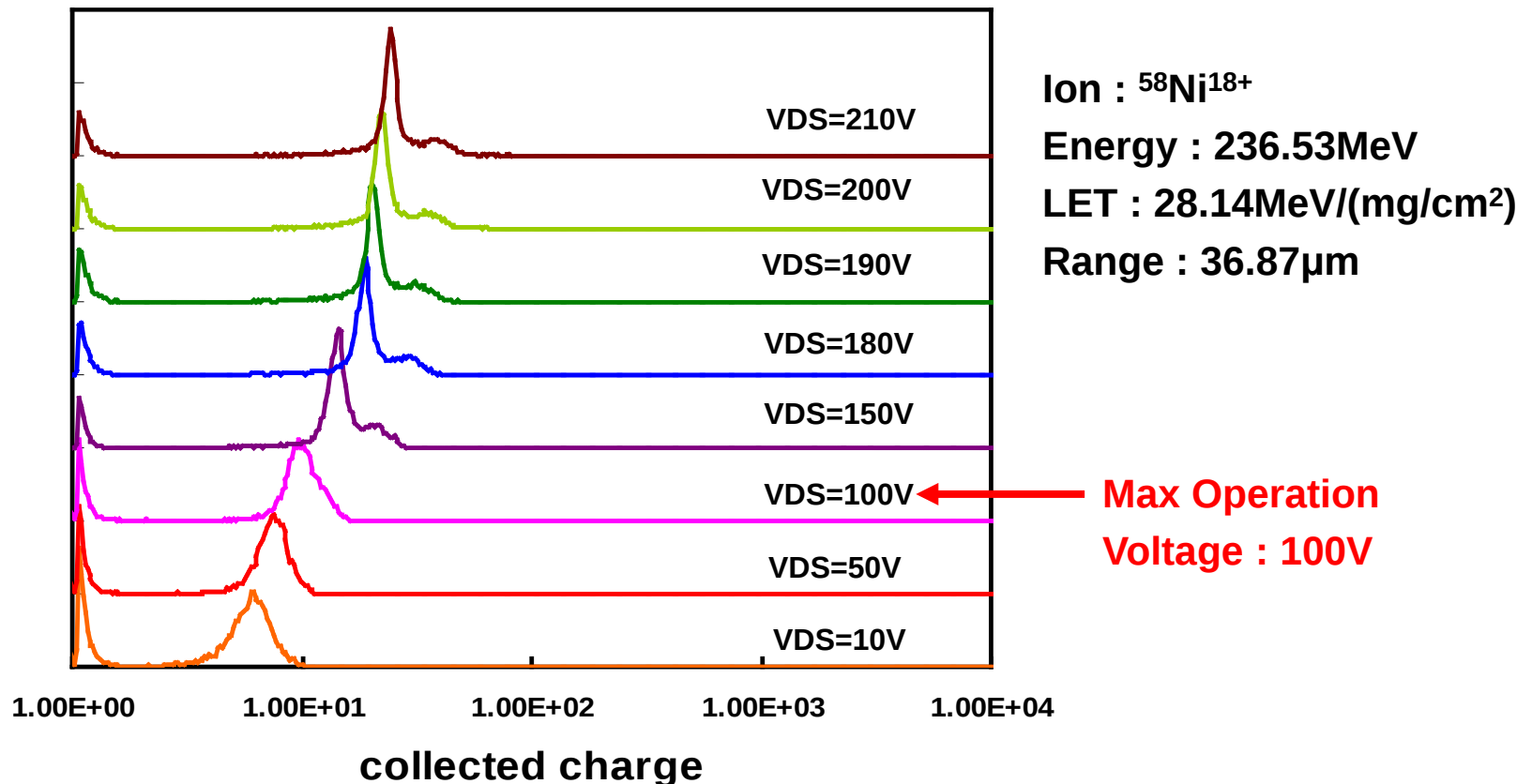
Total Dose Test Result of Analog ASIC

Increase of output voltage was observed
This will not pose a practical problem



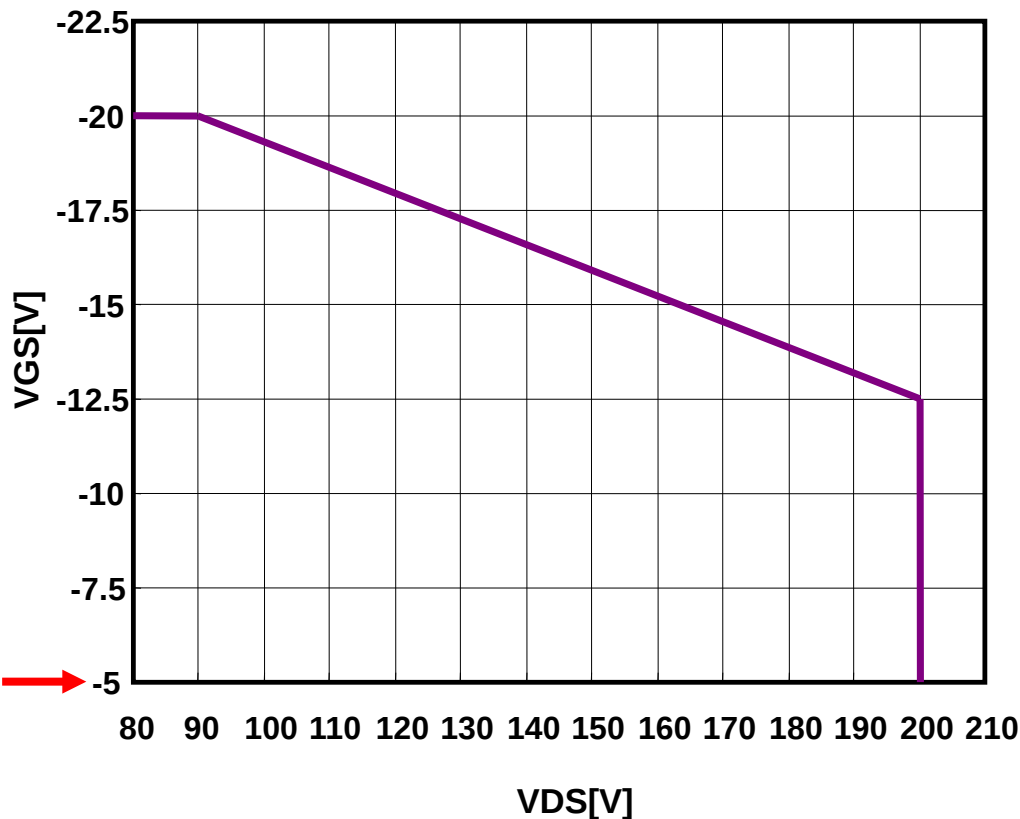
SEB Test Result of Power MOSFET

No SEB was observed up to $210V_{DS}$



SEGR Test Result of Power MOSFET

No Problem because of enough margin for SEGR



Ion : $^{58}\text{Ni}^{19+}$

Energy : 336.4MeV

LET : 25.36MeV/(mg/cm²)

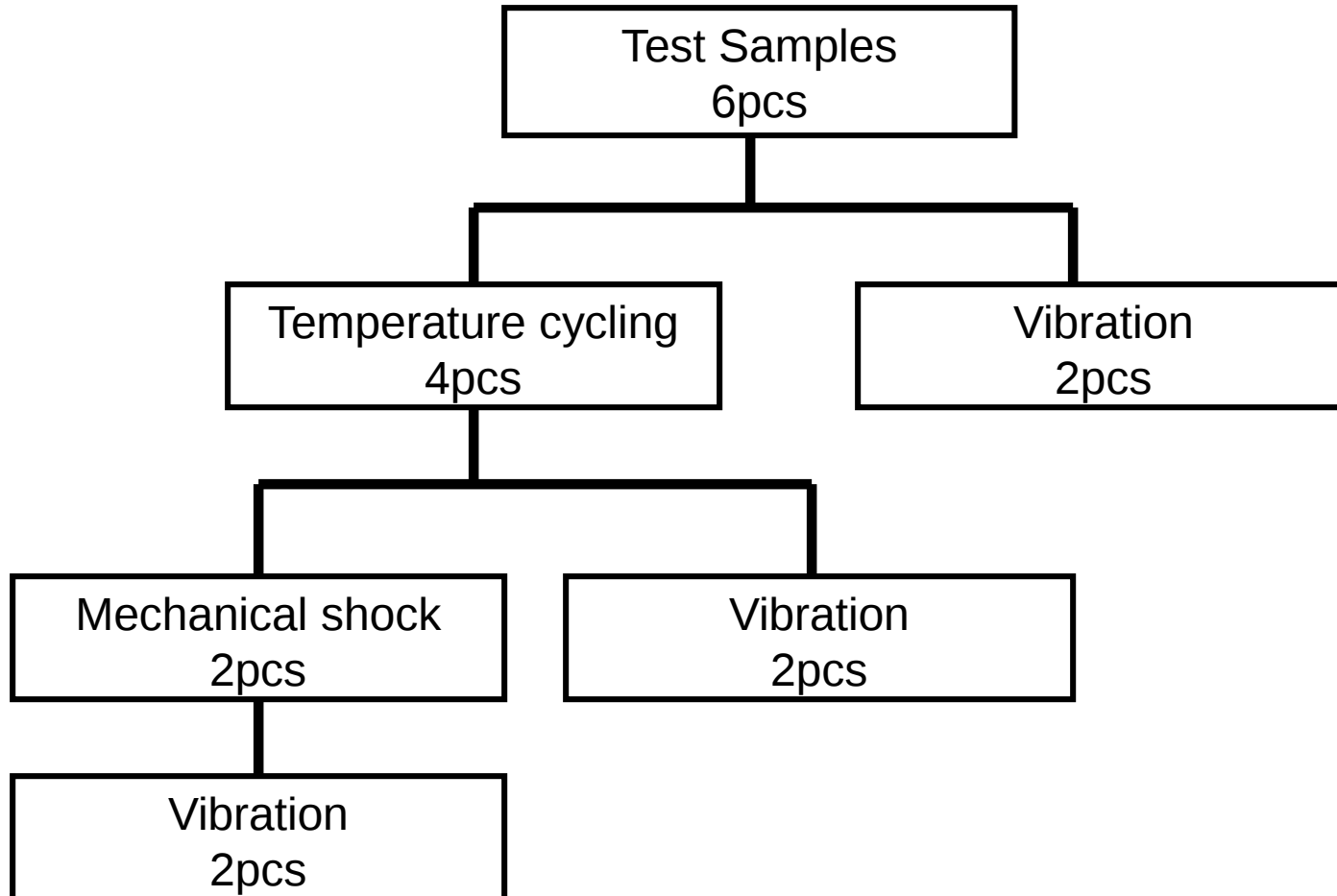
Range : 53.5 μm

Total Dose Test Result of Power MOSFET

Only small variations in all items

Parameter	Measurement Condition	Unit	Initial	$1 \times 10^3 \text{ Gy}$	
				VGS=+20V	VGS=-20V
BVDSS	ID=1mA	V	219.3	217.0	218.0
IDSS	VDS=160V	nA	7.15	40.8	24.3
+IGSS	VGS=+16V	nA	56.9	54.4	64.4
-IGSS	VGS=+16V	nA	46.0	32.4	46.0
VGS(th)	ID=1mA, VDS=5V	V	3.03	1.95	2.98
$\Delta \text{VGS(th)}$	—	V	—	-0.96	-0.17
RDS(on)	ID=5.5A, VGS=10V	m Ω	57.3	53.0	56.6

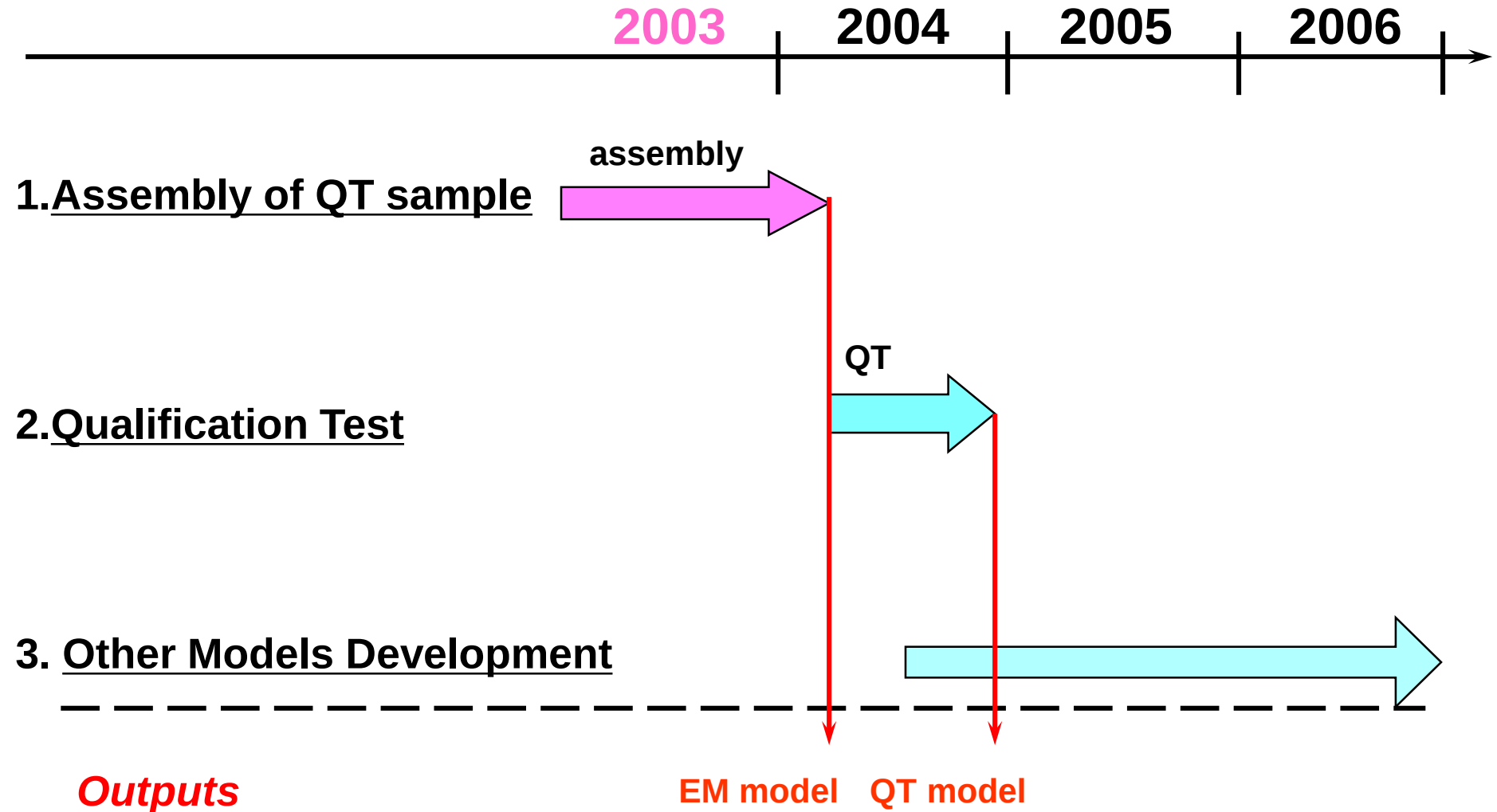
Test Flowchart



Initial Environmental Test Result

Test	Condition	IN	OUT	REJECT
Vibration	883 Method 2007 Condition A 20G, Sin, 3axis	6	6	0
Temperature cycling	883 Method 1010 Condition C -65°C/+150°C,100cyc	4	4	0
Mechanical shock	202 Method 213B Condition C 100G, 6ms,6axis	2	2	0

Development Schedule



- **New DC/DC Converter was developed with three key technologies :**
 - Triple-sided parts mounting structure**
 - Planar Transformer**
 - Analog ASIC**
- **Electrical tests confirmed its satisfactory performance in all respects.**
- **Initial environmental tests confirm its robustness against vibration, temperature, and shock.**
- **Qualification tests will start in May, 2004.**
- **QT Model will be available in November, 2004 to be followed with other models.**