eFlash Spotlight

NEPP

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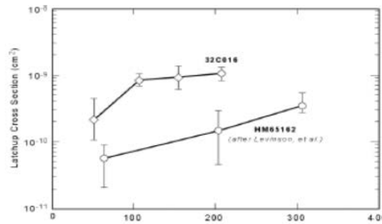
NASA Electronic Parts and Packaging Program
Technology Information for Future NASA Missions

NEWS FLASH OCTOBER 2002

FEATURES

Latchup/Latent Damage



Latent Damage From Single-Event Latchup Refutes the myth of using latchable parts in spacecraft without serious consequences…

Study of Catastrophic Latchup in the DSP2100 Signal Processor Chip for MLS Unveils a proposed mitigation strategy to reduce risk of latchup that causes immediate device destruction…

Latchup Test Considerations for Analog-to-Digital Converters Illustrates key test factors—effective ion range, current limiting, temperature, and circuit behavior during latchup…

Radiation Damage and Single-Event Effect Results for Candidate Spacecraft Electronics Presents data on SEE, Co-60 TID, and proton-induced damage on spacecraft electronics devices…

For further information on latchup/latent damage…

Tin Whiskers

Tin Whisker Observations on Pure Tin-Plated Ceramic Chip Capacitors Proves that MLCCs are not immune to tin whisker formation and highlights the confounding nature of tin whiskers…

Tin Whiskers: Attributes and Mitigation Analyzes problematic issues of tin whisker formation on passive components, summarizes recent experiments, and discusses practical recommendations…

Effects of Conformal Coat on Tin Whisker Growth Measures protective effects of Uralane coating on initiation/growth of tin whiskers, its ability to prevent or inhibit emergence of tin whiskers, and its ability to prevent shorting…

Tin Whiskers: Revisiting an Old Problem Describes tin whisker characteristics and formation and suggests strategies to reduce tin whisker risk on space flight hardware…

For further information on tin whiskers…

Other Topics

Overview of Ball Grid Array and Chip Scale Packaging Technology Presents a synopsis and pros and cons for designing, manufacturing, and testing printed wire assemblies populated with BGAs and CSPs…

Destructive Physical Analysis (DPA) Statistics, July Through September 2002 Shows recent DPA statistics by sample quantity, job type, part number, and project…

SPECIAL EVENTS

Virtual Conference on Plastic Encapsulated Microcircuits (PEMs) for Use in Space December 5, 2002, using Web-Ex at your computer station or in an e-room; for details, contact Dory Josephson, 301.286.7927 or Philomin.D.Josephson.1@gsfc.nasa.gov.

For other upcoming special events…
Next Issue of EEE Links…

Latchup/Latent Damage

For further information on latchup/latent damage, visit the GSFC Radiation Homepage at http://radhome.gsfc.nasa.gov and the JPL Electronic Parts Engineering page at http://nppp.jpl.nasa.gov.

Latent Damage From Single-Event Latchup

Heidi N. Becker, Tetsuo F. Miyahira, and Allan H. Johnston, NASA JPL/California Institute of Technology

This research illuminates the serious consequences resulting from flying latchable parts. Becker et al. detected evidence of melting, voiding, and fracturing of metallization; insulator/dielectric cracking; and globules of metal that could potentially cause short circuits in microcircuits that had suffered an SEL event. A full description of the characteristic physical signatures of latent damage is included, along with key parameters of these types of events. By using scanning electron microscopy and energy dispersive spectroscopy to detect and characterize latent damage in microcircuits that have suffered SEL, the research highlights the need for greater caution. Projects need to look for evidence of latent damage after the SEL test and ensure that current densities during latchup were low enough that damage to metallization and dielectrics is improbable.

To view the full-length article, go to http://nppp.jpl.nasa.gov/docs/Latent_Damage.pdf.

Study of Catastrophic Latchup in the DSP2100 Signal Processor Chip for MLS

Heidi N. Becker, Allan H. Johnston, and Tetsuo F. Miyahira, NASA JPL/California Institute of Technology

This report summarizes the results of a series of tests to characterize catastrophic radiation-induced latchup in the DSP2100, which is used in three different applications on MLS. Latchup has been observed by JPL as well as by two other test organizations (Aerospace Corporation and ESA) in heavy-ion tests of DSP2100 devices. Tests were done on devices from the same date code used in MLS. Those results were reported in an internal JPL Test Report in April 2001. Heavy-ion data from these reports were used to calculate expected latchup rates for MLS. The estimated rates were 0.102 per year from heavy ions, and 1.7 per "design-case flare." Those rates apply to each part. Three DSP2100 devices are used on MLS, increasing the latchup probability by three.

To view the full-length article, go to http://nppp.jpl.nasa.gov/docs/MLSLatchup-Cf2.pdf.

Latchup Test Considerations for Analog-to-Digital Converters

Allan H. Johnston and Tetsuo F. Miyahira, NASA JPL/California Institute of Technology

Many CMOS circuits are sensitive to latchup from heavy ions, and latchup is one of the major considerations when CMOS devices are evaluated for space applications. Radiation-induced latchup has been studied for many years, but it

remains a difficult problem in actual circuits because latchup sensitivity inherently depends on the layout and distribution of contacts, power, and ground within complex circuits. The gain of the parasitic bipolar transistors that form potential latchup paths is nearly always high enough so that latchup can potentially occur. However, the key factor in latchup sensitivity is the external resistance across the base-emitter junctions of the two parasitic transistors, not the transistor gain.

To view the full-length article, go to http://nepp.nasa.gov/index_nasa.cfm/478/BC46BBB1-3E90-42D5-982DDBDFC641DB28/.

Radiation Damage and Single-Event Effect Results for Candidate Spacecraft Electronics

Martha V. O'Bryan, Raytheon ITSS, Kenneth A. LaBel, NASA GSFC, Robert A. Reed, NASA GSFC, James W. Howard, Jr., Jackson & Tull Chartered Engineers, Ray L. Ladbury, Orbital Sciences Corporation, Janet L. Barth, NASA GSFC, Scott D. Kniffin, Orbital Sciences Corporation, Christina M. Seidlick, Raytheon ITSS, Paul W. Marshall, Consultant, Cheryl J. Marshall, Consultant, Hak S. Kim, Jackson & Tull Chartered Engineers, Donald K. Hawkins, NASA GSFC, Anthony B. Sanders, NASA GSFC, Martin A. Carts, Raytheon ITSS, James D. Forney, Jackson & Tull Chartered Engineers, David R. Roth, Applied Physics Laboratory, James D. Kinnison, Applied Physics Laboratory, Elbert Nhan, Applied Physics Laboratory, and Kusum Sahu, QSS Group, Inc.

We present data on the vulnerability of a variety of candidate spacecraft electronics to proton and heavy-ion induced single-event effects and proton-induced damage. We also present data on the susceptibility of parts to functional degradation resulting from total ionizing dose at low dose rates (0.003–4.52 rads (Si)/s). Devices tested include optoelectronics, digital, analog, linear bipolar, hybrid devices, Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), and DC-DC converters, among others.

To view the full-length article, go to http://radhome.gsfc.nasa.gov/radhome/papers/nsrec00_W21.pdf or http://nepp.nasa.gov/DocUploads/7EE2C982-FBCC-4931-BFCCB4FCB78B2560/nsrec01_W15.pdf.

Tin Whiskers

For further information on tin whiskers, visit the Tin Whiskers Homepage at http://nepp.nasa.gov/whisker.

Tin Whisker Observations on Pure Tin-Plated Ceramic Chip Capacitors

Jay Brusse, QSS Group, Inc.

Tin whiskers pose a risk of intermittent short circuits in terrestrial applications and potentially catastrophic metal vapor arcs in space (vacuum) environments. Research on whiskering and mitigation practices has historically produced highly variable results. These variations and recurring observations of whisker-induced failures are central to the high reliability community's reluctance to adopt lead-free finish alternatives, especially pure tin, until clear evidence exists that the factors affecting whisker growth are understood and can be controlled. This paper highlights the variability of previous claims using recent observations of greater than 200-μm-long whiskers on pure tin-plated

ceramic chip capacitors as a classic example of the confounding nature of this phenomenon.

For more information, contact: Jay Brusse, Senior Components Engineer, QSS Group, Inc. at NASA Goddard Space Flight Center, Bldg. 22, Room 036, Greenbelt, MD 20771, Jay.A.Brusse.1@gsfc.nasa.gov. This paper was presented at the Electronics Finishing II Session and published in the official proceedings of AESF SUR/FIN 2002, June 24-27, sponsored by the American Electroplaters and Surface Finishers Society, Orlando, FL. Posted with permission of the AESF.

To view the full-length article, go to http://nepp.nasa.gov/whiskers/references/tech_papers/brusse_2002_sur_fin_paper.pdf.

Tin Whiskers: Attributes and Mitigation

Jay A. Brusse, QSS Group, Inc., Gary J. Ewell, The Aerospace Corporation, and Jocelyn P. Siplon, The Aerospace Corporation

The movement to eliminate lead (Pb), especially active in Japan and the European Union, has resulted in an increasing use of pure tin (Sn) coatings on leads and other external and internal surfaces of capacitors, resistors, and other passive components. This paper discusses the issues of tin whisker growth with respect to passive components. It also presents both a critical analysis of existing published documents on tin whisker nucleation and growth and a summary of very recent experiments that provide further understanding of the potential means of whisker formation mitigation. Many of the proposed mechanisms for mitigation, including control of the immediate underplating material, use of conformal coating, regulating the thickness of the tin coating, use of matte tin electroplating, and annealing or fusing of the tin layer, are inadequate. They are likely to reduce the incidence of nucleation or growth but do not provide an absolute guarantee of lack of whisker formation.

To view the full-length article, go to http://nepp.nasa.gov/index_nasa.cfm/478/5A676ED4-A9EF-4F3E-975B05515589AF7F/.

Effects of Conformal Coat on Tin Whisker Growth

Jong S. Kadesch, Orbital Sciences Corporation/NASA GSFC, and Henning Leidecker, NASA GSFC

A whisker from a tin plated part was blamed for the loss of a commercial spacecraft in 1998. Although pure tin finishes are prohibited by NASA, tin plated parts, such as hybrids, relays, and commercial-off-the-shelf (COTS) parts, were discovered to have been installed in NASA spacecraft. Invariably, the assumption is that a conformal coat will prevent the growth of, or short circuits caused by, tin whiskers. This study measures the effect a Uralane coating has on the initiation and growth of tin whiskers, on the ability of this coating to prevent a tin whisker from emerging from the coating, and on the ability to prevent shorting.

To view the full-length article, go to http://nepp.nasa.gov/whisker/article/kadesch.PDF.

Tin Whiskers: Revisiting an Old Problem

Jay Brusse, QSS Group, Inc.

Recent events have reminded the space community of the potential risks associated with the use of pure tin-plated finishes on electronic components and assemblies. Pure tin finishes are susceptible to the spontaneous growth of single crystal structures known as tin whiskers. Tin whiskers are capable of causing electrical failures ranging from parametric deviations to catastrophic short circuits. Although the tin whisker phenomenon has been documented for decades and is reasonably well understood, it is still a reliability hazard that warrants special attention.

This article does not provide a complete explanation of the tin whisker growth mechanism; numerous (often contradictory) publications have attempted this task. The intent is to provide a comprehensive explanation of generally accepted understandings of tin whiskers along with some suggestions for how to reduce the risk of tin whiskers on space flight hardware. In addition, Goddard Space Flight Center is maintaining a Tin Whisker Information Homepage to provide regular updates to facts and findings as they become available.

To view the full-length article, go to http://nepp.nasa.gov/index_nasa.cfm/478/2B1FC8E9-4AF1-4F2F-837213A632C25CE9/.

Other Topics

Overview of Ball Grid Array and Chip Scale Packaging Technology for Space Flight Missions

Reza Ghaffarian, NASA JPL/California Institute of Technology

This document provides an overview for designing, manufacturing, and testing printed wiring assemblies populated with ball grid arrays (BGAs) and chip scale packages (CSPs). NASA Headquarters, Code AE, has funded JPL for the last several years to investigate the use of BGAs and CSPs for potential space flight missions. Within the last 2 years, a few types of BGAs have been qualified for NASA missions including X-2000 and Mars Exploration Rover, and are currently being qualified for Mars05.

The full-length article is currently being updated; upon completion, it will be posted on the NEPP Web site at http://nepp.nasa.gov.

Destructive Physical Analysis (DPA) Statistics, July Through September 2002

Darryl Lakins, NASA GSFC

DPAs in the table below were conducted at the GSFC Parts Analysis Lab.

Sample Qty.	Job Type	Part Number	Project
2	DPA	5962-9163901MFA	ASTROE2
2	DPA	ADDAC87D-DB1-V/88SB	ASTROE2
3	DPA	JANTXV2N222A	ASTROE2
3	DPA	JANTXV2N2907A	ASTROE2
3	DPA	5962-8984106LA	HST
5	DPA	CND2047-DAF/20	ST-5
3	DPA	5962-8874801UA	ASTROE2
2	DPA	JANTXV2N2905A	ASTROE2
3	DPA	M38510/13503BPA	ASTROE2
2	DPA	5962-9164001MFA	ASTROE2
2	DPA	5962H9215314QNC	ASTROE2
3	DPA	M8340110H1001FA	ASTROE2
3	DPA	M8340110H1002GA	ASTROE2
3	DPA	OP-221AZ/883Q	ASTROE2
1	DPA	7389-2030-09	MLA
2	DPA	M39016/29-057M	ASTROE2
2	DPA	5962--88762016A	ASTROE2
5	DPA	HMC220MS8	ST-5
5	DPA	RF2422	ST-5
3	DPA	H0705CPX2R00F10	ST-5
1	DPA	5962-0150802QYC	ST-5
12	DPA	66099-103	SWIFT
3	DPA	M38510/14103BEA	ASTROE2
3	DPA	5962-7705301XA	ASTROE2
5	DPA	CDR35BX334AKUS	SWIFT
5	DPA	CDR35BX334AKUS	SWIFT
5	DPA	CDR32BX333AKUS	SWIFT
5	DPA	CDR32BX333AKUS	SWIFT
5	DPA	CDRBX333AKUS	SWIFT
2	DPA	CD4047BKMSR	SWIFT
5	DPA	OP296GS	SWIFT
3	DPA	JANTXV2N3741	HST
5	DPA	CDR35BX474AKUS	SWIFT
3	DPA	5962-015-803QYC	AKTEL
3	DPA	JANXV1N5550	HST

3	DPA	MAX4503EVK	SWIFT
5	DPA	MAX4503EUK	SWIFT
5	DPA	JANTXVIN5331B-1	HST
3	DPA	JANTXVIN962B-1	HST
5	DPA	AMP03BH/883	ASTROE2
2	DPA	MN6400S/BCH	ASTROE2
5	DPA	JANTXV1N914	ASTROE2
5	DPA	JM38510/12802BGA	ASTROE2
5	DPA	5692-8757103XA	ASTROE2
5	DPA	AD648TQ/883B D/C0145A	ASTROE2
5	DPA	AD648TQ/883B D/C0145B	ASTROE2
1	DPA	5962-9320901MPA	ASTROE2
5	DPA	JM38510/11301BEA	ASTROE2
5	DPA	5962-8954401GA	ASTROE2
5	DPA	M38510/11202BPA	ASTROE2
2	DPA	5962-8757103XA	ASTROE2
3	DPA	JANTX1N1202A	ASTROE2
3	DPA	DAC349-12	ASTROE2
3	DPA	M3840110H2261FA	ASTROE2 ACHE
3	DPA	MCM2668-1M/1.6894MHZ	ASTROE2 ACHE
2	DPA	CR-101/U-12M00000	ASTROE2 ACHE
3	DPA	HS9-6617RH-Q	ASTROE2
2	DPA	9409-007-02BF	ASTROE2
2	DPA	9201-043-02B	ASTROE2
1	DPA	9409-002-02B-09911A	ASTROE2
3	DPA	M38510/13503BPA	ASTROE2
1	DPA	9409-002-02B-0114A	ASTROE2
2	DPA	9203-023-02B	ASTROE2
2	DPA	9201-052-02B	ASTROE2
2	DPA	9204-026-02B	ASTROE2
3	DPA	5962H9584501QYC	ASTROE2 CAP/CDP
2	DPA	787RPFB	ASTROE2CAP
3	DPA	HCST85KMSR	ASTROE2 ACHE
3	DPA	B767747-013	SWIFT
2	DPA	5962-8953402MXA	HST
5	DPA	87016C5002FC	ST-5
2	DPA	JANTXV2N5794	HST WFC3
3	DPA	M8340110H1003JB	ASTROE2 ACHE
2	DPA	66099-415	SWIFT
2	DPA	JANTXV1N4099-1	HST
2	DPA	JANTXV1N4103-1	HST
5	DPA	87016C2002FC	ST-5

5	DPA	CDR33BX104AKUS	ST-5
5	DPA	JANTXV1N5807	HST WFC3
2	DPA	M6106/38-004	HST
3	DPA	5962-8605305A	HST
3	DPA	AD549SH/883B	HST
3	DPA	JANTXV1N4467	ASTRO-E2 ACHE
3	DPA	RF2667	ST-5
3	DPA	TPS9103PWR	ST-5
5	DPA	OP420GS9940	SWIFT
1	DPA	KM48C8000B5-6	SWIFT

For further information, contact Darryl Lakins, Code 562 Branch Head, at 301.286.6631 or dlakins@pop500.gsfc.nasa.gov.

Special Events

For an up-to-date events listing, see the Calendar on the NEPP Web site at http://nepp.nasa.gov.

Workshop on Thermal Packaging of High Flux Military and Commercial Electronics
October 7-10, 2002, Grand Ballroom, Stamp Student Union, University of Maryland, College Park, MD
For details, contact Dr. Michael Ohadi, ohadi@eng.umd.edu, 301.405.5263, or see Web site http://www.s2ts.umd.edu/registration.htm

CALCE Technical Review and Planning Meeting
October 8-10, 2002, Grand Ballroom, Stamp Student Union, University of Maryland, College Park, MD
For details, contact Joan Yuan, joanyuan@eng.umd.edu, 301.405.1905, or see Web site http://www.calce.umd.edu

International Test Conference
October 8-10, 2002, Baltimore Convention Center Baltimore, MD
For details, contact Jill Sibert, j.sibert@advantest.com, 610.758.8190

Optoelectronics Packaging and Microoptoelectromechanical Systems (MOEMS)
October 8-11, 2002, Bethlehem, PA
For details, contact Rajeshuni Ramesham, rajeshuni.ramesham@jpl.nasa.gov, 818.354.7190, or see Web site www.imaps.org

World Space Congress 2002
October 10-19, 2002, George R. Brown Convention Center, Houston, TX
For details, contact World Space Congress, www.aiaa.org/wsc2002, 800.639.2422, or see Web site www.aiaa.org

IMAPS Advanced Technology Workshop (Optoelectronics Packaging)
October 11-14, 2002, Radisson Hotel, Bethlehem, PA
For details, contact Bill Heffner, wheffner@agere.com, 202.548.4001, or see Web site www.imaps.org/callfor/atw2001opto.htm

Virtual Conference on Plastic Encapsulated Microcircuits (PEMs) for Use in Space
December 5, 2002, using Web-Ex at your computer station or in an e-room
For details, contact Dory Josephson, Philomin.D.Josephson.1@gsfc.nasa.gov, 301.286.7927

Coming Soon

Articles are being accepted for the December 2002 issue of EEE Links.

Guidelines for EEE Links Article Submission

EEE Links is a quarterly publication. The next publication date and focus will be:

December 2002 – Plastics
Article submission deadline is November 15, 2002.

Submitting articles for EEE Links is a great means by which to transfer information and knowledge inside and outside of the NASA community.

EEE Links supports the NASA Electronic Parts and Packaging Program (NEPP), and the information presented in this newsletter augments electronic parts, packaging, and radiation technologies.

EEE Links publishes many types of articles relevant to electronic parts, packaging, and radiation. Primary consideration is given to articles that relate specifically to the NEPP program, but we also consider articles outside of the NEPP program that address electronic parts, packaging, or radiation issues.

Article submissions can cover current efforts, referencing status and completion date. Articles can be informal and be from one paragraph to three pages in length on the following subjects:

- Current Events Within the NEPP Program and Projects
- Parts
- Packaging
- Radiation
- Reliability Issues Concerning NEPP
- New/Emerging Technology
- Space Flight Hardware
- Quality Assurance Issues.

To submit an article, please send it in a text-only format, preferably Microsoft Word, to Jeanne Beatty at jbeatty@pop500.gsfc.nasa.gov. Please provide the following information with your article submission:

- Abstract: This two- to four-sentence paragraph summarizes the key points to capture the reader's attention.
- Contact Information: The author must include his or her business address, phone, fax, and e-mail address.
- Notes and References: Most articles require some references, and some contain incidental information best treated as notes. Use brackets for references and superscripts for notes, then list the two groups separately at the end of the article. These should be numbered in the order in which they appear in the article, not alphabetically.
- Additional Reading: Our readers appreciate pointers to relevant books and articles. List these at the end of the article in the same format as the references.
- Copyright: The author is responsible for obtaining any copyright releases or other releases necessary for their

article. The releases should be forwarded to the EEE Links Editor (see Jeanne Beatty's e-mail address above).

- Biography (to be supplied when requested): This should be between 50 and 75 words outlining the author's job, background, professional accomplishments, and other pertinent accolades or areas of interest. Accompanying photographs might be requested also; these should either be in .gif or .jpg format if possible.

Letters to the Editor

Please limit letters to 250 words. Include your name, phone number, and e-mail address. Names are withheld from publication upon request. We reserve the right to edit for style, length, and content.