SYNOPSIS V1.0: Proton and Heavy Ion Single Event Effects Testing of a 12.5 GHz Pseudo-Random Number Generator Designed by Mayo Foundation and Fabricated in IBM 7HP SiGe

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Heavy Ion Test Date: 8/12/02

I. INTRODUCTION

Dynamic Single Event Upset (SEU) measurements on devices operating in the multi-GHz regime have shown that the SEU test results can depend strongly on the frequency of operation of the device. Since emerging satellite applications using the compound semiconductor InP and SiGe devices are for data rates from ~1.5 to 100 GHz, it is critical to predict on-orbit performance using relevant, at-speed, ground testing.

New high speed, low power technologies including SiGe and InP Heterojunction Bipolar Transistor (HBT) technologies are rapidly becoming available to spacecraft designers. SiGe HBT technology offers device performance competitive with existing III-V technology while maintaining the cost and yield advantages associated with conventional silicon manufacturing. In addition, the natural compatibility of SiGe HBT technology with CMOS fabrication schemes has allowed the realization of an aggressive SiGe HBT BiCMOS technology from IBM, and thus potentially enables a host of Si-based System On A Chip (SOAC) solutions for the rapidly emerging commercial communications infrastructure, for NASA and for military applications. InP HBT technology is also very promising for its ultra high frequency potential.

Previous work has observed negligible radiation induced degradation from proton induced total ionizing dose and displacement damage effects in the SiGe HBT process out to the 5 megarad level! However, SEU sensitivities require substantial attention.

In general, SEU sensitivity is enhanced at the clock edge, and for very high-speed technologies this presents a significant hardening challenge. The data rate dependence of the SEU rates observed in these technologies must be characterized to ensure that the proper ground tests are performed for meaningful on-orbit predictions.

This study was undertaken to determine the proton and heavy ion-induced SEU sensitivity of a PRN fabricated in IBM 7HP HBT SiGe technology over frequency. DTRA supported Mayo Foundation to design and fabricated the device. GSFC/NASA and DTRA supported Mayo Foundation to package the PRN and support the radiation testing.

II. DEVICES TESTED

The device module consists of a high performance dielectric Printed Circuit Board (PCB) mounted to an aluminum or brass ~100 mil substrate, see Figure 1. The Device Under Test (DUT) die is mounted on top of the PCB as are various capacitors. The DUT board was designed and assembled by Mayo Foundation. All SMA and SMB connectors are mechanically mounted to the "underside" of the PCB/substrate with the shields connecting directly to the substrate (V_{ee}), with the center conductors passing through the substrate and PCB to solder connections to traces on the top of the PCB. This is a special package configuration that allows easy line-of-site exposures during radiation testing. The die connections to the PCB traces are by wirebond as are the thin-film capacitor top-side connections to the PCB. Hex standoffs at the corners of the top of the PCB hold a clear plastic protective cover in place. Additional hex standoffs on the bottom of the PCB provide protection for the SMA and SMB connections and also provide mounting points for the DUT. The plastic cover was not removed for this proton test.

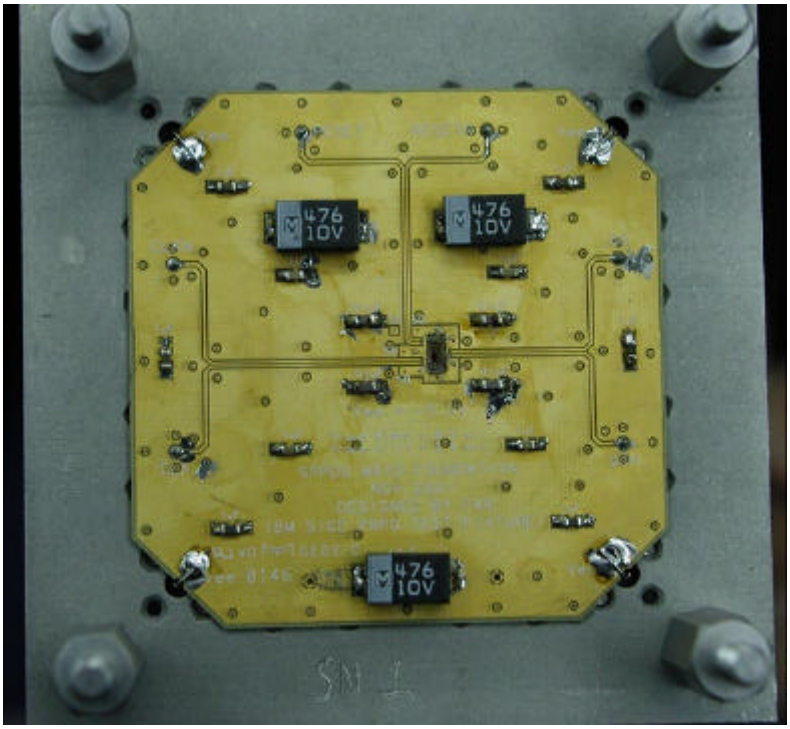

Figure 1. Picture of the high performance dielectric printed circuit board. The PRN is mounted near the center of the board. The input and output SMA and SMB connectors are mounted on the far side. (The plastic cover has been removed in this picture).

The DUT is a 2^7-1 PRN fabricated in IBM 7HP SiGe process. It was designed by Mayo Foundation and fabricated by IBM under a DARPA contract. Mayo Foundation packaged the DUT under GSFC contract. It consists of 7 flip-flops in series, with the output of the last two stages XORed and fed back to the input of the first stage. All permutations of states of the 7 flip-flops are generated except all zeros (which condition is referred to as the "zero state", and which does not sequence to any other state), giving a sequence of 127 (one less than the number of states representable with 7 bits, 2^7 = 128). Because of the particular implementation of this circuit the sequence is generated in reverse order from what is considered the standard PRN7 sequence.

The DUT has two truly differential inputs, a clock signal (CLK and CLK_{bar}) and a reset signal (R and R_{bar}) to help recover from the zero-state. High level for both is 0 V_{dc}. Low level for both is –0.3 V_{dc}. The single DUT output is also truly differential, with the same levels (300 mVpp on –150 mVdc).

The inputs and outputs supplied to the DUT module are expected to be proper 50 ohm male SMA transmission lines.

The circuit is powered with 5 volts, and is positive-supply referenced, so ground and –5 volts is used as with normal Emitter Coupled Logic (ECL). V_{cc} is ground, which is the signal connector shield voltage. V_{ee} is –5.0 Vdc. V_{ee} and V_{cc} are supplied by four parallel SMB snap-on connectors on the corners of the module.

III. TEST FACILITIES

Proton Facility: Indiana University Cyclotron Facility
Flux Range: $1.7x10^9$ to $1.9x10^{10}$ particles/cm^2/s.
Proton Test Energy: 198-203 MeV

Heavy Ion Facility: Texas A&M Cyclotron Facility
Flux Range: 1.8x10^3 to $5.4x10^{10}$ particles/cm^2/s.
Cyclotron Tuned Energy: 15 MeV/amu and 40 MeV/amu

Table 1. Heavy Ion Used:

Ion	Energy (MeV/amu)	Linear Energy Transfer (LET) ($MeVcm^2/mg$)
Ne	40	1.2
Ar	40	3.9
Ar	15	8.9
Kr	15	28

(Note: angle between DUT and beam path were varied to obtain the Effective LETs)

IV. TEST METHODS

The test setup reflects the operational needs of the DUT (especially handling 12.5 GHz digital signals and providing a static-safe environment to these exceptionally static-sensitive parts) as well as the radiation environment (specifically, establishing particle beam access to the DUT and accommodating generated stray neutron flux). This section describes the test setup and discusses these issues.

IV.A Test Hardware Description

Figure 2 gives a block diagram of the test setup. The test controller is a National Instruments PXI (PCI eXtension for Instrumentation; essentially this is cPCI, Compact PCI) format computer (PXI-8176) with a General Purpose Instrumentation Bus (GPIB) port, running the Win98 operating system. The test application program is written in the Labview 6.0 environment. The program controls and reads data from the test equipment and logs data for further processing. More details on the test application program follow further below.

The frequency source is an HP 83712B 10 kHz to 20 GHz CW signal generator, "SigGen". Frequency and nominal output power are controlled by GPIB.

The SigGen output is split via a 3 port, 6 dB, resistive splitter, which ensures that at all frequencies every port is 50 ohms, so that no energy is reflected from any port. The nominal drop from input to either output is 6 dB, or half-voltage, so that ¼ of the input power comes out each of the two outputs.

One output of the first 6 dB splitter feeds a second 6 dB splitter, which supplies both the Anritsu Bit Error Rate Tester (BERT) and a power meter. Both of these are discussed later. The other output of the first 6 dB splitter feeds a balanced-unbalanced converter (balun). This type of balun is bi-directional, so that either one signal can be split into two, out-of-phase, signals, or two complementary signals can be added to form one single-ended signal. Either way, about 8 dB of loss is incurred. Within this balun, a 6 dB splitter feeds both an inverting transformer as well as a short (non-inverting) transmission line, so that both inverted and non-inverted signals are available. Careful design of the Picoseconds Pulse Laboratories PPL5315A ensures that the phase relationship of the two outputs up thru 17 GHz is kept to within +/- 2 ps, making it suitable for use in these tests.

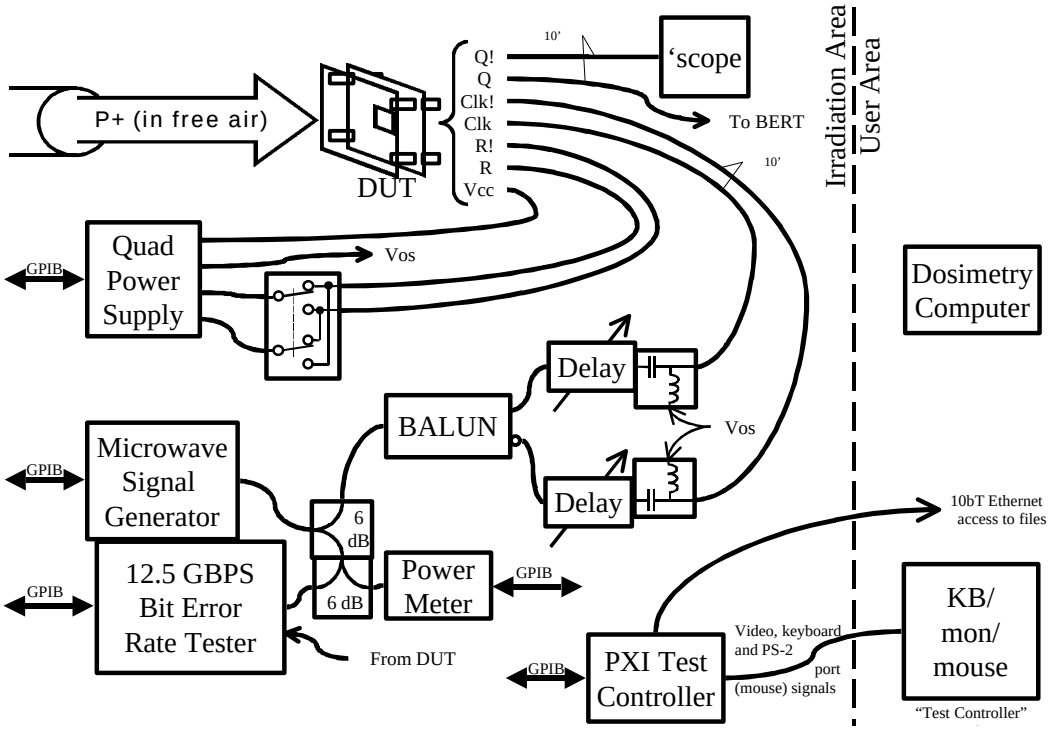

Figure 2. Block Diagram of test setup.

Each of these complementary clock outputs of the balun feeds an adjustable delay line, which is essentially a telescoping piece of coaxial cable. A locking nut prevents or allows change in the physical, and thus electrical, length, to accommodate potential differences in overall delay between the balun input and the DUT clock inputs.

In practice, at the highest operational frequency (at which the sensitivity to small delay adjustments is highest) a considerable adjustment of this differential delay was seen to have no effect on the performance of the circuit. Specifically, change in the differential signal delay by X ps at the DUT clock inputs caused no change in the pattern eye width/position, as measured by operational delay-setting range/center, at the BERT. Changing both the delays in common caused the optimum phase relationship between clock and input data at the BERT to shift by X/2 ps (which is expected). The delay adjusters were thus set equally, in the middle of their range.

Each of the adjustable delay lines feeds a bias-T, which allows the addition of a DC voltage (labeled "V_{os}" in the block diagram) onto the output of the bias-T without affecting the incoming signal's DC level. This is detailed in the bias-T symbols in Figure 2. Bias-Ts are necessary because the DUT clock input levels are designed to be –300 mV (low level) and 0 mV (high level), which is 300 mVpp with a DC offset of -150 mVdc.

In general, care has been taken to make components mate directly with each other without cables when possible to eliminate cabling effects (e.g. between the balun and the delays and the bias-Ts). Coaxial cabling is nonetheless necessary--The RF coaxial cable type used throughout the test setup, Semflex, Inc. DKT type, is rated to 18 GHz. Short (2') lengths of this are used where

possible, but between the test equipment and the DUT a larger separation is necessary to allow for positioning and rotation of the DUT in front of the beam, in addition to reducing the stray neutron flux at the equipment during proton irradiations.
Other comments on RF connections:

- SMA connector type is used generally. Elbows, male-to-female solid adapters with a 90 degree bend, are used where necessary to alleviate cable strain.
- Short, 6", pieces of thin (high flexibility) coax are inserted between the DKT coax and the DUT, at all six SMA connections.
- Although the extra connectors and lesser performance of these short coaxes impacts performance, using these lessen the mechanical forces on the DUT connector and PCB trace solder joint.
- All SMA connections are hand-tightened, and after the test setup is laid out as it will be used, each connection is torqued to specifications with use of an SMA torque wrench (There are significant differences in reflection/transmission thru an SMA connection that is hand-tightened vs properly torqued, and overtightening with a non-torque limiting wrench both damages the connectors and deteriorates the reflection/transmission quality of the connection.

Differential clock (CLK, CLKbar) is supplied to the DUT. Supply of a differential reset signalis described below. The DUT's differential data outputs (Q, Qbar) are both carried via the same kind of cabling (6" flexible plus 10' DKT) to the test equipment. The uninverted signal feeds the BERT (described below). The inverted signal either feeds an oscilloscope for diagnostics or is properly terminated.

The heart of the test system is the Anritsu MP1764A , a 12.5 GBPS (Giga Bit Per Second) BERT, supplied by NRL (Naval Research Laboratory). It provides error detection of an incoming serial data stream, given a synchronizing clock signal and knowledge of the expected data. The data in this case is a PRN-7 (Pseudo-Random Number, 7 bit, which is $2^7 - 1 = 127$ bits long) sequence. This DUT generates a PRN-7, which is similar to the standard pattern, except that it is generated backwards. The BERT's internal PRN-7 pattern cannot be used, because of this. Instead, the BERT's user-defined pattern function is used, with the pattern manually programmed into it.

The DUT's differential reset signal inputs (R, Rbar) are nominally RF-capable, but in practice they are fed with DC. Their use is to recover the DUT from a possible, though normally not occurring, state where all flip-flops are set to zero. When the differential reset signal transitions from active to inactive (with the differential clock signal is active) DUT reset occurs, regardless of whether R and Rbar switch slowly and/or simultaneously. Thus, for reasons of simplicity, the reset signals are generated with either a power supply or a manual toggle switch. Two outputs of the quad-output power supply normally provide inactive reset HI and LO (–300 mVdc and 0 Vdc, respectively). These are swapped and then swapped back to normal in order to perform a reset. This can be done either programmatically by changing the supply levels, or by momentarily switching a double-pole double-throw toggle switch. RF cabling from the switch box to the DUT was used for convenience instead of for signal integrity.

The DC component of the clock supplied to the DUT is as invariant as the power supply output providing it. It does not vary over frequency or as AC level varies. In contrast, the AC level supplied by the system to the DUT input connectors varies substantially, and non-monotonically, as frequency changes. These DUTs are extremely sensitive in some ways (specifically, they are amazingly susceptible to static damage), so damage by RF over-drive is a concern. Also, other types of devices have been found to have a single event cross section which varies substantially with input drive level. Thus, care to drive the DUT with a precisely controlled clock signal as possible was taken.

Each time the test setup is connected, the amplitude response of the entire clock drive path (SigGen → Splitter → Balun → Bias-Ts → Delays → Long coax →Short coax) is characterized at all frequencies considered for operation:
With the DUT unconnected, three sweeps of RF power vs SigGen frequency setting are made. CLK, CLKbar, and the second 6dB splitter output levels are measured using the power meter at a constant SigGen power level (with the two other signals properly terminated, of course). Then, the greater of CLK and CLKbar (the level of the Balun outputs vary even in relation to each other) is used to calculate the required SigGen setting for 300 mVpp at the DUT CLK (or CLKbar) input. Because the greater of the two clock input levels was used in the calculation the other clock input level will either be the same or less than the one set to 300 mVpp. Finally, the second 6dB splitter level expected at the calculated SigGen setting for each frequency is figured and used to monitor proper operation, and the power meter is reconnected to its normal position, the second 6dB splitter output. Test software does not allow operation at other than these power-swept frequencies in case the power level at that frequency spikes up and presents a damage danger to the DUT. The sweep data and calculations are stored in a file called BALUN.txt in order to persist through program and power cycles. Note that it is considered safest to regenerate these numbers each time the RF portion of the test setup is reconstructed or modified.

The quad output power supply supplies four channels of constant voltage to the test setup. Channels 1 and 2 are R and Rbar, respectively. Channel 3 is the DC offset voltage (Vos) added the the RF signal at the bias-Ts. Channel 4 is the DUT power supply, which is fed to the DUT via four (parallel) SMB snap-on connectors.

The test application program controls the test equipment (see Figure 3), reads data from the test equipment, logs data, and restricts control of the equipment to ensure that safe operation and safe sequencing are followed. When the program is started all of the equipment is initialized, including the power supply, the RF power meter, the signal generator, and the BERT. The power-on sequence, is: GPIB interface takes control of the bus. SigGen RF output OFF, with frequency set to 1.000 GHz and power level set according to latest calculated value. Power meter initialized and zeroed, with an option to connect it to its reference output for calibration. Power supply outputs OFF, with voltage and current settings appropriate for the test needs, and with over-current protection OFF. BERT is initialized with settings such as pattern type, phase delay, threshold voltage, etc. set appropriately for this test. Also, the BERT is set to make use of the GPIB service request interrupt function, so that when certain events occur (loss of sync) an immediate report to the PXI controller (on which the test application is running) is made.

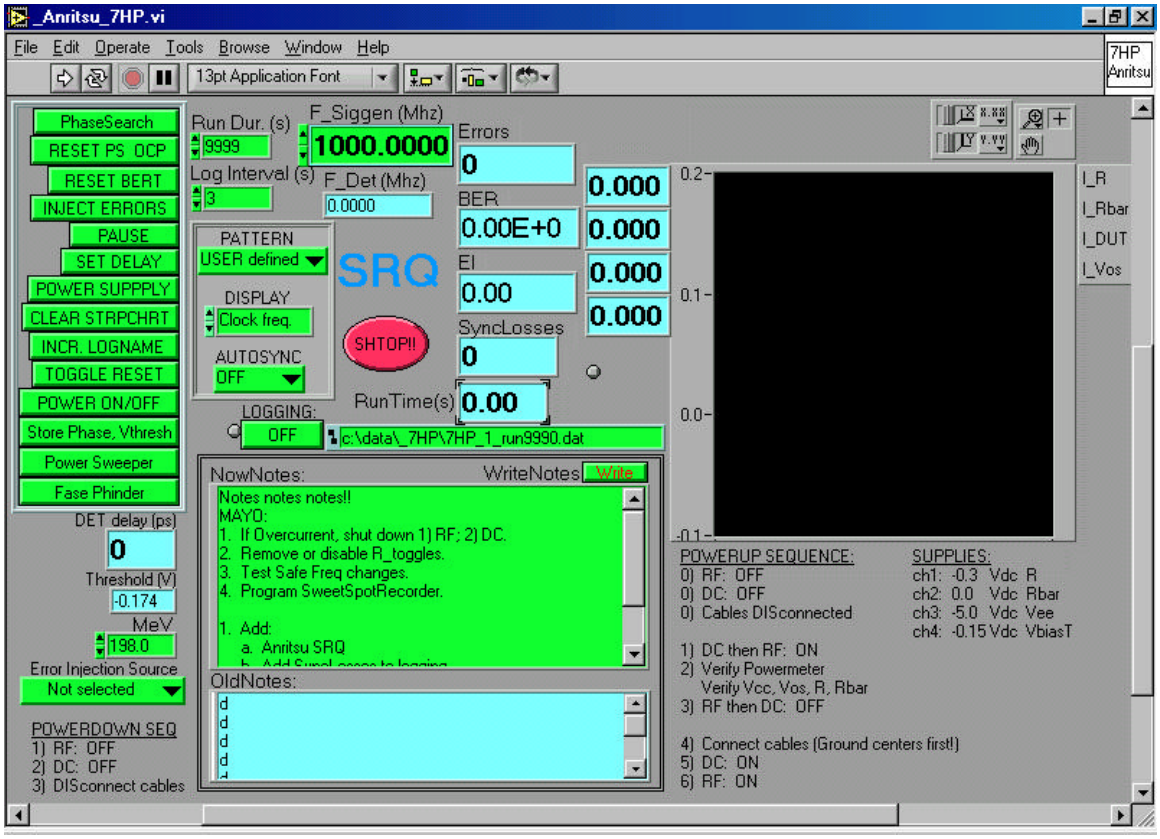

Figure 3. Front panel of the test application

One of two files describing the power vs frequency relationship of the DUT clock input supply, either the aforementioned BALUN.txt, or HYBRID.txt, is read for use in changing frequencies (the option to use the latter file was included before the decision was made to use only the balun).

After this initialization two software loops, or “threads”, run in parallel. The first loop performs only one function. It waits to be interrupted with information on the BERT loss-of-synchronization (LOS) state, via the service request (SRQ) interrupt functionality of the GPIB. It has a time-out of 500 ms. When no LOS has occurred in 500 ms the loop finishes and repeats. This provides a periodic opportunity to interrupt (and politely terminate, in the case of a user-directed command to stop the program) the wait. This loop normally uses very little processor time, a millisecond or so every 500 ms. When it uses more time than this, it is for processing the essential data of the DUT response to radiation.

The second, main, loop performs all other functions. The power supply state, including voltage, current and output On/Off status are periodically read. The frequency control is periodically compared with the BERT frequency indication and if they are different the frequency change protocol is initiated.

The frequency change protocol is so: If the new frequency is not in the BALUN.TXT lookup table, the user is warned and no change is made. Otherwise, the new power level is next set if it is lower than the current power level. Next, the new frequency is set. Next, if the new power level is higher than the old one, the power level is set. This way, the DUT never sees an inappropriately large clock input voltage. Next, the BERT delay and threshold voltage settings recorded as optimal in BALUN.TXT for the new frequency are sent to the BERT. For frequencies where the delay and threshold have not previously been determined and stored, the nominal, 0ps and –174 mV, are used.

Periodically, various non-time critical functions are performed by the second loop: User notes are added to the logfile. Various settings of the BERT are read and displayed. 17 front panel controls are monitored and some action is performed if indicated.

According to the state of the logging control on the front panel, various logging functions including opening a logfile, adding periodic (according to the period set by front panel control) data entries, closing the logfile, entering of post-run data (e.g. fluence).

When the second loop terminates due to user command, the first loop is terminated within 500 ms. If the power state of the DUT is ON the final action of the program is to perform a safe power-down, so that the DUT is not left powered without oversight and control by the program.

Some of the front panel controls worth note are:

-Phase Search: This commands the BERT to initiate its internal routine to search for the optimum data–to-clock phase relationship. The results are reported, either as a failure, or as new DetDelay(ps) and Threshold(V) values. For this search to occur there must be a bit error rate (BER) of less than approximately 0.005 (less than one bit error in every 200 bits), which means that synchronization must exist. If the BERT delay setting is not close enough to optimal synchronization might not be possible.

-Reset BERT: Normally the BERT measurement period is set to untimed, which counts and integrates errors without time limit. The Reset BERT control allows the restarting of the BERT measurement period and the zeroing of the program's event counters.

-Inject Errors: Individual bit errors cannot be injected because the DUT is not a transmission device, it is a generation device. However, a loss of sync and some concurrent number of bit errors can be generated by interrupting the DUT. This is done both by pulsing the DUT's reset signal and by jumping the (non phase-continuous) SigGen's frequency a small amount (and back). Normally the latter is chosen, tho either can be selected via the ErrorInjectionSource control in the lower left corner of the front panel.

-Pause: Prevents the program from communicating with the equipment (which prevents manual front panel operation). This is useful especially during setup and debugging.

-Set Delay: Sets the expected delay relationship between the BERT clock and data signals according to user choice.

-Power Supply: Allows interactive control of the power supply.

-Toggle Reset: Sets R and Rbar from the nominal –300&0 mV to 0&-300 mV, then back to nominal, in order to reset the DUT.

-Power On/Off: Allows the user to select automated (and thus, safely sequenced) power up or powerdown. If the program is ended with the DUT still powered up, the program will automatically execute a Powerdown.

-Store Phase, Vthresh: The current BERT settings are inserted into the appropriate cells in the BALUN.TXT file. In this way the file can be updated as new frequencies are added to the file or when system reconfiguration results in changes to these numbers.

-Power Sweeper: This utility resweeps the RF network and recalculates the correct SigGen output level for each frequency. It allows resweeping of existing frequencies, and the inclusion of new frequencies.

-Fase Phinder: This (uncompleted) utility will, for each frequency, automatically search for some phase for which synchronization exists. Then it will perform a BERT Phase Search to find the optimal delay and insert that in to BALUN.TXT.

-Logging, path: Turns logging on. Resets the BERT, opens the selected logfile, resets the RunTime(s) indicator, instigates logging to happen every LogInterval(s) seconds, etc.

-Pattern, Display, AutoSync: These set the expected BERT pattern, front panel display selection, and BER at which auto-resynchronization occurs.

-F_SigGen(MHz): Control for setting the SigGen frequency. When a change in this value is detected the safe frequency change protocol, as described earlier, is initiated.

-NowNotes, WriteNow: When WriteNow is pushed the current value of NowNotes is written to the logfile path, regardless of whether logging is on or not. In this way, annotations to the data files is encouraged and is easy.

V. PROTON TEST RESULTS

Figure 4 gives the measured synchronization cross-section versus the frequency for the 7HP PRN when exposed to 200 MeV protons. Two DUTs where tested, showing similar results. For DUT #1 two input powers where used, again with similar results.

No apparent bit errors were observed at the test site. A careful analysis of the data is required to verify that there are no bit errors.

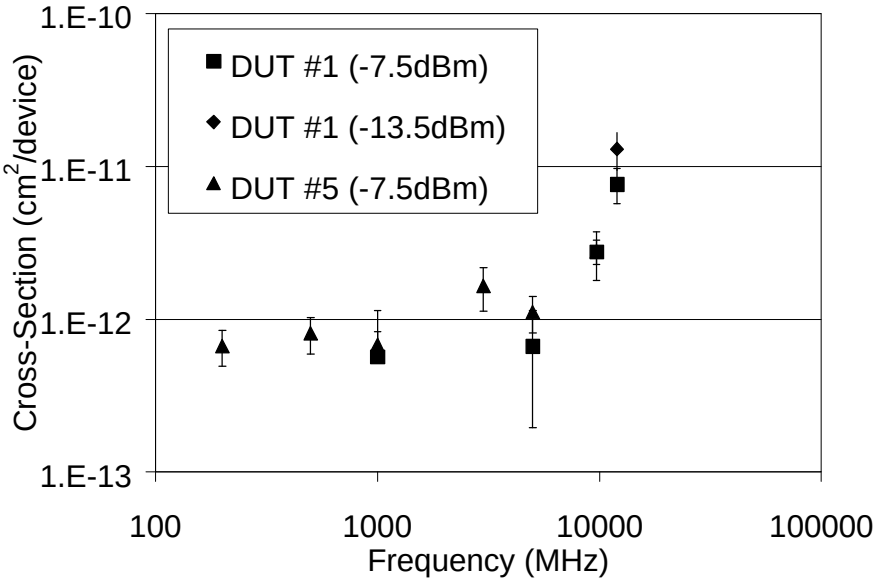

Figure 4. Synchronization error cross-section for the PRN when exposed to 200 MeV protons

VI. HEAVY-ION TEST RESULTS

Figure 5 gives the measured synchronization cross-section for two frequencies for the 7HP PRN when exposed to various ion LETs given in Table 1, effective LET was obtained by rotating the angle DUT relative to the incident beam. DUT #7 was tested. Figure 6 give frequency dependence for two ion LETs.

No apparent bit errors were observed at the test site. A careful analysis of the data is required to verify that there are no bit errors.

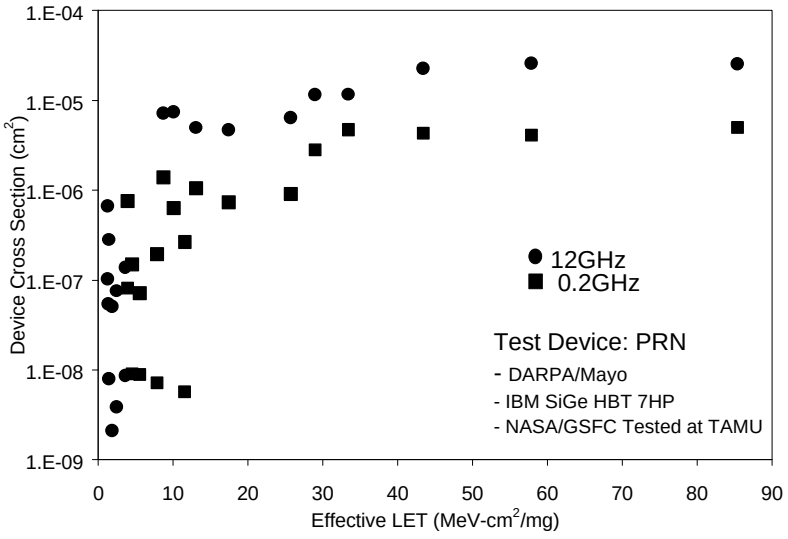

Figure 5. Heavy-ion results for synchronization errors on the PRN for various effective LETs

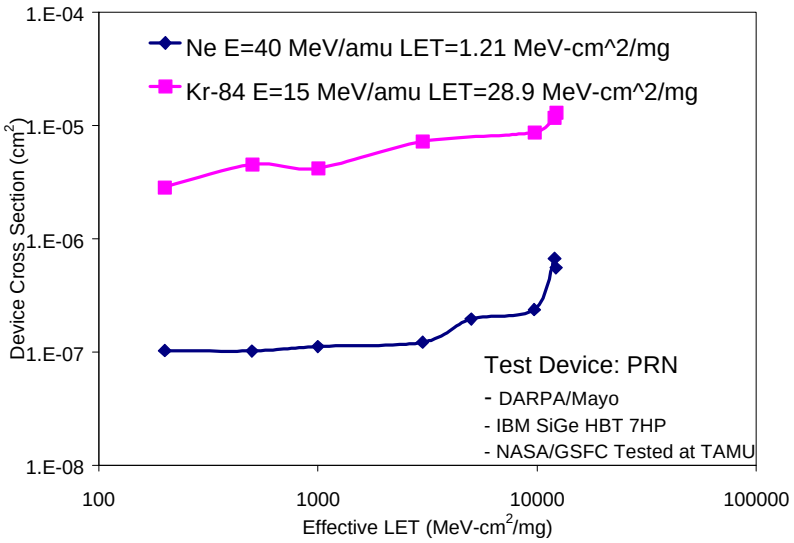

Figure 4. Synchronization error cross-section for the PRN when exposed to two heavy ion species