Silicon Carbide (SiC) and Silicon-on-Insulator (SOI) Electronics for Harsh Environmental Applications

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University of Illinois at Chicago

- **Silicon carbide (SiC) high-power high-temperature electronics**
  - NASA Glenn Research Center, Cleveland, OH
  - DARPA (Sterling Semiconductor)
  - Infineon and Power Electronics Reliability Group (PERG)
- **Silicon-on-insulator (SOI) RF and low-power electronics**
  - US Army (PolyFET RF Devices, Allied Signal, Honeywell)
  - Caltech/Jet Propulsion Laboratory (MIT Lincoln Labs, Honeywell)

Bulk versus SOI Technology

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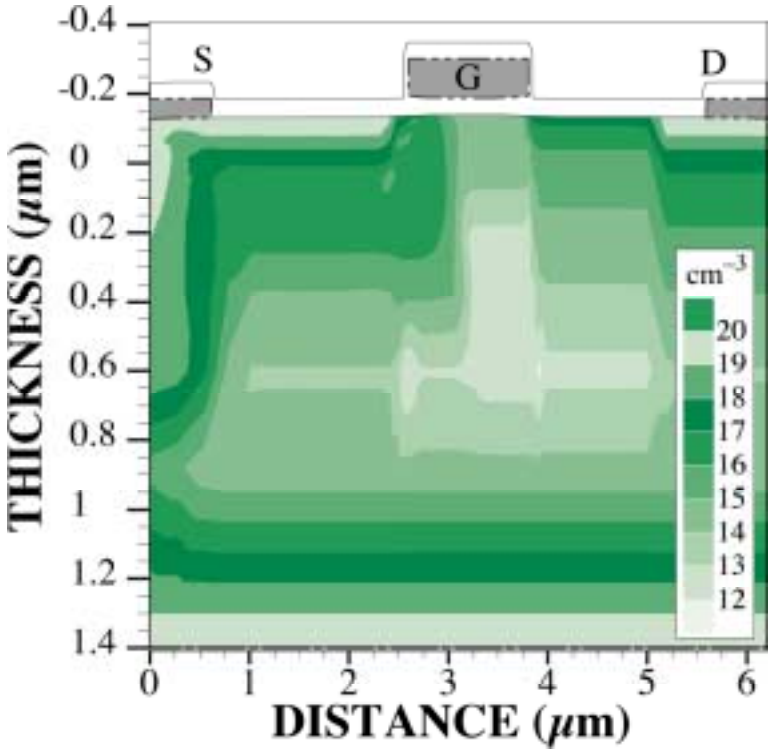

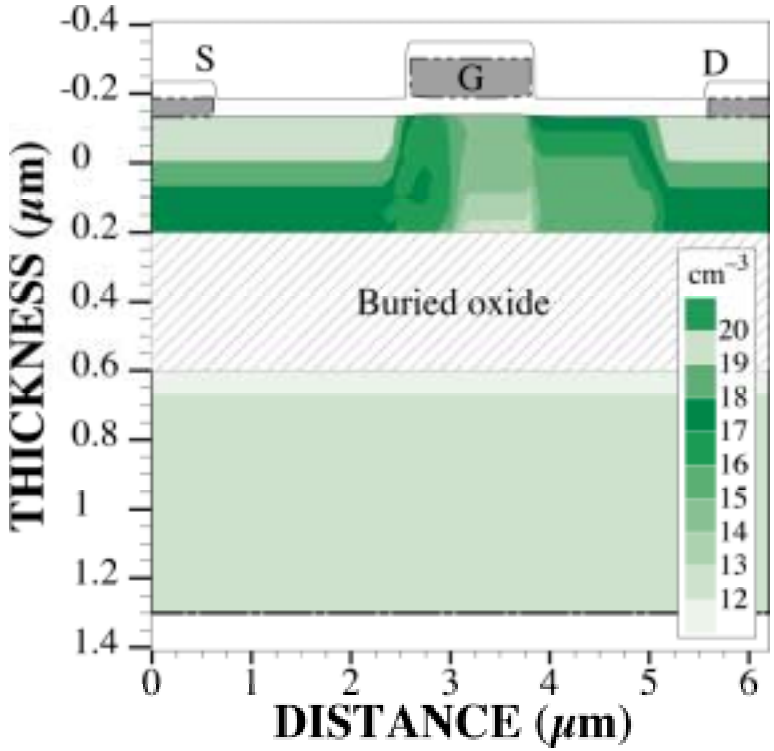

Bulk

- No “kink” in output current
- Low self-heating

SOI

- Suppressed substrate coupling
- Low capacitance
- Excellent passive components

Reliability Characteristics

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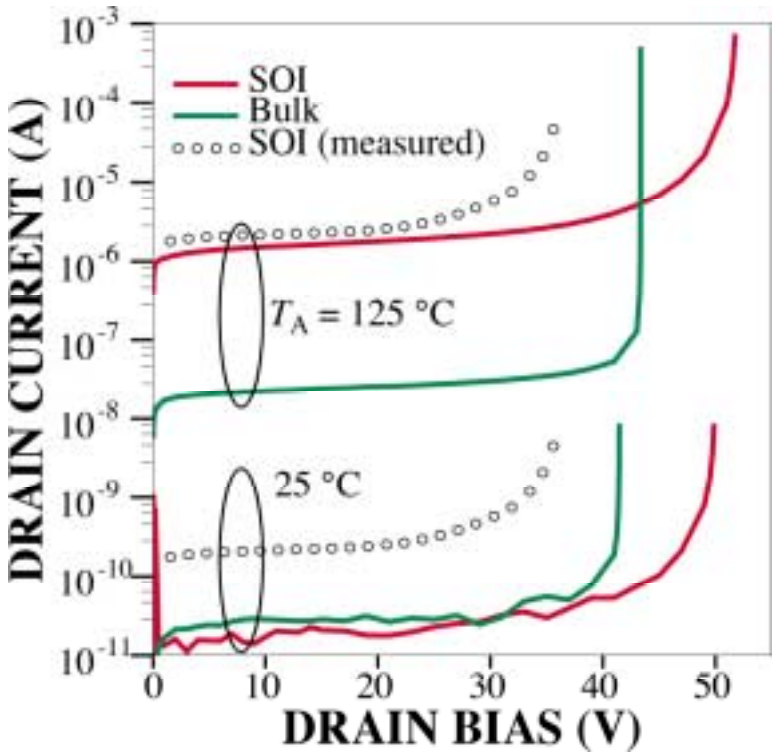
- Breakdown voltage
  - SOI has about 25% higher V_{BDD}
  - SOI breakdown is softer
- Leakage current
  - SOI typical has lower leakage
  - High leakage here due to unoptimized drain-body diode



DC Characteristics

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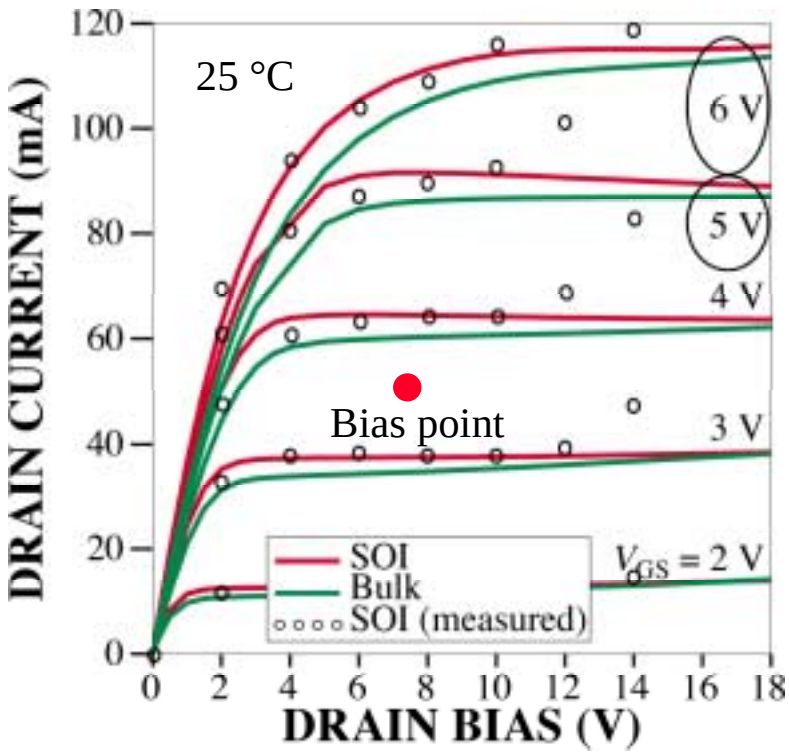

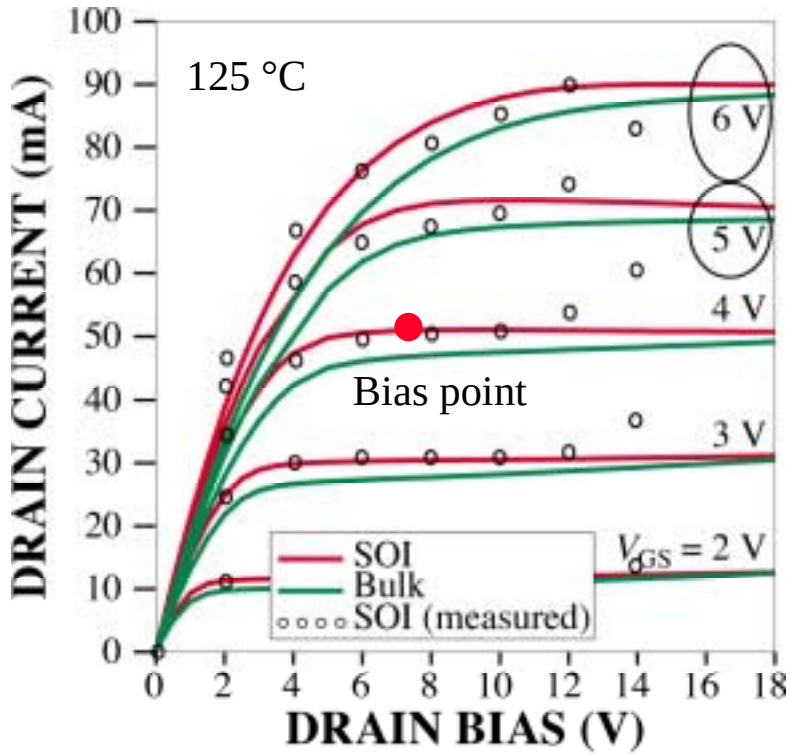

- SOI has higher saturation current
- SOI current degrades less at elevated temperatures
- SOI shows some negative differential resistance from self-heating

RF Characteristics

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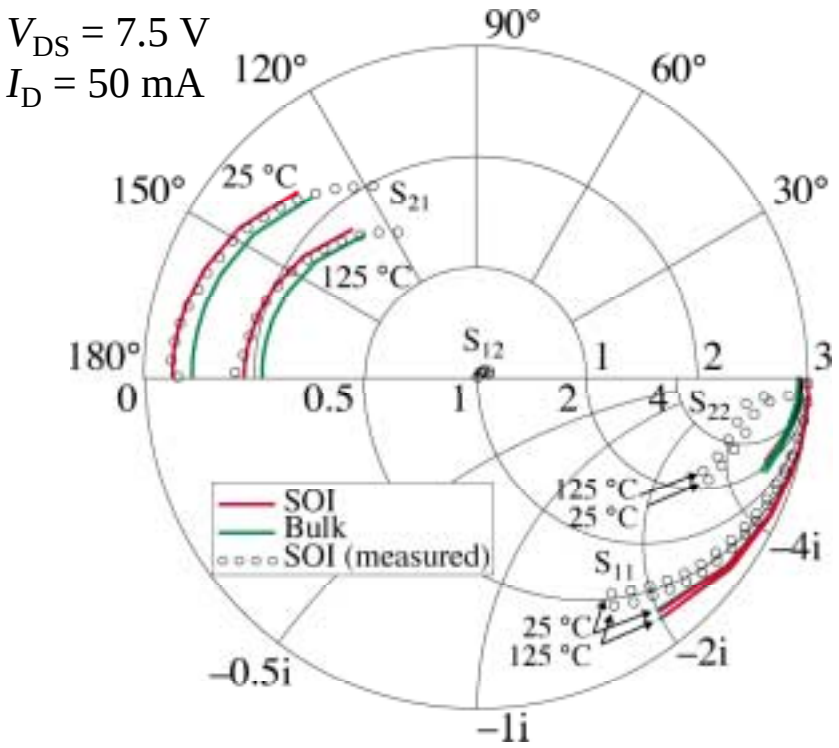

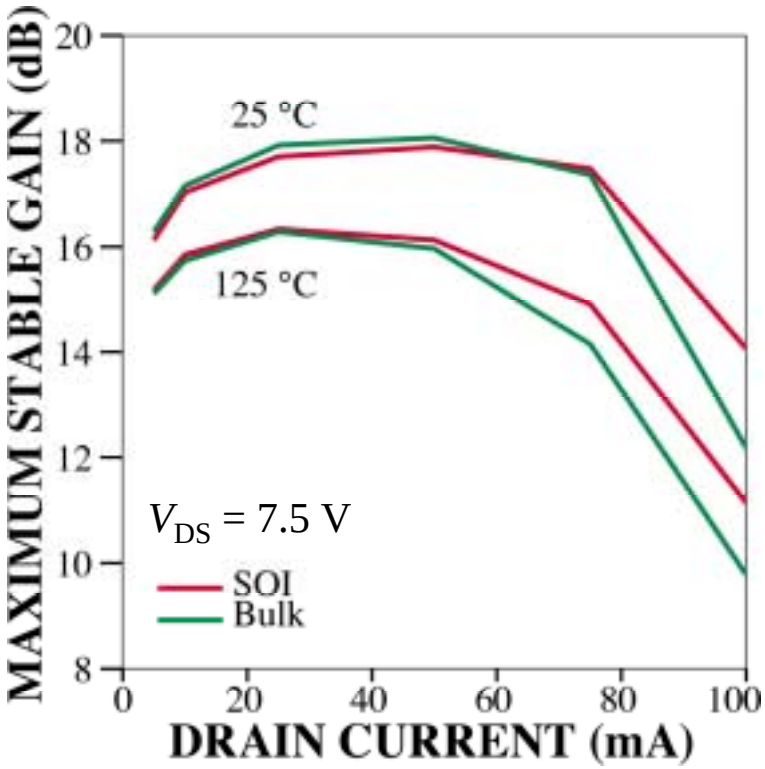

- SOI has higher forward gain (S_{21}) at room and elevated temperature
- SOI and bulk have very similar S_{11}: SOI can replace bulk without redesigning input matching networks
- SOI has better gain, especially when DC bias current is high (class A)

Self-Heating

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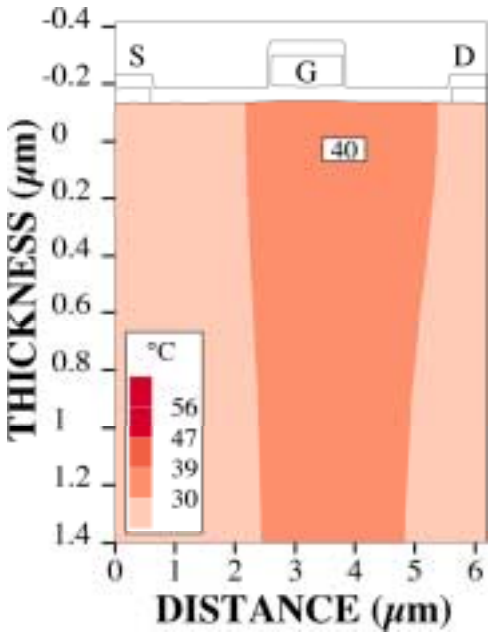
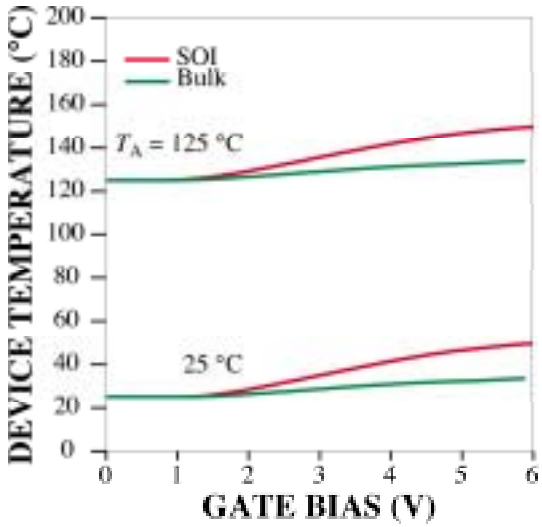
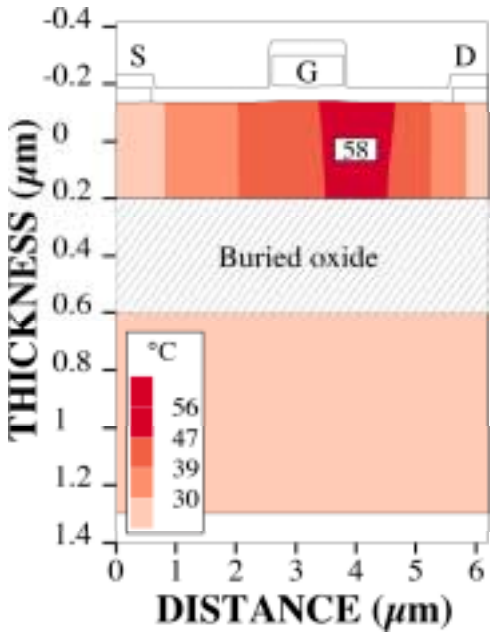


V_{DS} = 7.5 V, I_D = 50 mA





V_{DS} = 7.5 V, I_D = 50 mA

- SOI shows more pronounced self-heating at DC bias point
- Despite 20°C higher internal temperature, SOI outperforms bulk

Device Comparison

V_{DS} = 5 V, V_{GS} = 0 V

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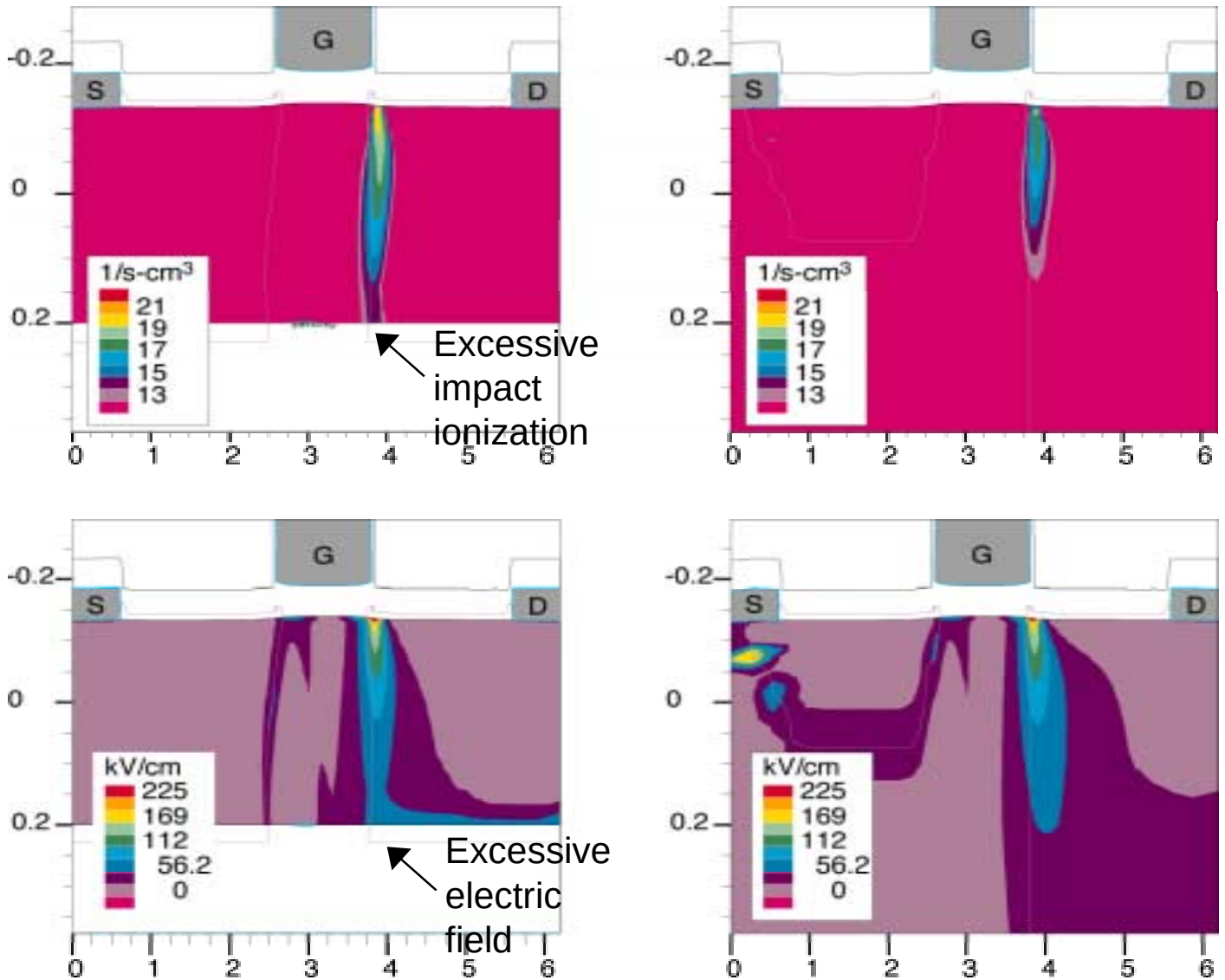

Frequency and Power Ratings

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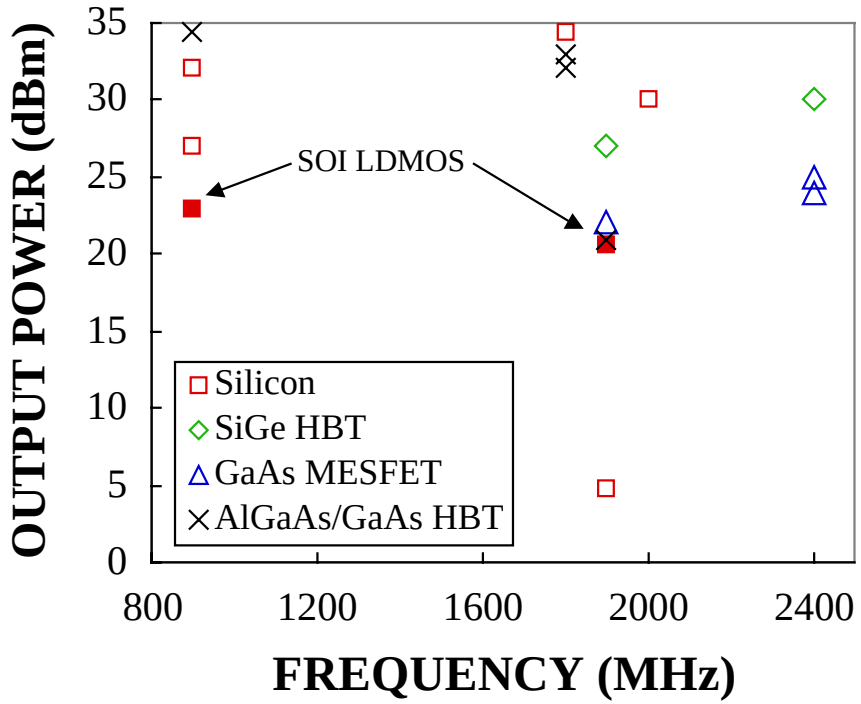
- Mid- to long-range transmission
  - 800 MHz to 2.4 GHz
  - mW to W
  - Wireless handsets, pagers, GPS
- Short-range transmission
  - 2.4 GHz
  - µW to mW
  - Bluetooth, wireless LAN



1G	AMPS	800 MHz, 900 MHz
2G/2.5G	cdmaOne	900 MHz
	GSM	900 MHz, 1.8 GHz, 1.9 GHz
	GSM EDGE, PCS	1.9 GHz
3G	UMTS, W-CDMA	2.1 GHz
Embedded	Bluetooth	2.4 GHz

SOI LDMOS Performance Trends

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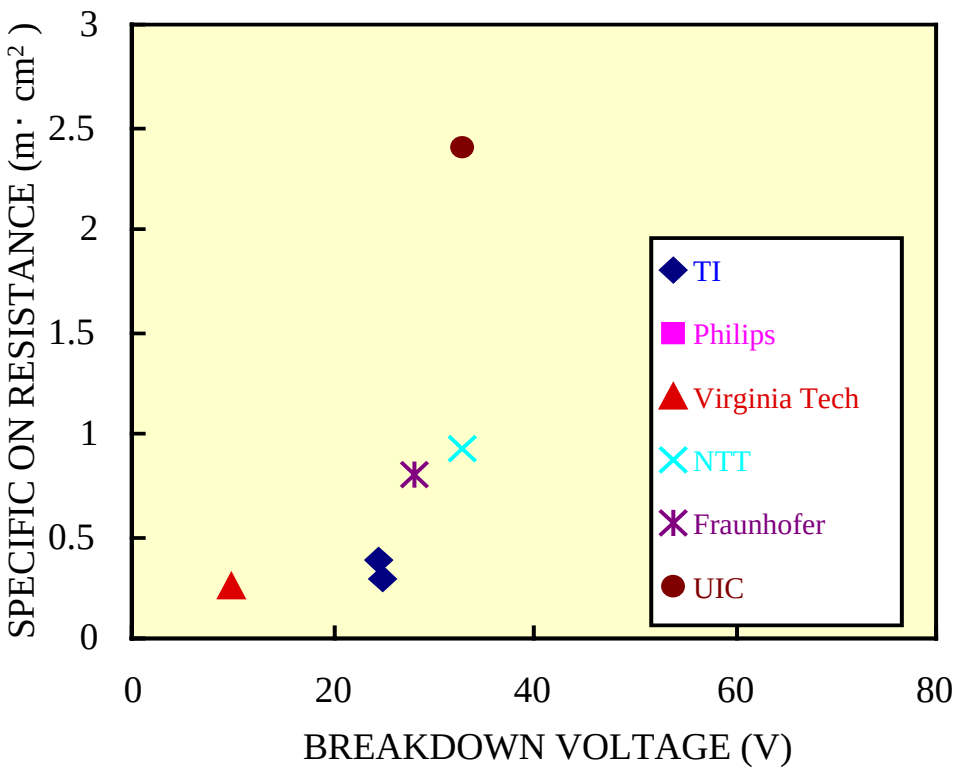
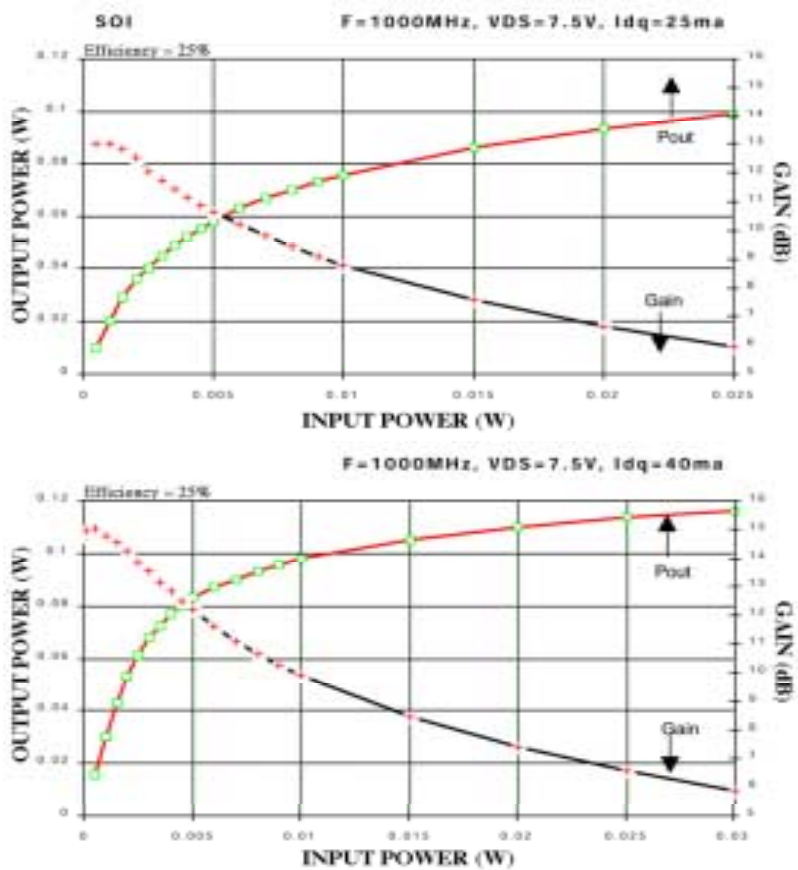
SPECIFIC RESISTANCE



RF DRAIN EFFICIENCY



More efforts towards power IC application than RF power amplifiers

K.Shenai, E. McShane, and S.K. Leong, "Lateral RF SOI Power MOSFETs with fT of 6.9GHz,"
IEEE Electron Device Lett., vol. 21, no. 10, Oct. 2000 pp. 500-502

Power Delivery Trends

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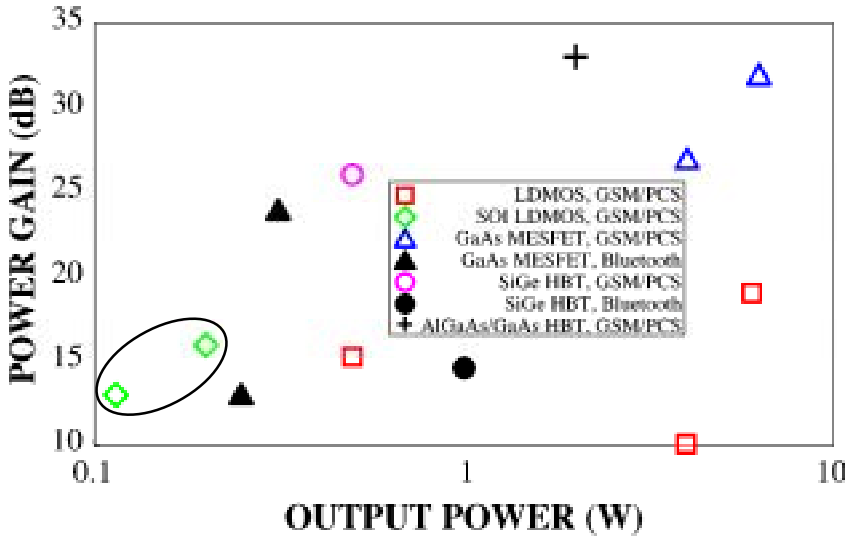
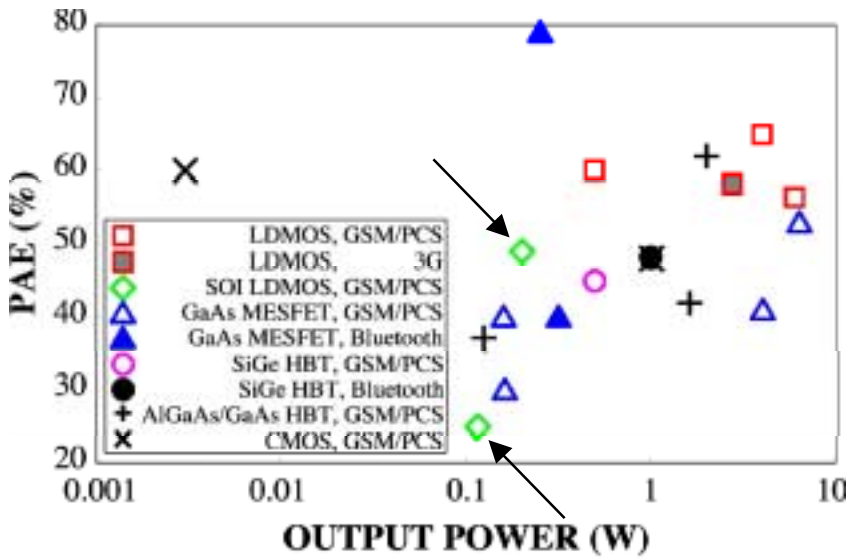
- Power gain
  - Silicon “power” devices limited to LDMOS and CMOS variants
  - Bulk and SOI show similar performance
  - SiGe competes well with GaAs MESFETs to 2.4 GHz



- PAE
  - Silicon “power” devices very competitive to 2.1 GHz
  - Ordinary CMOS is promising
  - SiGe is comparable to GaAs MESFETs



SOI Devices for Radiation Tolerance

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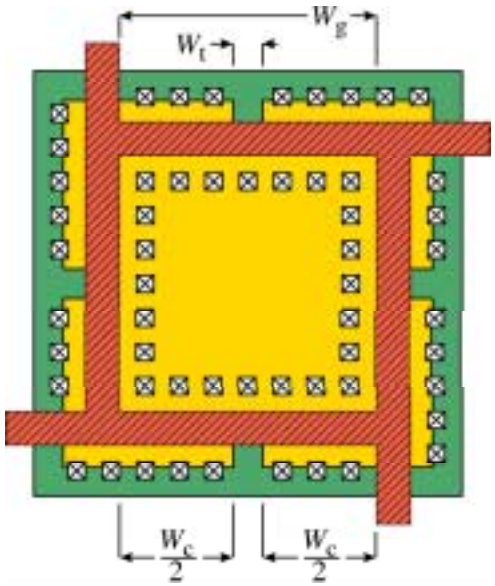
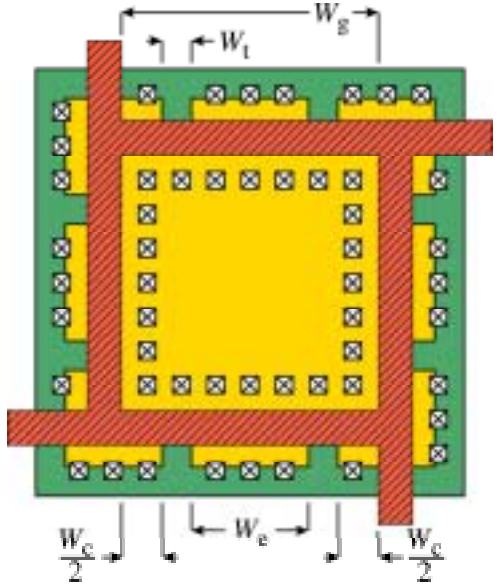
Device	Pattern	W_c (μm)	W_e (μm)	W_g (μm)	r	W_t/W_g (%)	$R_{b\,eff}$ (kž)
1	A	8.9	0	10.1	4	11.9	55
2	A	12.9	0	14.1	4	8.51	77
3	A	16.9	0	18.1	4	6.63	99
4	B	0.9	6.8	10.1	8	23.8	37
5	B	4.9	6.8	14.1	8	17.0	39
6	B	8.9	6.8	18.1	8	13.3	50
7	C	0.9	6.8	10.1	8	23.8	37
8	C	0.9	10.8	14.1	8	17.0	57
9	C	0.9	14.8	18.1	8	13.3	78

- Enclosed layout transistors
  - Gate is a continuous loop
  - No oxide edge shared by drain and source
  - Body resistance defined by ratio of gate segments

$$R_{b,\mathrm{eff}} = \frac{R_{sh}}{2}\left(x\frac{W_c + W_t}{L} + (1-x)\frac{W_e + W_t}{L}\right) \qquad x = \frac{W_c + W_t}{W_g}$$





Physics of Scaling and the Kink Effect

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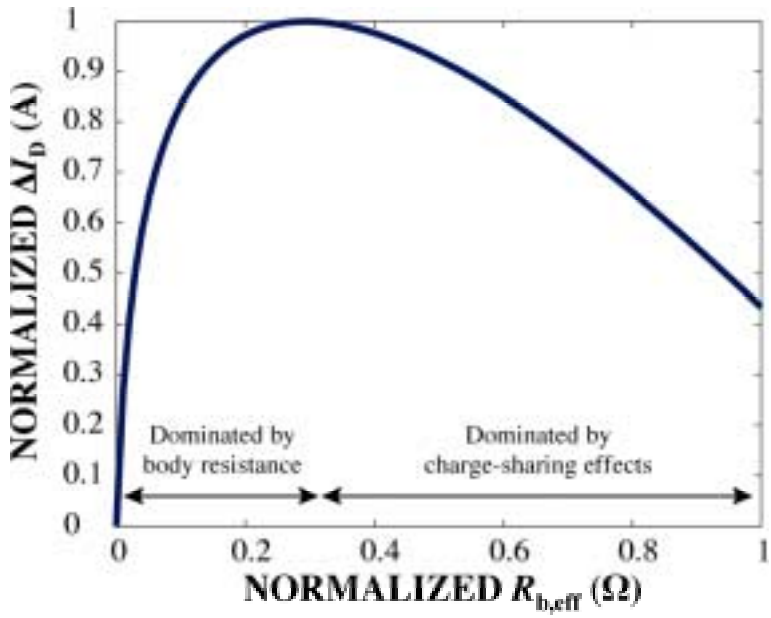
- Narrow devices
  - Kink is proportional to device width (or separation of body ties)
  - Charge-sharing effects are suppressed by body ties
- Wide devices
  - Kink is inversely proportional to device width (or separation of body ties)
  - Enhanced charge-sharing reduces C_d and hence ?I_D



$$\Delta I_D = \underbrace{\frac{C_d}{C_{ox}} g_m}_{\text{body transconductance}} \cdot \underbrace{\frac{kT}{q} \log\left(\frac{I_{sub}}{I_0} + 1\right)}_{\text{internal substrate bias}}$$

Reliability and Subthreshold Characteristics

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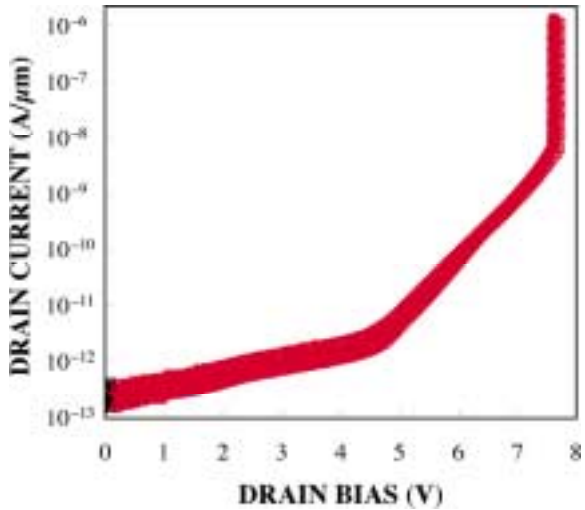
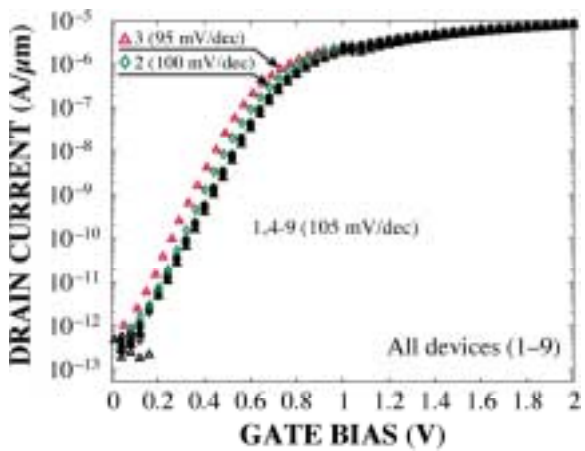
- Breakdown
  - Little sensitivity to body tie geometry
  - Device “corners” do not contribute to high electric field



- Leakage
  - Widest separation of body ties has most severe charge-sharing (lowest C_d)
  - Lower C_d causes a more ideal subthreshold slope

$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_d}{C_{ox}}\right)$$



Output Conductance Flatness

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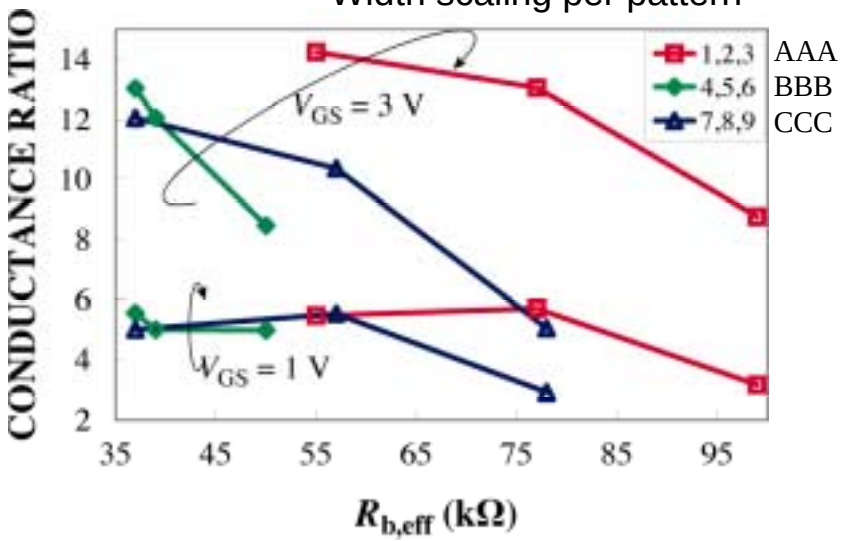
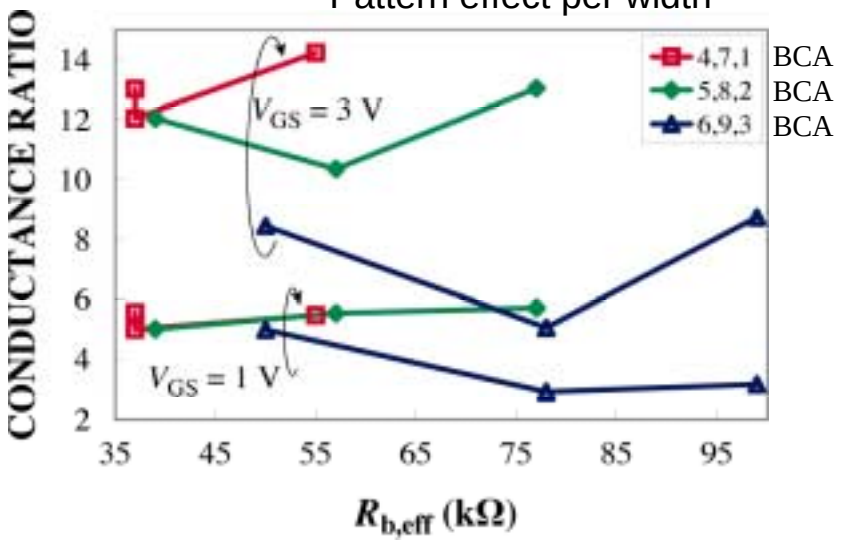
- Effect of device width
  - Kink is suppressed with increasing body resistance
  - Kink can be reduced by over 60%

Width scaling per pattern



- Effect of body tie pattern
  - Body tie pattern plays a role in suppressing kink
  - Kink always reduced most using pattern “C” (body ties close to device corners)

Pattern effect per width



Conclusions: SOI

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Present

- RF SOI has performance competitive with bulk—could be better than bulk with optimization
- Signal-level SOI is very sensitive to body tie position—bulk CMOS models are unsuitable

Future

- Reduce leakage currents
  - Extend lightly-doped drain to BOX interface
- Reduce specific on-resistance
  - Operate device at higher gate overdrive
  - Shrink drawn gate length closer to effective gate length
  - Optimize length of lightly-doped drain extension
- Increase forward gain
  - Increase BOX thickness to reduce further the output capacitance