S-311-24

REVISIONS				
SYMBOL	PREP BY	DESCRIPTION	DATE	APPROVAL

PREPARED BY	Maurice J. Robertson MJR	DATE 10-17-73	TITLE Screening Procedure for a Medium Power, PNP, Silicon Transistor (2N4236)
APPROVED	Albert Lunchick A.L.	10/30/73	
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			# SP 73-15070

Branch – Parts
Division – Quality Assurance
Project – IUE

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

520-23 (3/64)

GSFC APPLICATIONS SECTION

SCREENING PROCEDURE

1. SCOPE

This procedure covers the screening requirements for a Medium Power, PNP, Silicon Transistor (2N4236).

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein.

MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-750	Test Methods for Semiconductor Devices

3. TEST PROCEDURES AND REQUIREMENTS

3.1 External Visual Inspection

Examine all transistors with a microscope at a minimum of 10X magnification:

(a) Verify that all markings are in accordance with the manufacturer's data sheets.

(b) Inspect all transistors for defects in workmanship.

(c) Verify that all materials, design and construction are in accordance with the manufacturer's data sheets. Determine if the leads are solder or gold plated.

3.2 Initial Measurements

Make all the electrical parameter measurements listed in Table I. All measurements made at T_A = 298 K ±3 K unless otherwise specified. Devices shall be serialized at this time.

3.3 High Temperature Storage

473 K for 48 hours. (If the leads are tinned or solder plated, reduce the test temperature to 398 K.)

3.4 Thermal Shock (Temperature Cycling)

Method 1051 of MIL-STD-750 (Method 107 of MIL-STD-202), Test Condition C, except 10 cycles total, 15 minute rest at each temperature extreme. (If the leads are tinned or solder plated, reduce the test temperature to 398 K.)

3.5 Acceleration

MIL-STD-750, Method 2006, at 20,000 G, in Y_1 orientation only, one time only. The one minute hold-time requirement shall not apply.

3.6 Hermetic Seal (Fine Leak) Test

Test for a maximum leak rate of 10^{-8} atm cc/sec per Test Condition G or H of Method 1071 of MIL-STD-750.

3.7 Hermetic Seal (Gross Leak) Test

Test Condition C of Method 1071 of MIL-STD-750.

3.8 Reverse Bias Burn-In

Time	Temperature	Collector to Base Voltage	Emitter Current
(T)	(T_A)	(V_{CB})	(I_E)
48 hours	448 K for gold plated leads; 398 K for tinned leads	-60 Vdc	0

After the 48 hour burn-in, the collector to base voltage (V_{CB}) shall be maintained on the devices until the ambient temperature (T_A) is 303 K ±5 K.

3.9 Postburn-In Electrical Parameter Measurements

The postburn-in electrical parameter measurements shall be made within 24 hours of the conclusion of burn-in. The test measurements are listed in Table II and shall be performed at an ambient temperature (T_A) of 298 K ±5 K. These test measurements will be used as preburn-in electrical parameter measurements for the power burn-in and used in the calculation of the delta (Δ) changes during and following the power burn-in.

3.10 Power Burn-In

Time	Temperature	Collector to Base Voltage	Total Power Dissipation
(T)	(T_A)	(V_{CB})	(P_T)
168 hours Note 1 Note 2	298 K ±3 K	-10 Vdc	1.0 W

Notes: 1. Before burn-in of the lot is started, three transistors from the lot shall be subjected to a 24-hour burn-in followed by the postburn-in measurements. If any part fails the parameter limits or delta criteria, the burn-in test set-up shall be reevaluated.

2. After 96 hours of burn-in remove devices from test and subject them to the postburn-in tests. Then continue the burn-in for the remaining 72 hours.

3.11 Postburn-In Electrical Parameter Measurements

Make all the electrical parameter measurements listed in Table II. All measurements made at T_A = 298 K ±3 K unless otherwise specified.

3.12 Parameter Change Criteria

All devices exhibiting parameter changes between the preburn-in electrical parameter measurements (paragraph 3.9) and the postburn-in electrical parameters which are not within the ranges indicated below, shall be rejected.

ΔI_{CBO} = 100% or 25 nanoamperes, whichever is greater

Δh_{FE} = ±15%

3.13 Final Measurements

Make all the electrical parameter measurements listed in Table I. All measurements made at T_A = 298 K ±3 K unless otherwise specified.

4. LOT ACCEPTANCE

When more than 10 percent of the lot fails screening, the entire lot shall be subject to rejection. The Applications Section shall be notified when any lot is subject to rejection.

5. DATA

A copy of the data generated during this test shall be sent to the Applications Section.

6. MARKING

Each device that is screened to the requirements of this specification shall receive a serial number that remains with the device when it is returned to the requester along with the test data.

TABLE I. INITIAL AND FINAL ELECTRICAL MEASUREMENTS

Test	Symbol	MIL-STD-750		Limits		Unit
		Method	Details	Min.	Max.	
Collector-emitter sustaining voltage	$BV_{CEO(sus)}$	3011	I_C = 100 mAdc I_B = 0 Bias Condition D See Note 1	80	---	Vdc
Collector to emitter cutoff current	I_{CEO}	3041	V_{CE} = 60 Vdc I_B = 0 Bias Condition D	---	1.0	mAdc
Collector to emitter cutoff current	I_{CEX}	3041	V_{CE} = 80 Vdc $V_{BE(off)}$ = 1.5 Vdc Bias Condition A	---	0.1	mAdc
Emitter to base cutoff current	I_{EBO}	3061	V_{EB} = 7.0 Vdc I_C = 0 Bias Condition D	---	0.5	mAdc
Forward current transfer ratio	h_{FE}	3076	V_{CE} = 1.0 Vdc I_C = 100 mAdc See Note 1	40	---	
Forward current transfer ratio	h_{FE}	3076	V_{CE} = 1.0 Vdc I_C = 1.0 Adc See Note 1	10	---	
Small signal forward current transfer ratio	h_{fe}	3306	V_{CE} = 10 Vdc I_C = 50 mAdc f = 1.0 kHz	2 5	---	

TABLE I. INITIAL AND FINAL ELECTRICAL MEASUREMENTS (Continued)

Test	Symbol	MIL-STD-750		Limits		Unit
		Method	Details	Min.	Max.	
Base-emitter saturation voltage	$V_{BE(sat)}$	3066	I_C = 1.0 Adc I_B = 100 mAdc See Note 1	---	1.5	Vdc
Collector emitter saturation voltage	$V_{CE(sat)}$	3071	I_C = 1.0 Adc I_B = 125 mAdc See Note 1	---	0.6	Vdc
Collector to base cutoff current	I_{CBO}	3036	V_{CB} = 80 Vdc I_E = 0 Bias Condition D	---	100	nAdc
Base-emitter on voltage	$V_{BE(on)}$	3066	I_C = 250 mAdc V_{CE} = 1.0 Vdc	---	1.0	Vdc
Output capacitance	C_{ob}	3236	V_{CB} = 10 Vdc I_E = 0 f = 100 kHz	---	100	pF
Forward current transfer ratio	h_{FE}	3076	V_{CE} = 1.0 Vdc I_C = 250 mAdc See Note 1	30	150	

Note 1. Pulse Test: PW ≤ 300 μs, Duty Cycle ≤ 2%.

TABLE II. PREBURN-IN AND POSTBURN-IN ELECTRICAL PARAMETER MEASUREMENTS

Test	Symbol	MIL-STD-750		Limits		Unit
		Method	Details	Min.	Max.	
Collector to base cutoff current	I_{CBO}	3036	V_{CB} = 80 Vdc I_E = 0 Bias Condition D	---	100	nAdc
Forward current transfer ratio	h_{FE}	3076	V_{CE} = 10 Vdc I_C = 250 mAdc See Note 1	30	150	

Note 1. Pulse Test: PW ≤ 300 μs, Duty Cycle ≤ 2%.