Military and Aerospace FPGA and Applications (MAFA) Meeting

Preliminary Schedule for Tuesday, November 27, 2007

Last Updated: 11/16/07

7:30	Registration and Continental Breakfast		
8:15	General Introduction	Ken LaBel and Mike Sampson	Ken LaBel and Mike Sampson, NASA/GSFC
8:30	Radiation Hardened FPGA Technology for Space Applications	Dinu Patel	Leonard Rockett, Dinu Patel, Steven Danziger, BAE Systems; John McCollum, Brian Cronquist, Actel Corporation
9:00	Advanced ASICs For Obsolete FPGA Replacement	David Wick	David Wick and Thomas Romanko, Honeywell
9:30	Actel Space Product Roadmap	Ken O'Neill	Ken O'Neill, Actel Corporation
10:00	Current Status of the SIRF Program	Joseph J Fabula	Joseph Fabula, Xilinx
10:30	Break		
11:00	ATMEL ATF280E Rad-Hard Reprogrammable FPGA	Nicolas Renaud	Nicolas Renaud, ATMEL
11:30	New Reprogrammable and Non-Volatile Radiation Tolerant FPGA RTA3P	Sana Rezgui	Sana Rezgui, J. J. Wang, Brian Cronquist, John McCollum, Actel Corporation
12:00	Lunch with Invited Speaker		
1:00	Invited Speaker: “Advanced Techniques for Microelectronic Reliability Investigation”	Martin Leung	M. S. Leung, J. Chaney, G. Eng, B. Foran, N. Ives, M. Mason, S. C. Moss, N. Presser, G. Stupian, T. Yeoh, and M. Zurbuchen , The Aerospace Corporation
1:30	Reconfigurable, High Density, Gigahertz Speed Low Power Radiation Hardened FPGA Technology	Dinu Patel	Rajit Manohar, Clinton W. Kelly, IV, John Lofton Holt, Chris Liu, Achronix Semiconductor Corporation; Leonard Rockett, Dinu Patel, Steven Danziger , S.Ramaswamy, BAE Systems; Ken LaBel, NASA/GSFC
2:00	Innovations in High Rel Power Management	Randy Roberts	Randy Roberts, Intersil Corporation
2:30	Update on the Universal FPGA Support Device for Spaceborne Applications	Joseph Marshall	Joseph Marshall, BAE Systems
3:00	Break		
3:30	Radiation Hardened Field Programmable Object Array (FPOA) for Space Processing	David Lupia and Sean Riley	David Lupia, Honeywell; Sean Riley, MathStar
4:00	The Gaisler Research Roadmap for FPGA IP-Cores	Sandi Habinc	Sandi Habinc and Jiri Gaisler, Gaisler Research AB
4:30	Prototyping RTAX using Flash Devices	Jerry Kaczynski (Presented by Olga Melnikova)	Jerry Kaczynski, Aldec, Inc.
5:00	Wrap-up		

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7:30	Registration and Continental Breakfast		
8:15	General Introduction	Ken LaBel and Mike Sampson	Ken LaBel and Mike Sampson, NASA/GSFC
8:30	Overviews on FPGA activities in ESA and European Missions	David Merodio Codinachs	David Merodio Codinachs, ESA
9:00	Overview of Radiation Hardened Electronics for Space Environments	Andrew S. Keys	Andrew S. Keys, NASA/MSFC
9:30	Improving FPGA Reliability in Harsh Environments Using Triple-Modular Redundancy with More Frequent Voting	Michael Wirthlin	Brian Pratt, Michael Wirthlin, Bringham Young University; Paul Graham, Keith Morgan, Los Alamos National Laboratory; Severn Shelley, Bringham Young University and Los Alamos National Laboratory
10:00	Correcting Single-Event Upsets Using Self-Hosting Partial Dynamic Reconfiguration	Jonathan Heiner (presented by Michael Wirthlin)	Jonathan Heiner, Nathan Collins, Michael Wirthlin, Brigham Young University
10:30	Break		
11:00	Optimized Configuration Management for SEU Mitigation in Xilinx Virtex-4 FPGA and Self-Scrubbing	Chen Wei Tseng (presented by Greg Allen)	Chen Wei Tseng, Carl Carmichael, and Gary Swift, Xilinx, Inc.
11:30	Comparing the Robustness of Upset Mitigation via RHBD and TMR System Error Rates for SRAM-based Re-configurable FPGAs	Gary Swift	Gary Swift, Xilinx, Inc.; Larry Edmonds, JPL/Caltech
12:00	Lunch with Invited Speaker		
1:00	Invited Sponsor Talk		
1:30	The Response of Deep Sub-Micron FGPAs to High Energy Atmospheric Neutrons	Joe Fabula	Joseph Fabula, Austin Lesea, Xilinx, Inc.
2:00	Upset Measurements on a Mil/Aero Virtex-4 FPGAs Incorporating 90 nm Features and a Thin Epitaxial Layer	Greg Allen	Gregory Allen, JPL; Gary Swift, Carl Carmichael, Chen Wei Tseng and Greg Miller, Xilinx, Inc.
2:30	New Reliability Vehicle from Aeroflex Improves FPGA ViaLink™ Perceptivity	Ronald Lake	Ronald Lake, Aeroflex Colorado Springs
3:00	Break		
3:30	Monitoring Temperature in SRAM-based FPGAs Using a Ring-oscillator Design	Douglas J Sheldon, Ramin Roosta, Michael J Sadigursky & Arjang Farrokhy	Douglas J Sheldon, Ramin Roosta, Michael J Sadigursky, Arjang Farrokhy, JPL
4:00	Reliability of FPGA Assembled with Tim-lead and Pb-free Solders Tested based on IPC 9701A Specification	Reza Ghaffarian	Reza Ghaffarian, JPL
4:30	Actel RTAX4000S Generic Burn-In Test Feature	Solomon Wolday	Solomon Wolday, Don Kinell, and Antony Wilson, Actel Corporation
5:00	Wrap-up		

Military and Aerospace FPGA and Applications (MAFA) Meeting

Preliminary Schedule for Thursday, November 29, 2007

Last Updated: 11/16/07

7:30	Registration and Continental Breakfast		
8:15	General Introduction	Ken LaBel and Mike Sampson	Ken LaBel and Mike Sampson, NASA/GSFC
8:30	FPGA Insertion Guidelines	Douglas J Sheldon	Douglas J Sheldon, JPL
9:00	Microelectronics Research Development Corporation (Micro-RDC) Capabilities	Keith Avery	Keith Avery, Micro-RDC
9:30	The LEON3 processor and SpaceWire Codec and their Application	Sandi Habinc	Sandi Habinc and Jiri Gaisler, Gaisler Research AB
10:00	Sandia Xilinx Virtex FPGA SEU and Passive Devices Experiment on the International Space Station	Ethan Blansett	Ethan Blansett, Sandia National Laboratories
10:30	Break		
11:00	A Comparative Study of Field Programmable Gate Array Error Cross Sections: Putting Data into Perspective	Melanie Berg	Melanie Berg, MEI Technology Inc., NASA/GSFC
11:30	Using the Xilinx FPGA as a Test “System”	Paul Eaton	Paul Eaton, Microelectronics Research Development Corporation
12:00	Lunch		
1:00	RadSafe™ Technology and JPEG200 image compression ASSP	Ran Ginosar	Ran Ginosar, Ramon Chips Ltd.
1:30	Radiation and Reliability Issues for SOI in Next Generation FPGAs	Hugh Barnaby	Hugh Barnaby, Bert Vermeire, Arizona State University; Philippe Adell, JPL
2:00	Lessons Learned with Performance Prediction and Design Patterns on Molecular Dynamics	Brian Holland	Brian Holland, CHREC University of Florida
2:30	Standardized test system for optical link in radiation environment based on FPGA	Jingbo Ye	Jingbo Ye, Southern Methodist University
3:00	Intermittency Detection and Mitigation in FPGAs	James P. Hofmeister	James P. Hofmeiser, Ridgetop Group, Inc.
3:30	Break		
4:00	Flexible Fault Tolerance Using the ARTEMIS Reconfigurable Payload Processor	Ian Troxel	Ian A. Troxel, Matthew Fehringer, Michael T. Chenoweth, SEAKR Engineering
4:30	Survey results and open discussion		
5:00	Wrap-up		