Radiation Hardened FPGA Technology for Space Applications

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RHAX250-S effort supported by the Defense Threat Reduction Agency

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RHFPGA Programs at BAE SYSTEMS

- RH FPGA Roadmap
- RH FPGA Technologies
  - ONO
  - M2M
- RH FPGA Program Status Review
  - Restart RH1020/RH1280 FPGA Program
  - RHAX FPGA Demonstration and Qualification Program
- Summary and Outlook

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Radiation Hardened FPGA Roadmap

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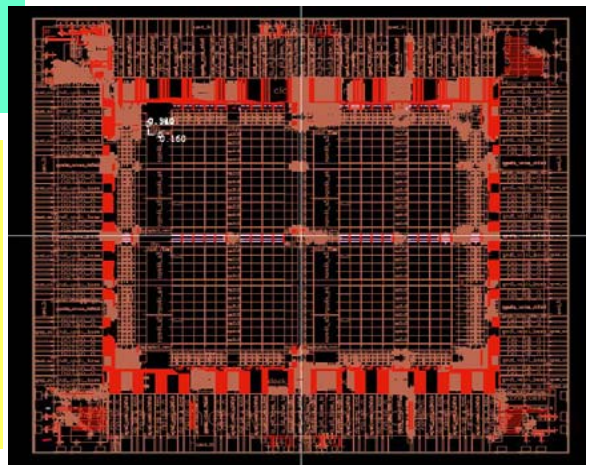
Rad Hard FPGA Product

Past

- Heritage: Actel ONO RH1280 and RH1020
  - Anti-fuse technology, non-volatile
  - 0.8µm RH CMOS, 5V Supply
  - In production since 1996, over 25,000 shipped

Present

- M2M Anti-fuse Technology:
  - 250K-gate (RHAX250-S)
  - RH15 CMOS, 1.5V Core / 3.3V I/O
  - Flight Orders in 2008



Future

- ≥3M-gate, re-programmable, non-volatile
- Radiation Hardened, high speed
- RH15 CMOS, 1.5V Core / 3.3V I/O
- Projected qualification starts in 2009

BAE Supporting RHFPGA Needs for RHOC requirements

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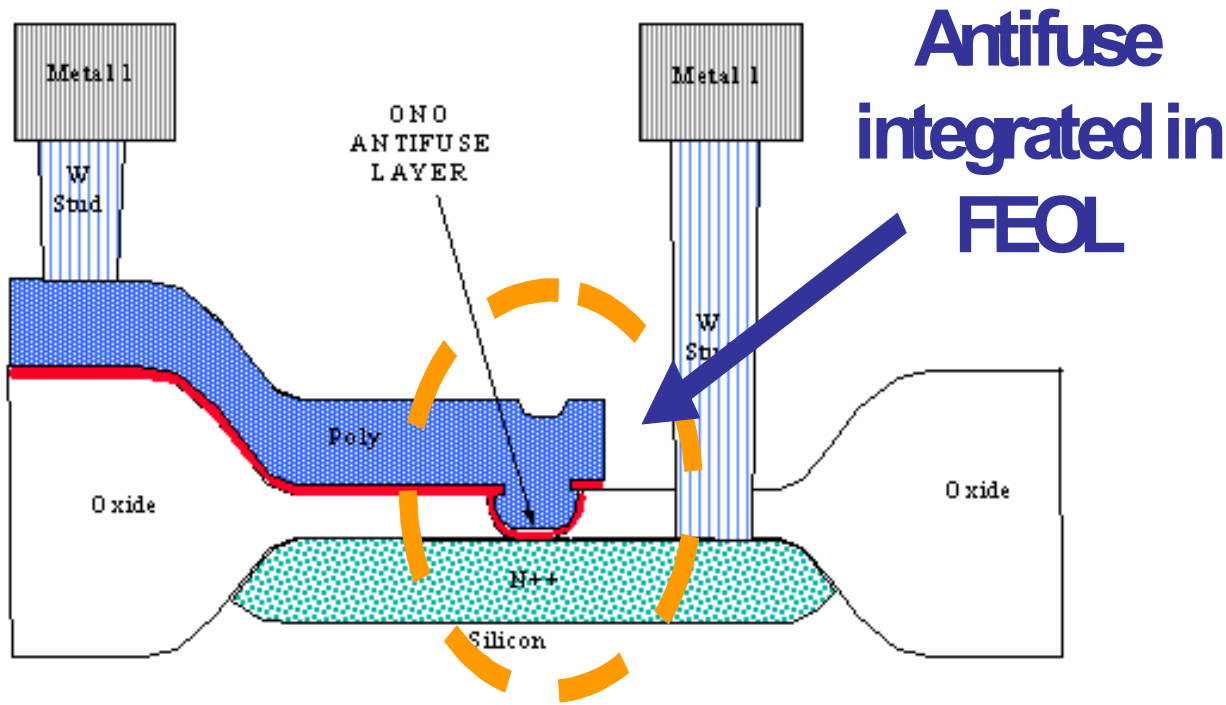
ONO Antifuse Based FPGA's



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ONO RHFPGA Program Plan

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- ONO technology originally installed and qualified to support RH1020 and RH1280 FPGA's and a 256K PROM [1994-96]
- Flight qualified production (with build-out inventory) [1996-2002]
- Production shutdown during foundry modernization [2002-2005]
  - ➢ Process line re-tooled to support 250 and 150 nm technology nodes on 150mm wafers
- ONO technology now reinstalled in modernized foundry to restart FPGA & PROM product to supply continued demand [2007-]
  - ➢ Used same design data ⇒ same form, fit, and function as product built previously

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Rad Hard FPGA RH1280B Technology Features

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Features

- Guaranteed Total Dose Radiation Capability
- Low Single Event Upset Susceptibility
- High Dose Rate Survivability
- Latch-Up Immunity Guaranteed
- QML Qualified Devices
- Commercial Devices Available for Prototyping and Pre-Production Requirements
- Gate Capacities of 2,000 and 8,000 Gate Array Gates
- More Design Flexibility than Custom ASICs
- Significantly Greater Densities than Discrete Logic Devices
- Replaces up to 200 TTL Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to Two High-Speed, Low-Skew Clock Networks
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Non-Volatile, User Programmable Devices
- Fabricated in 0.8 µ Epitaxial Bulk CMOS Process
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer

Product Family Profile

Device	RH1020	RH1280
Capacity		
System Gates	3,000	12,000
Gate Array Equivalent Gates	2,000	8,000
PLD Equivalent Gates	6,000	20,000
TTL Equivalent Packages	50	200
20-Pin PAL Equivalent Packages	20	80
Logic Modules	547	1,232
S-Modules	0	624
C-Modules	547	608
Flip-Flops (Maximum)	273	998
Routing Resources		
Horizontal Tracks/Channel	22	35
Vertical Tracks/Channel	13	15
PLICE Antifuse Elements	186,000	750,000
User I/Os (Maximum)	69	140
Packages (by Pin Count)		
Ceramic Quad Flat Pack (CQFP)	84	172

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Rad Hard FPGA RH1280B Technology Features

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Radiation Specifications

Table 1-2 • **Radiation Specifications[1, 2]**

Symbol	Characteristics	Conditions	Min.	Max.	Units
RTD	Total Dose			300 k	Rad (Si)
SEL	Single Event Latch-Up	$-55°C \le T_{case} \le 125°C$		0	Fails/Device-Day
SEU1[3]	Single Event Upset for S-modules	$-55°C \le T_{case} \le 125°C$		1E-6	Upsets/Bit-Day
SEU2[3]	Single Event Upset for C-modules	$-55°C \le T_{case} \le 125°C$		1E-7	Upsets/Bit-Day
SEU3[3]	Single Event Fuse Rupture	$-55°C \le T_{case} \le 125°C$		<1	FIT (Fails/Device/1E9 Hrs)
RNF	Neutron Fluence		>1 E+12		N/cm^2

Notes:

1. *Measured at room temperature unless otherwise stated.*
2. *Device electrical characteristics are guaranteed for post-irradiation levels at worst-case conditions.*
3. *10% worst-case particle environment, geosynchronous orbit, 0.025" of aluminum shielding. Specification set using the CREME code upset rate calculation method with a 2 µ epi thickness.*

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RH ONO Technology TID Data - PROM

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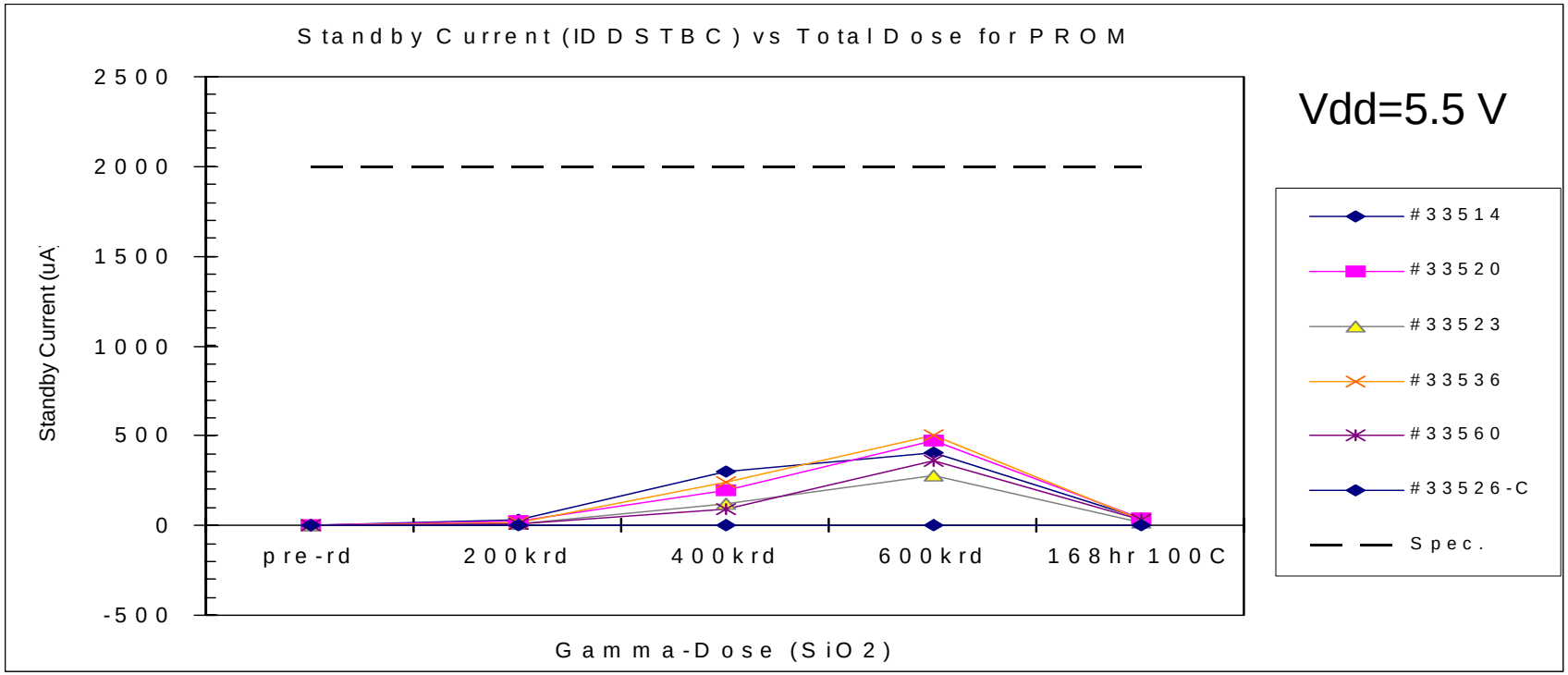

- Active current, VIL, VIH, Access time and chip enable time all remain stable through 600 Krd

RH ONO Technology Exceeds 400 Krad TID Requirements

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ONO RHFPGA Program Status

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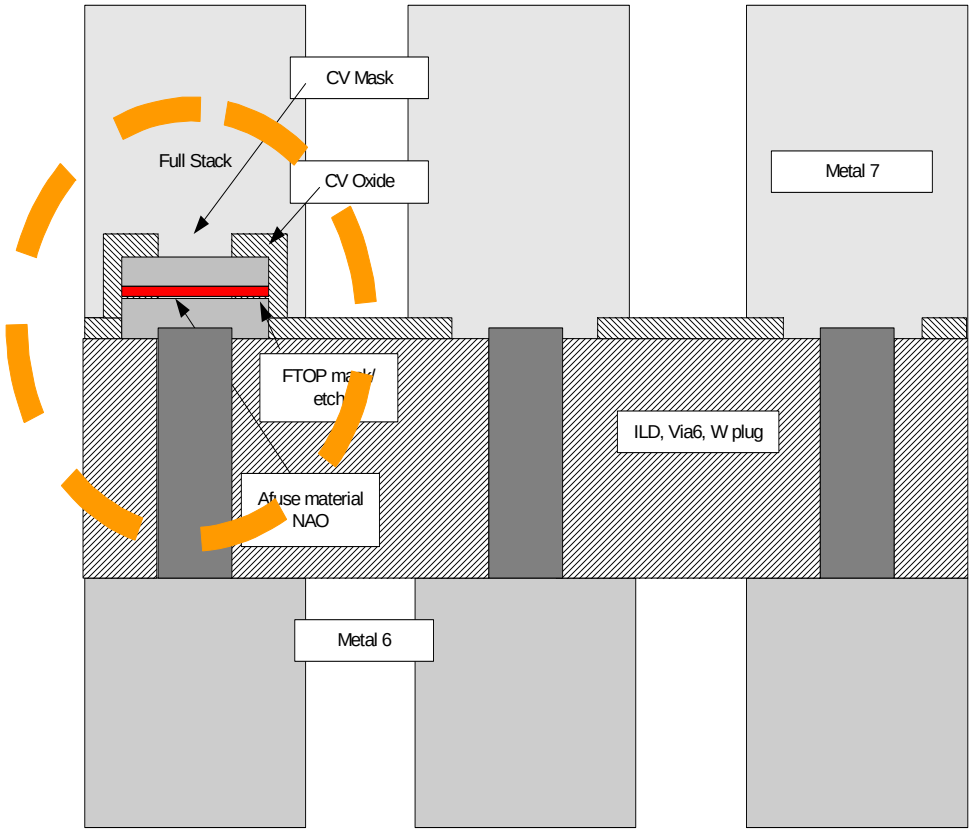
- Successfully reinstalled ONO process technology
- Flight-qualified PROM production restarted
- RH1280B prototype hardware successfully built and tested, additional hardware being built in accordance with qualification plan.
  - BAE acquired license from Actel to produce, market and sell RH1280 FPGA's
  - SEGR completed successfully, TID testing in progress this week
- RH1020 FPGA market assessment underway for potential product reinstallation.

RH1280B FPGA Flight Hardware Orders being taken

For shipments in 2008

Metal to Metal Antifuse Based FPGA's

Antifuse integrated in BEOL



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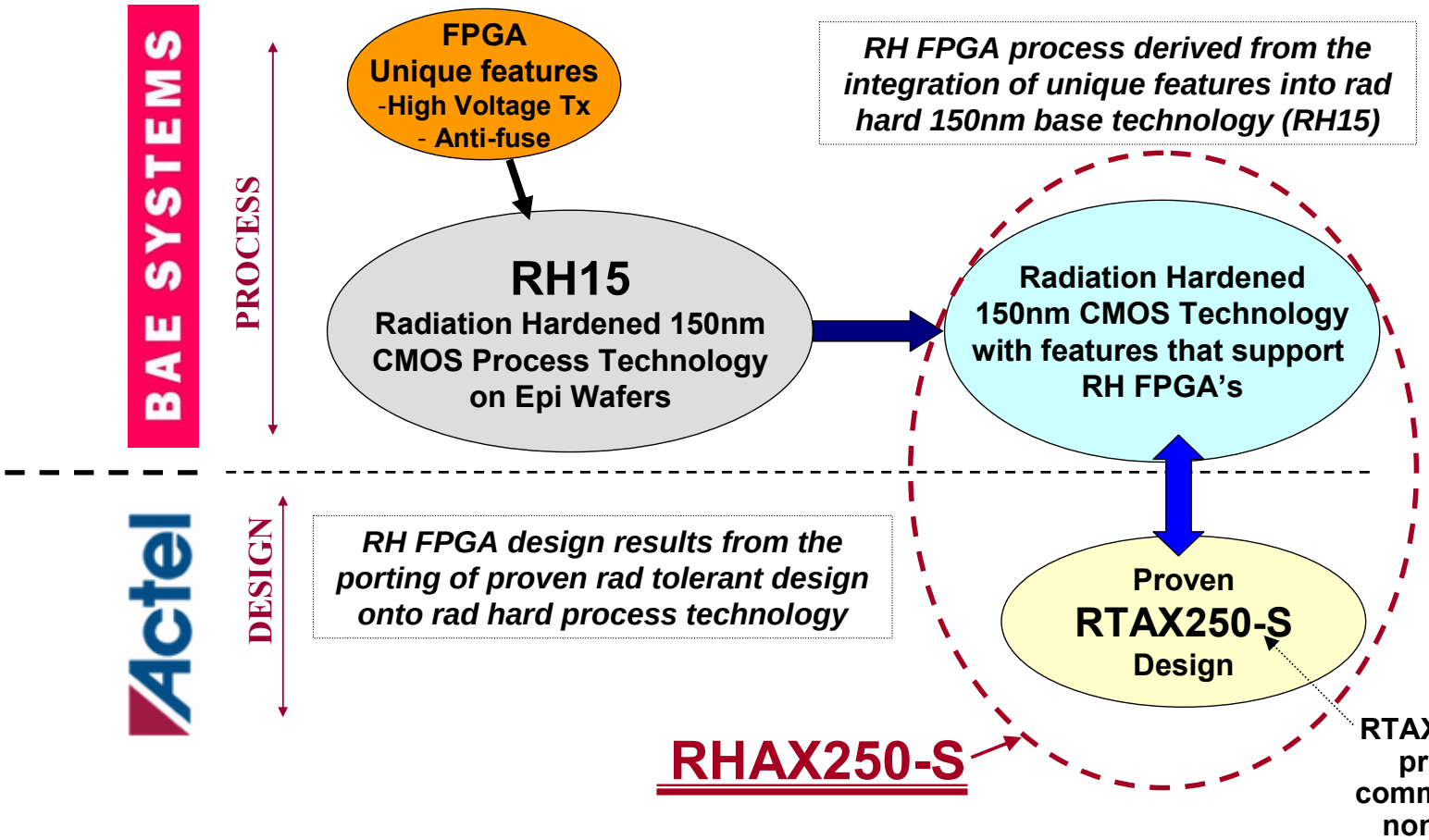
Product Installation Approach

Low Risk: Port a proven RT design to a validated RH process.



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RHAX250-S Installation and Qualification Roadmap

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Approach

RTAX250-S

- RT AX250-S design transferred to BAE

Process & Design Rule Development

- assess RTAX design rules & process details
- define process flow
- create parametric targets
- build & evaluate short loops (Hi-V Tx; antifuse)

Process Integration / Technology Validation

- design technology characterization vehicle (TCV)
- build & evaluate full TCV lots

Product Demonstration
Prototypes Built & Tested

QML Qualification

- perform qualification testing on FPGA samples taken from ≥ 3 lots

RHAX250-S

- flight qualified product, same form/fit/function

Port Other RTAX Designs

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- Introduction
- **Technology Features**
  - 150nm Rad Hard CMOS
    - Antifuse Programming Element
- RHAX250-S Product Description
- Radiation Hardness
  - TID Test Results
  - SEU/SET Test Results
- Summary and Plans

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RH15 Technology Features

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Rad Hard 150nm CMOS Technology (RH15) Features

Minimum Feature Size	150nm
Isolation	Shallow Trench Isolation
Device Options	26 Å / 70 Å
S/D Engineering	Halo with S/D Extensions
Supply Voltages	1.5V / 3.3V
Gate Electrodes	N+ Poly (NFET) / P+ Poly (PFET)
Metal Levels	7 Levels (Planarized BEOL)
Poly & Diffusion Silicide	$CoSi_2$

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RH15 QML Qualification Test Summary

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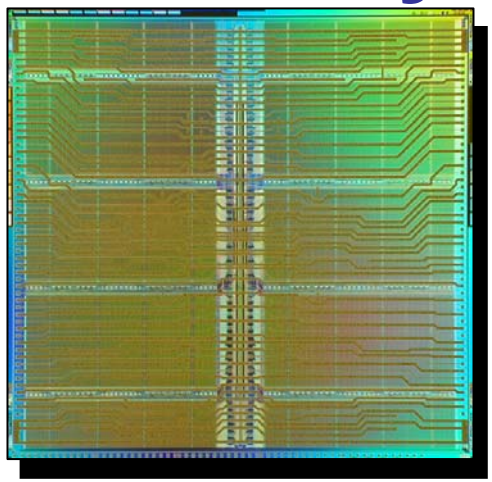
Qualification Test Vehicle:

4M SRAM



- Chip Image: 17.6 mm x 17.1 mm
- 6T2R1C cell
- 31 Masking Levels
- Six Metal Levels
- Number of Transistors : 30M
- Number of Resistors : 8M
- Number of Capacitors : 4M
- Number of Contacts : 100 M
- Number of Vias : 70 M
- Wiring Length : ≈1Km

Qual Tests:

✓ Group A:	All Electrical Tests	PASSED
✓ Group C:	1000- Hr / 125°C Life Test	PASSED
✓ Group E:	All Radiation Testing	PASSED

✓ Latchup	Immune
✓ Single Event Upset	<< 1E-10 upsets/bit-day
✓ Total Ionizing Dose	> 2 Mrad(Si)
✓ Prompt Dose Upset	> 1E9 rad(Si)/s
✓ Prompt Dose Survivability	> 1E12 rad(Si)/s

Demonstrated

All Qualification Testing Completed Successfully

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RH15 Performance Assessment

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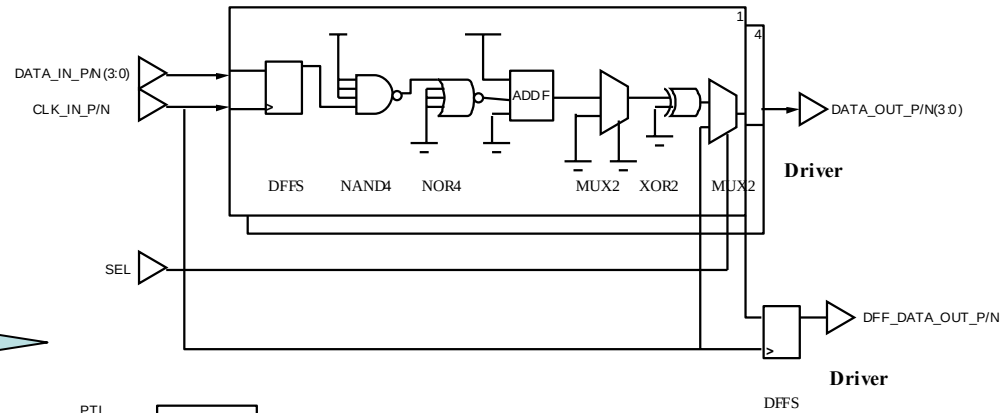
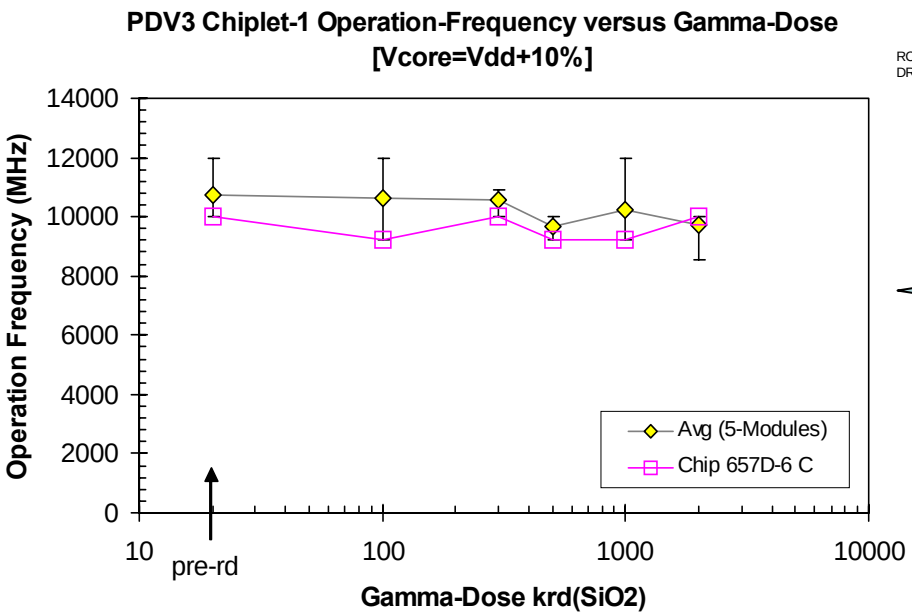
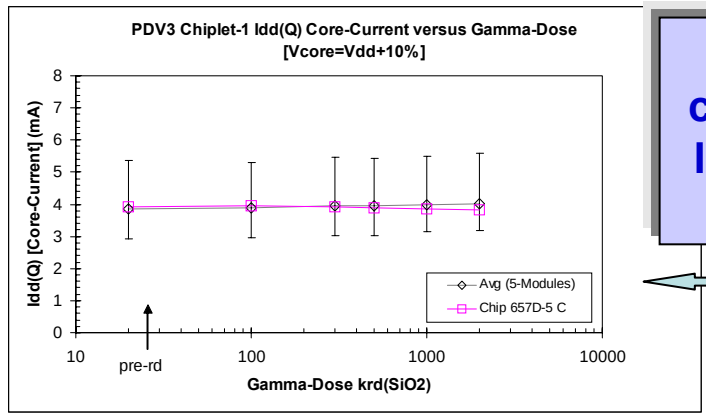
High Speed Circuit Testing
to measure on-chip gate delay.

Logic Representation of High Speed Signal Paths





Results confirm >1GHz performance both pre- and post-irradiation (2 Mrd(SiO_2))



No change in Iddq with dose.

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RH15 Reliability Test Results Summary

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Category	Requirement	Results
PFET Hot Carrier	10% shift in Vth @ 10-year life	Exceeds requirement
PFET NBTI	10% shift in Vth or 20% Ids change @10-year life	Exceeds requirement
NFET Hot Carrier	Less than 20% degradation in Ids @ 10-year life	Exceeds requirement
Gate Oxide Integrity	Less than 0.01% Cum. failure @ 10-year life	Exceeds requirement
Mobile Ions	Less than 5E11/cm2	No issue
Interconnect EM	Less than 0.01% Cum. failure @ 10-year life @ current density of 0.5 mega-A/cm2	Exceeds requirement
Interconnect Temp-Cycle	Less than 20% change in resistance	No change in resistance
Stress Migration	Less than 20% change in resistance after high Temp. stress for min stress time of 500 hours	Stress-migration is not an issue
BEOL Dielectric Integrity	Less than 5e-14uA/um2 leakage current after high Voltage/Temp. stress for 500 hours	No significant change in resistance

Reliability Assessments Exceed Requirements in All Categories

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Metal-to-Metal Antifuse

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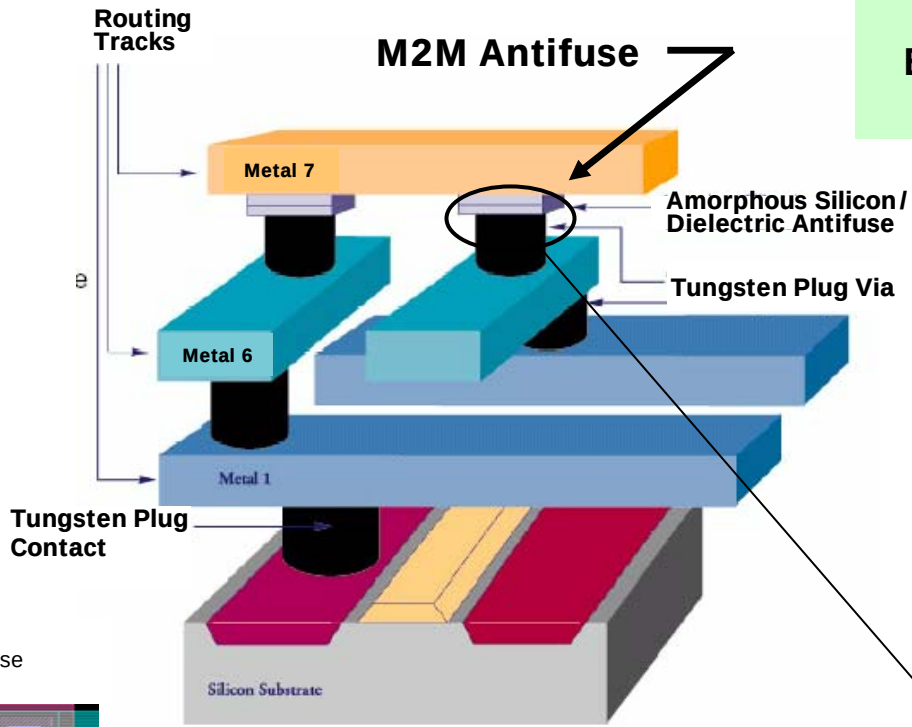
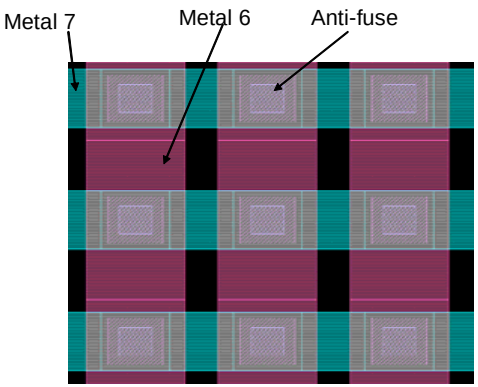
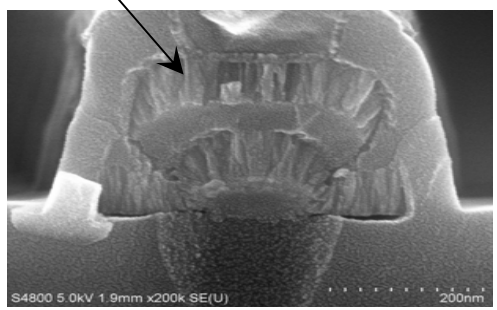
Antifuse Placement: Between to last two metal layers.





Metal to Metal Anti-fuse



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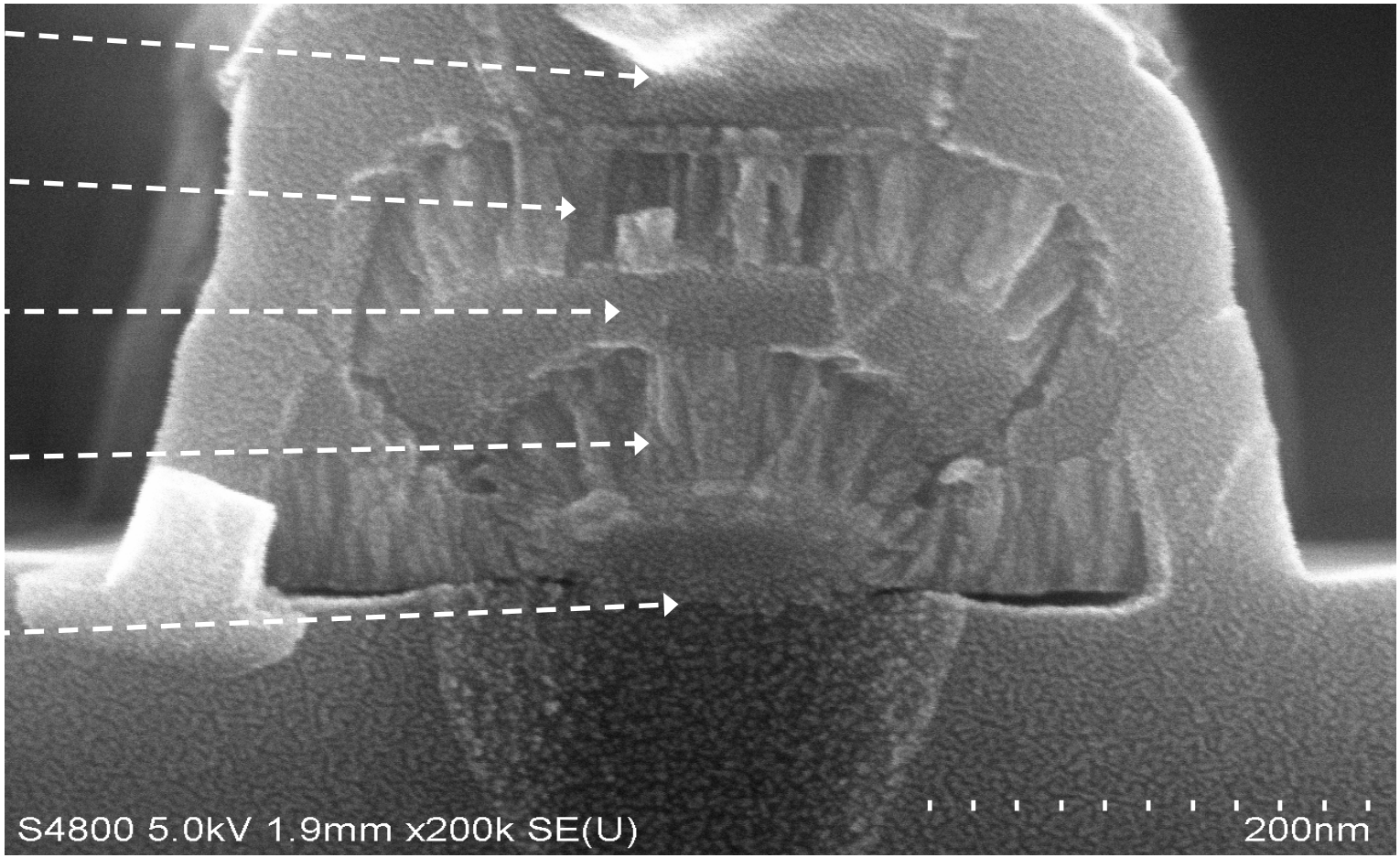
Antifuse Cross-section



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Antifuse Integrity

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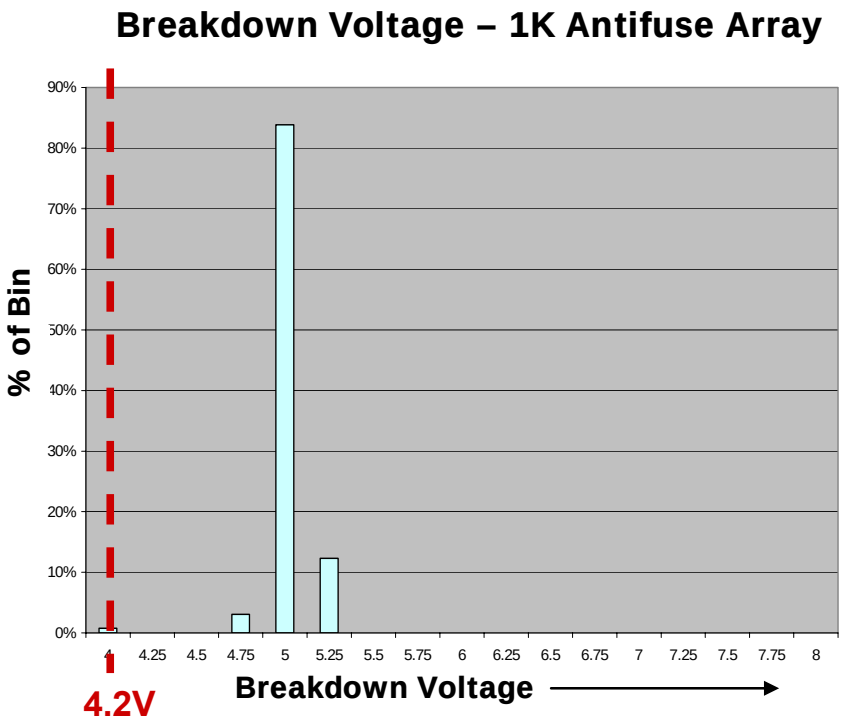

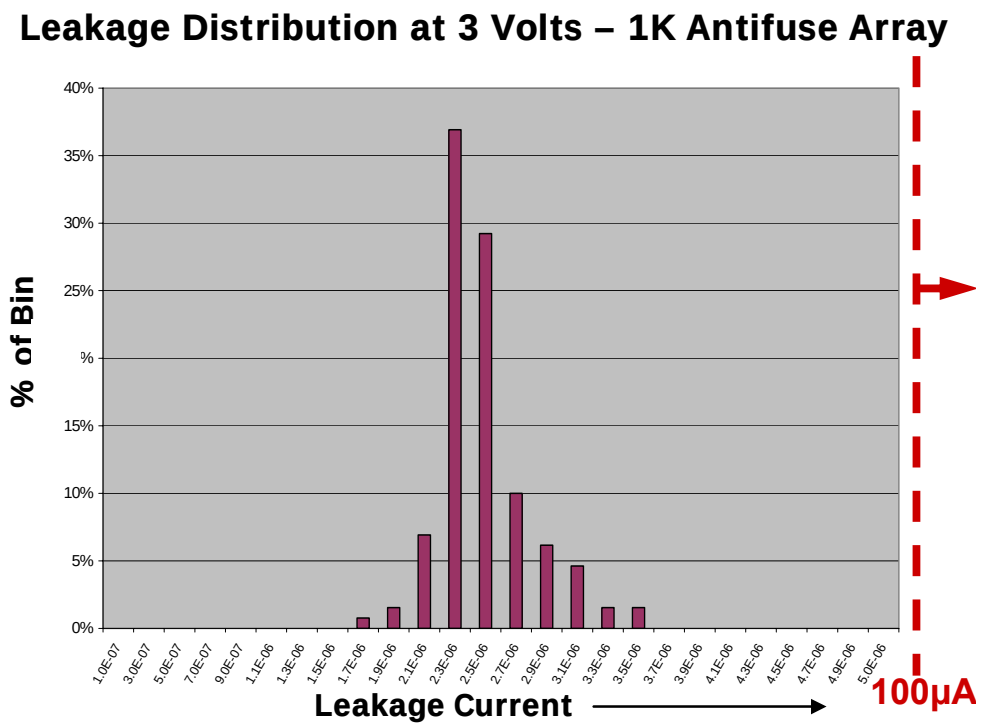

Breakdown Voltage Distribution Exceeds Requirement (>4.2V)

Leakage Distribution Far Exceeds Requirement (<100µA)

Excellent Fuse Integrity Test Results

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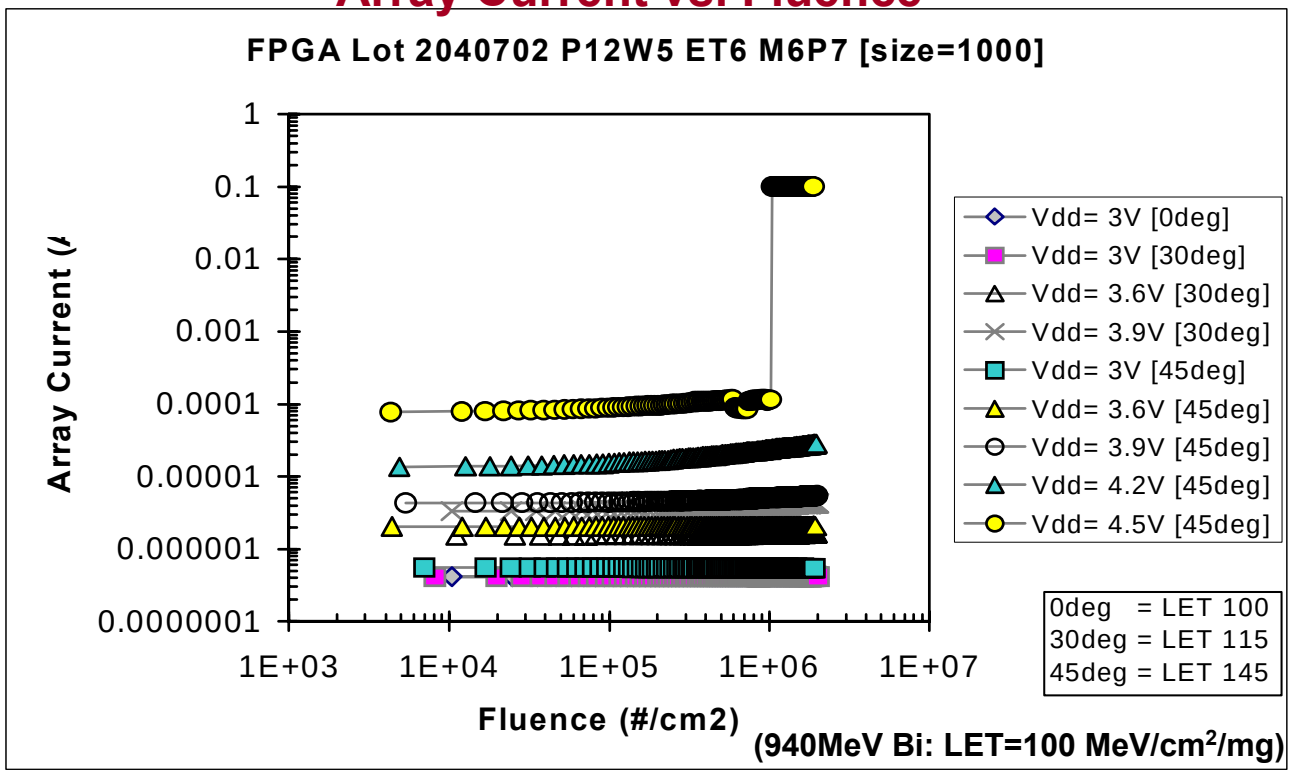
Early Assessment of SEDR

on RHAX antifuse arrays (1K)

SEDR = Single Event Dielectric Rupture

Array Current vs. Fluence



No Rupture Observed Up to Vdd = 4.2V
Demonstrating a large SEDR hardness margin for nominal 1.5V antifuse array

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RHAX250-S Description

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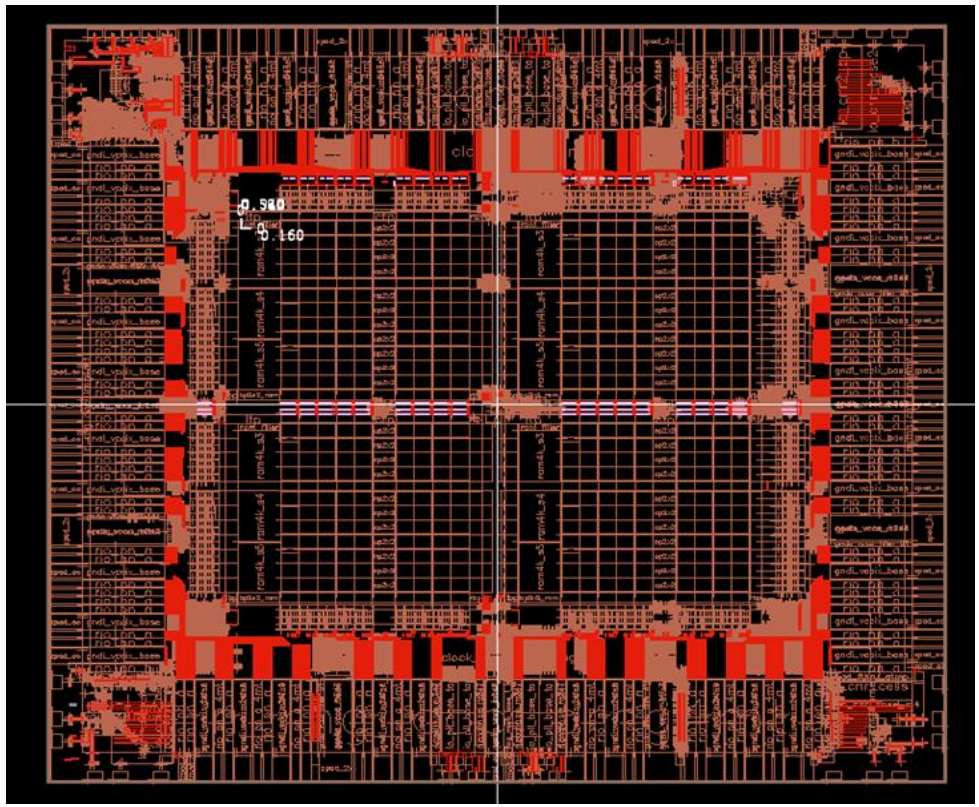

RHAX250-S **chip size : W=9.6mm; H=9.4mm**

Total Transistors :	5.589	million
Total Anti-fuse Elements:	7.743	million
Total Contacts	59.480563	million
Total Via's	132.824787	million

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RHAX250-S Module

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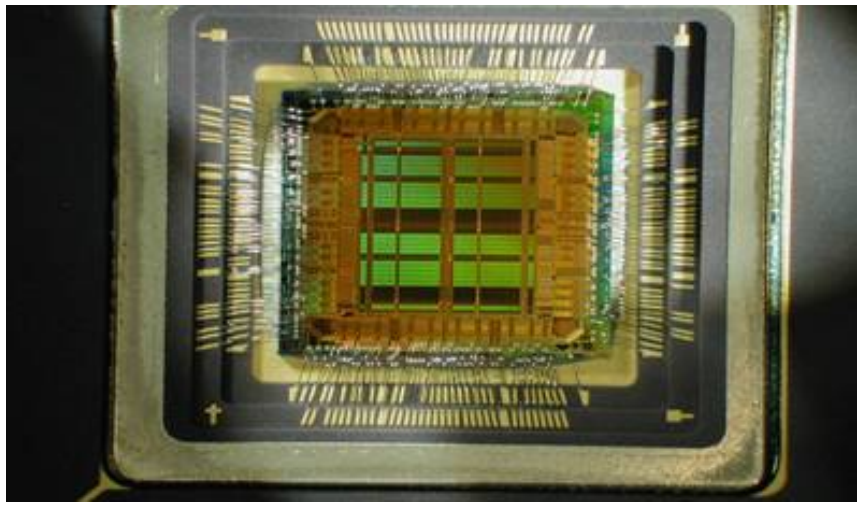

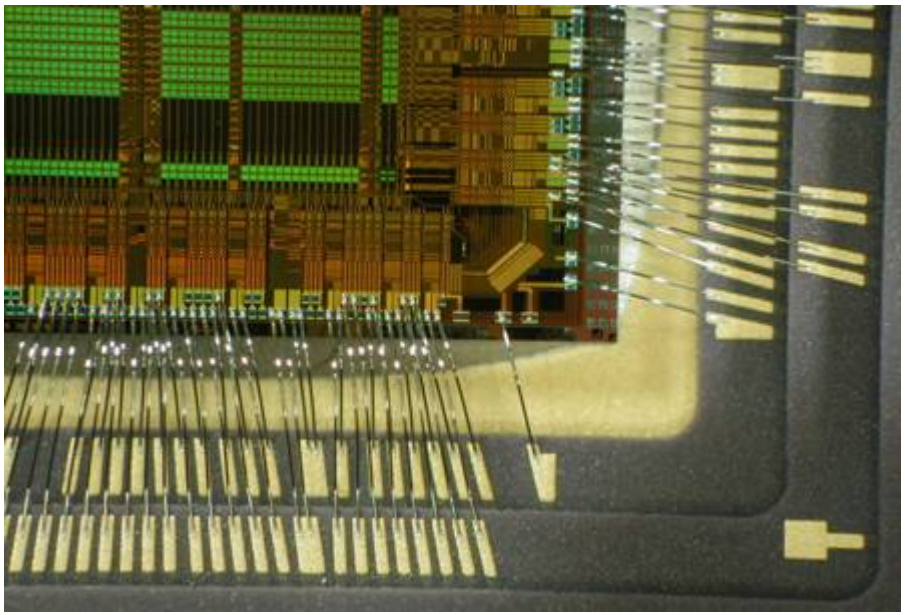

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RHAX250-S Product Profile

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Device	RHAX250-S
Capacity	
Equivalent System Gates	250,000
ASIC Gates	30,000
Modules	
Register (R-Cells)	1,408
Combinatorial (C-Cells)	2,816
Flip-Flops (Maximum)	2,816
Embedded RAM/FIFO (without EDAC)	
Core RAM Blocks	12
Core RAM Bits (K = 1,024)	54 K
Clocks Segmentable	
Hardwired	4
Routed	4
I/O's	
I/O Banks	8
User I/O's (Maximum)	248
I/O Registers	744
Package	
CCGA/LGA	-
CQFP	208, 352

Performance

- 1.5V Core; 3.3V I/O
- High-Performance Embedded FIFOs
- 350+ MHz System Performance
- 500+ MHz Internal Performance
- 700 Mb/s LVDS Capable I/Os

Radiation Hardness Targets

TID	≥ 1Mrad(Si)
DR Upset	> 1E9 rad(Si)/sec
SEL	Immune
SEU_{REGS}	< 1E-10 errors/bit-day (TMR-hardened)
$SEU_{e\text{-}RAM}$	< 1E-10 errors/bit-day (EDAC)

RHAX FPGA will have the identical form, fit, and function of its RTAX counterpart.

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RHAX250-S Prototype Hardware

Recently built prototype RHAX250-S FPGA's have yielded functional hardware, despite anomalous Hi-V Tx junction leakage.

Modules were programmed for total ionizing dose testing.

Circuit elements tested per module:

- 12 blocks of 4Kx1 SRAM (total: 48K)
- 1408-stage DFF register string
- Two 1408-stage logic chains

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RHAX250-S TID Test Results

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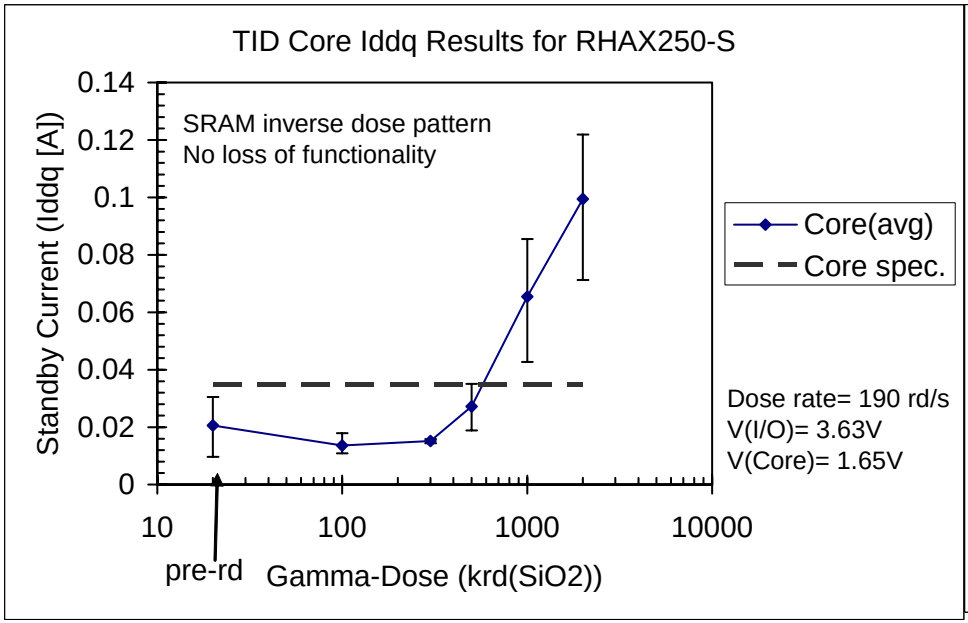
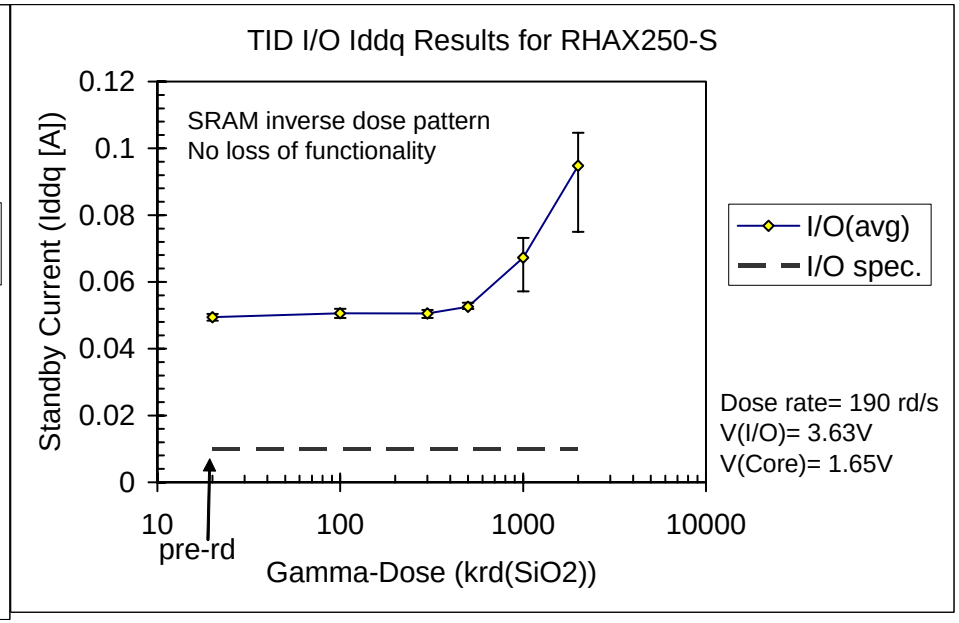
RHAX250-S modules remained fully functional throughout testing to 2Mrd($Si0_2$)





TID test results on prototype FPGA's demonstrate improved hardness. Hardening process adjustments are being implemented to further enhance hardness.

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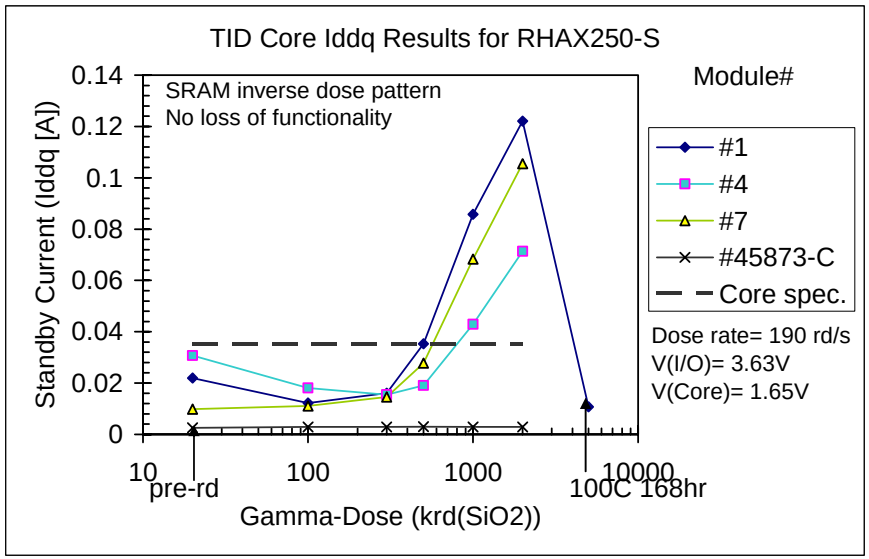
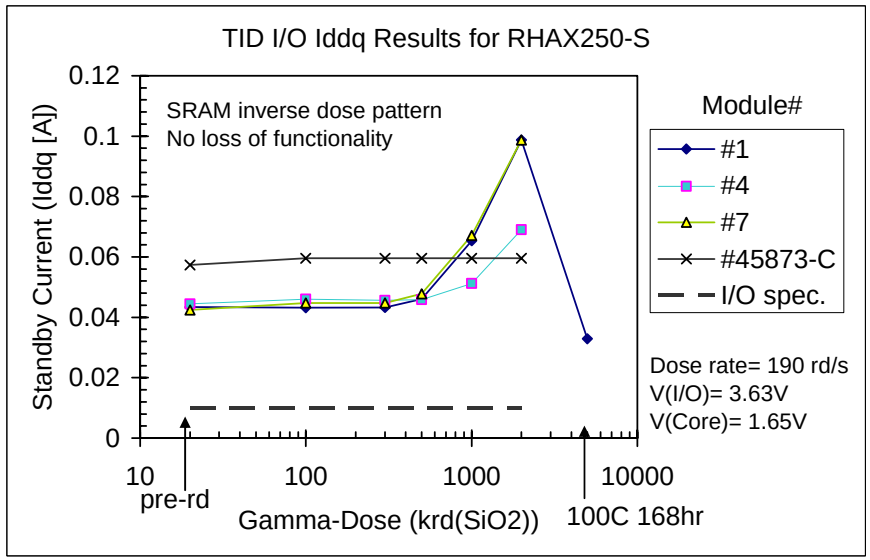
RHAX250-S TID Test Results

RHAX250-S modules remained fully functional throughout testing to 2Mrd(SiO_2)





These results demonstrate prototype capability

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Hardened Flip-Flop Design

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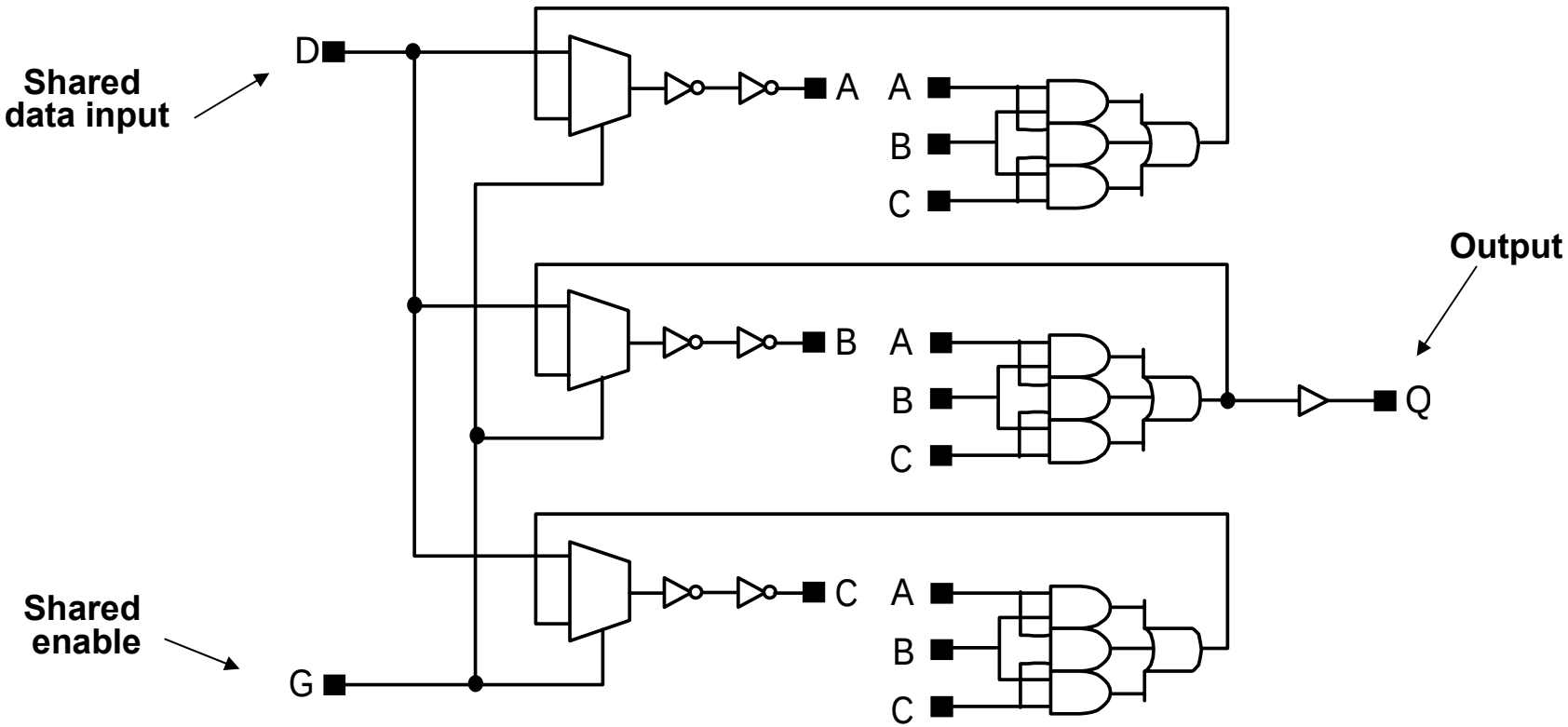
Uses Triple Modular Redundancy (TMR) [hard-wired]



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SEU Test Circuit

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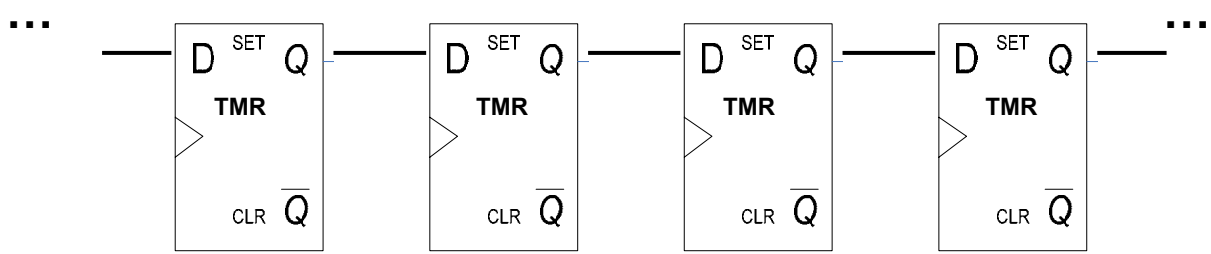
200-stage DFF chains
Clock: 2 MHz



Reference: J.J. Wang, W. Wong, S. Wolday, B. Cronquist, J. McCollum, R. Katz, and I. Kleyner, “Single Event Upset and Hardening in 0.15 µm Antifuse-Based Field Programmable Gate Array,” *IEEE Trans. on Nucl. Sci., vol. 50, No. 6, Dec. 2003.*

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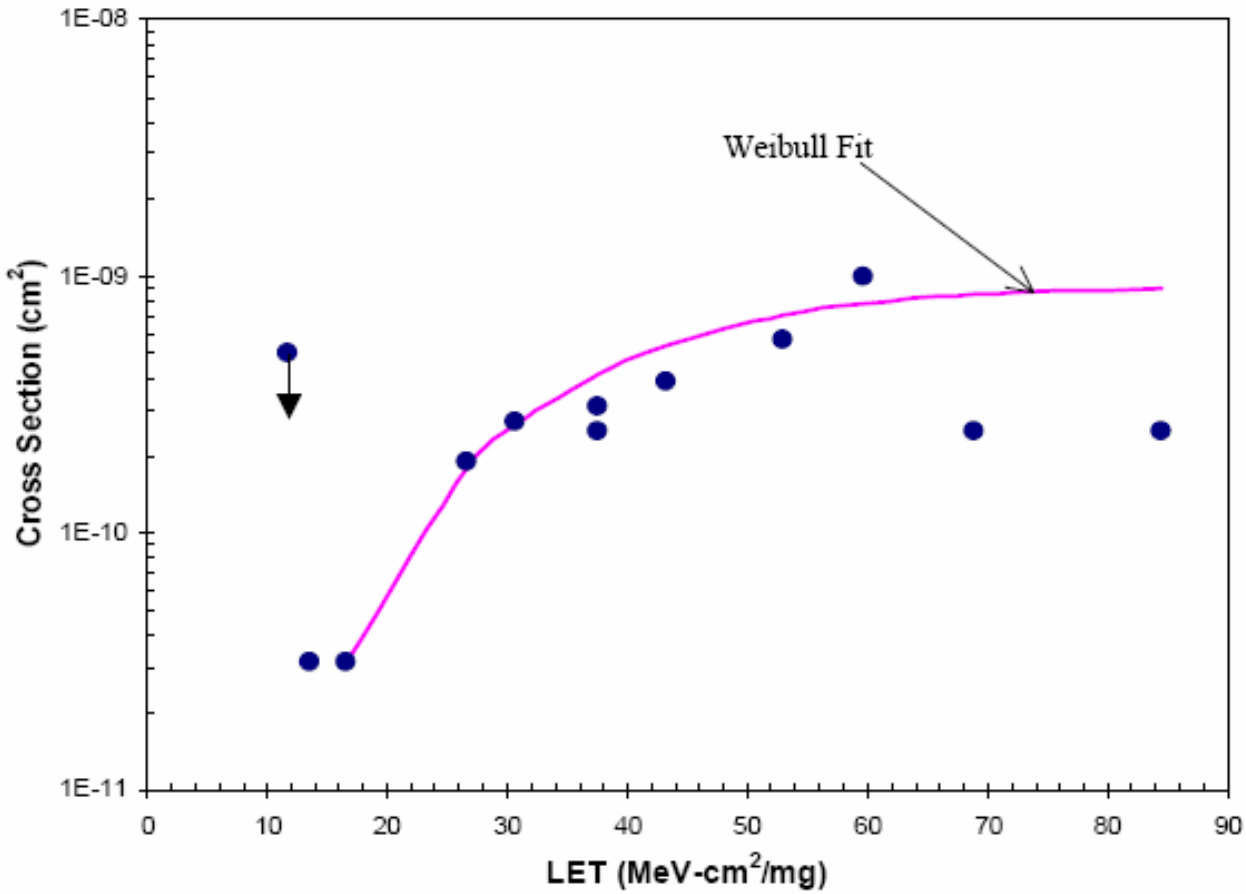
SEU Test Results

on RTAX hardware



SEU Rate: 1.96E-11 upsets/bit-day*

* assumed radiation environment: GEO-min and 100 mil Al shielding

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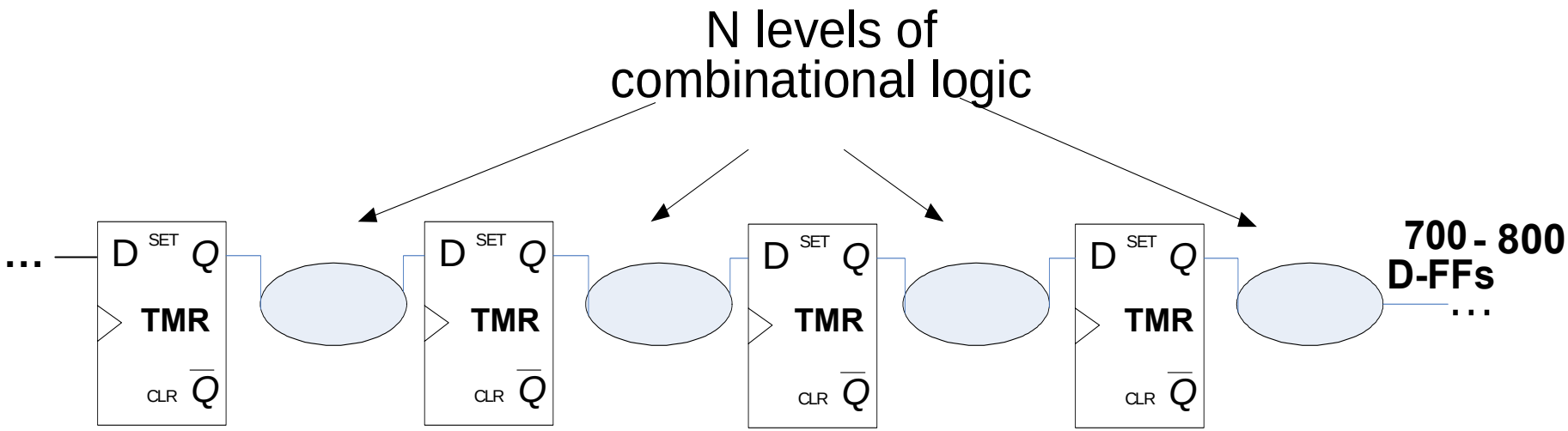
SET Analysis Circuit

BAE SYSTEMS

DFF chain with interwoven combinational logic



Signal Frequencies: 15MHz, 37.5MHz, 75MHz, and 150MHz

Reference: M. Berg, J.J. Wang, R. Ladbury, S. Buchner, H. Kim, J. Howard, K. LaBel, A. Phan, T. Irwin, and M. Friendlich, "An Analysis of Single Event Upset Dependencies on High Frequency and Architectural Implementations within Actel RTAX-S Family Field Programmable Gate Arrays," *IEEE Trans. on Nucl. Sci.,* vol. 53, No. 6, Dec. 2006.

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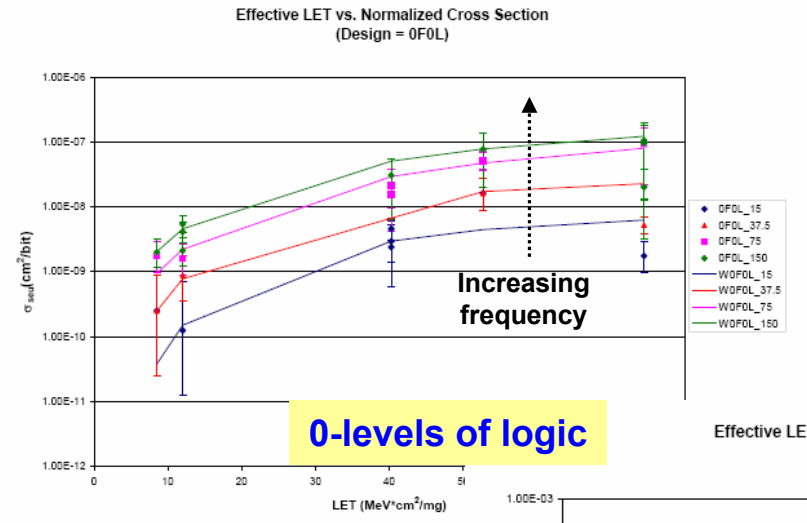
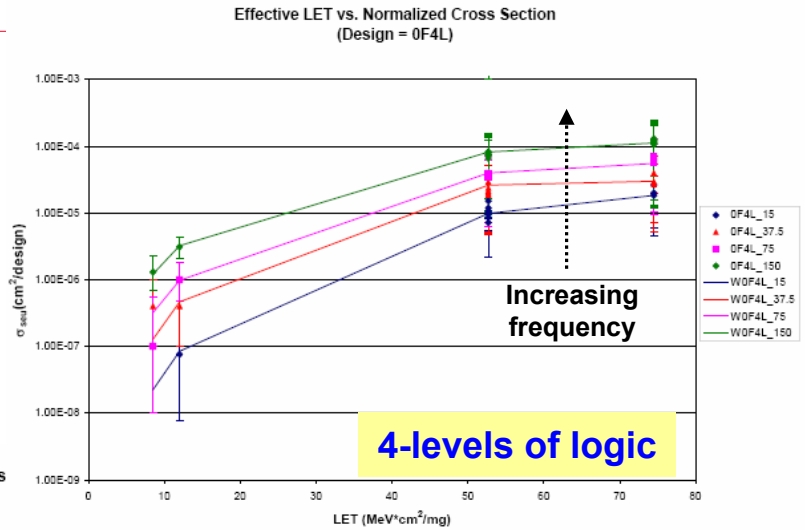
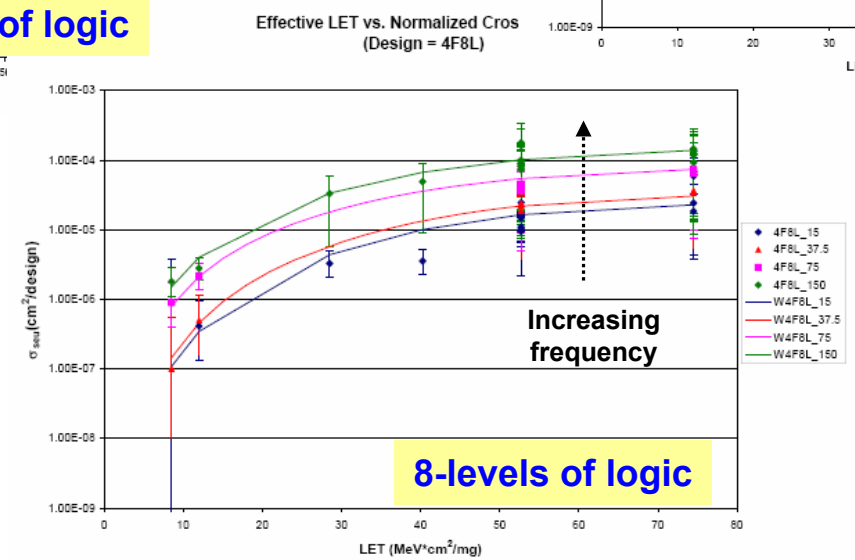
SET Test Results
on RTAX hardware

BAE SYSTEMS







Weibull fits to SET test data

SEU susceptibility increases for increasing signal frequencies and for increasing levels of logic.

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Predicted SEU Rates

vs. logic level & freq.

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Predicted SEU Rates (errors/bit/day) *

Levels of Intervening Logic	Signal Frequency 15 MHz	37.5 MHz	75 MHz	150 MHz
8-Levels	5.31E-09	7.88E-09	3.75E-08	8.17E-08
4-Levels	2.01E-09	8.71E-09	1.89E-08	6.29E-08
0-Levels	6.08E-10	5.14E-09	2.84E-08	5.84E-08

Worsening SEU Rate

* assumed radiation environment: GEO-min and 100-mil Al shielding

(Probability of Generating an SET)

Logic

Frequency

(Probability of Capturing an SET)

Impact of SET on error rate depends on circuit design and signal frequency.

Further SEU Enhancements projected in Rad Hard Process

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Outline

Introduction

Technology Features

- 150nm Rad Hard CMOS
- Antifuse Programming Element

RHAX250-S Product Description

Radiation Hardness

- TID Test Results
- SEU/SET Test Results

→ **Summary and Plans**

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Future Work - RHAX

BAE SYSTEMS

- Build more hardware incorporating identified process enhancements for improved yield and hardness
- Subject functional hardware to full battery of reliability and radiation testing
- QML qualify the RHAX process technology
- Begin full RHAX250-S wafer production to supply Actel
- Port additional Actel RTAX FPGA designs onto rad hard process technology at BAE to extend rad hard offerings.

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Summary

- BAE and Actel are continuing their >12 year collaboration as rad hard FPGA suppliers.
- Next generation rad hard product is being built and tested.
- Total dose test results on RHAX250-S hardware demonstrates improved hardness over RTAX250-S.
- Single-event effects test results demonstrates product design's high tolerance.
- Electrical, radiation, and reliability testing is on-going.
- Full flight-qualified production to begin by yearend.

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Acknowledgements

The authors gratefully acknowledge the support for this effort provided by the Defense Threat Reduction Agency under contract DTRA01-03-D-0007 / 0004.

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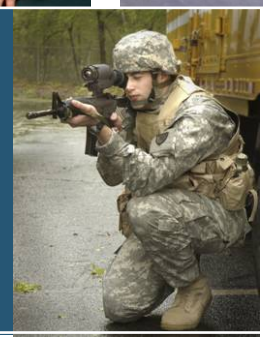


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