Radiation Hardened Field Programmable Object Array (FPOA) for Space Processing

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MathStar Timeline

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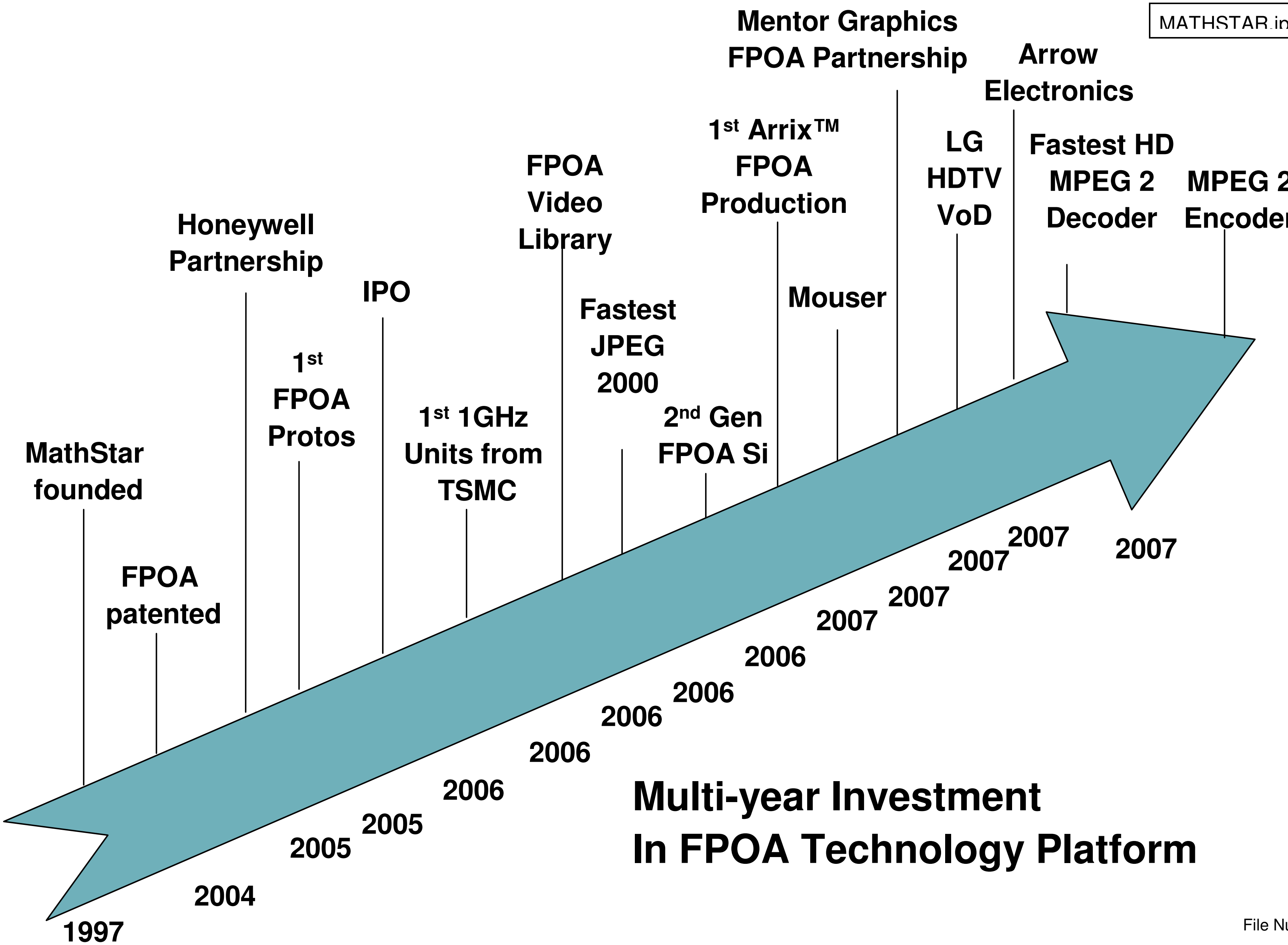

Multi-year Investment
In FPOA Technology Platform

Arrix FPOA Value Proposition

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- 1 GHz "ASIC-like" Performance

  Up to 4 times FPGA performance

- Customer Programmable Device

  Fast TTM, No NRE

- Application support

  Quick Start with Libraries of IP Cores

- Mentor Graphics Design Flow

  Tools supported by Industry Leader

FPOA Architecture Overview

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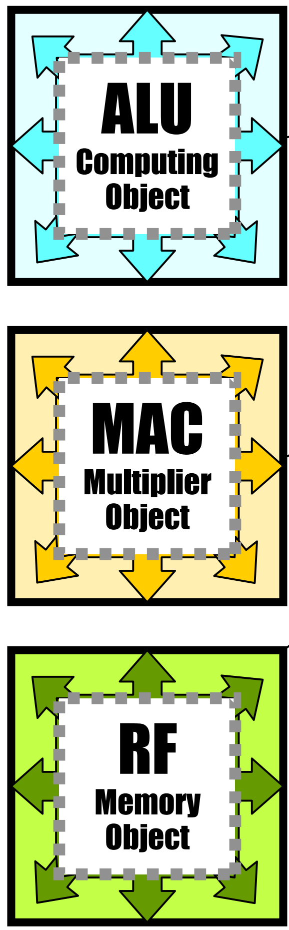
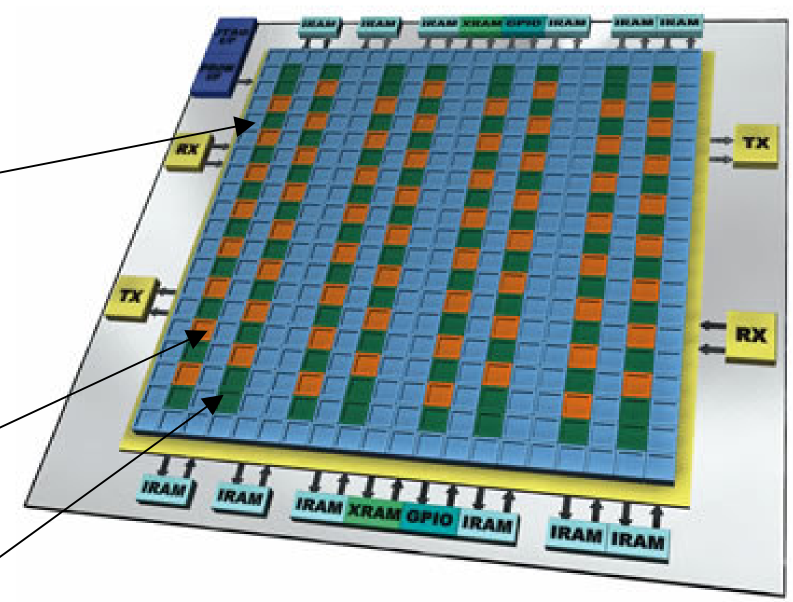
FPOA Objects

Building Blocks



1 GHz Object Array



Object Architecture

- Coarse-grained Architecture
- Same inter-object communication
- All synchronized at 1 GHz

Objects arranged by abutment

- Enables 1 GHz performance
- Manageable design with hundreds of objects -vs- sea of gates

Two Layer, 1 GHz Interconnect

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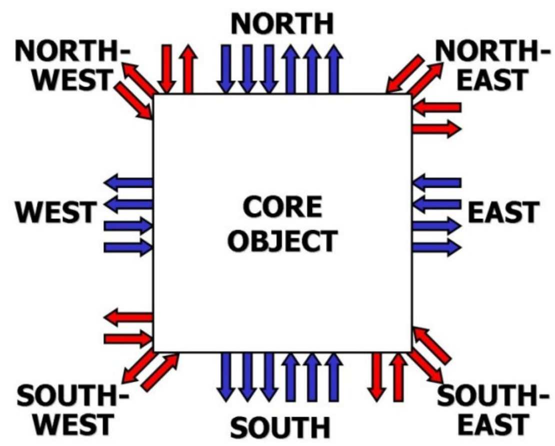
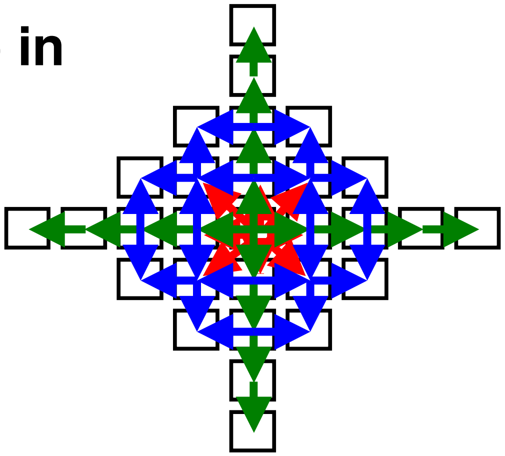
- **21-bit Interconnect Lanes**
  - **16 registered data bits (R Bits)**
  - **4 Control bits (C Bits)**
  - **1 Valid Bit (V Bit)**
  - **1 GHz speeds**



- **Nearest Neighbor Interconnect**
  - **8 Per Object**
  - **Range of 1 object (N/E/S/W, diagonals) in 1 clock cycle**



- **Party Line Interconnect**
  - **10 Per Object**
    - 6 North / South, 4 East / West
  - **Range of 4 Object hops in One Clock Cycle**

FPOA Performance Scales

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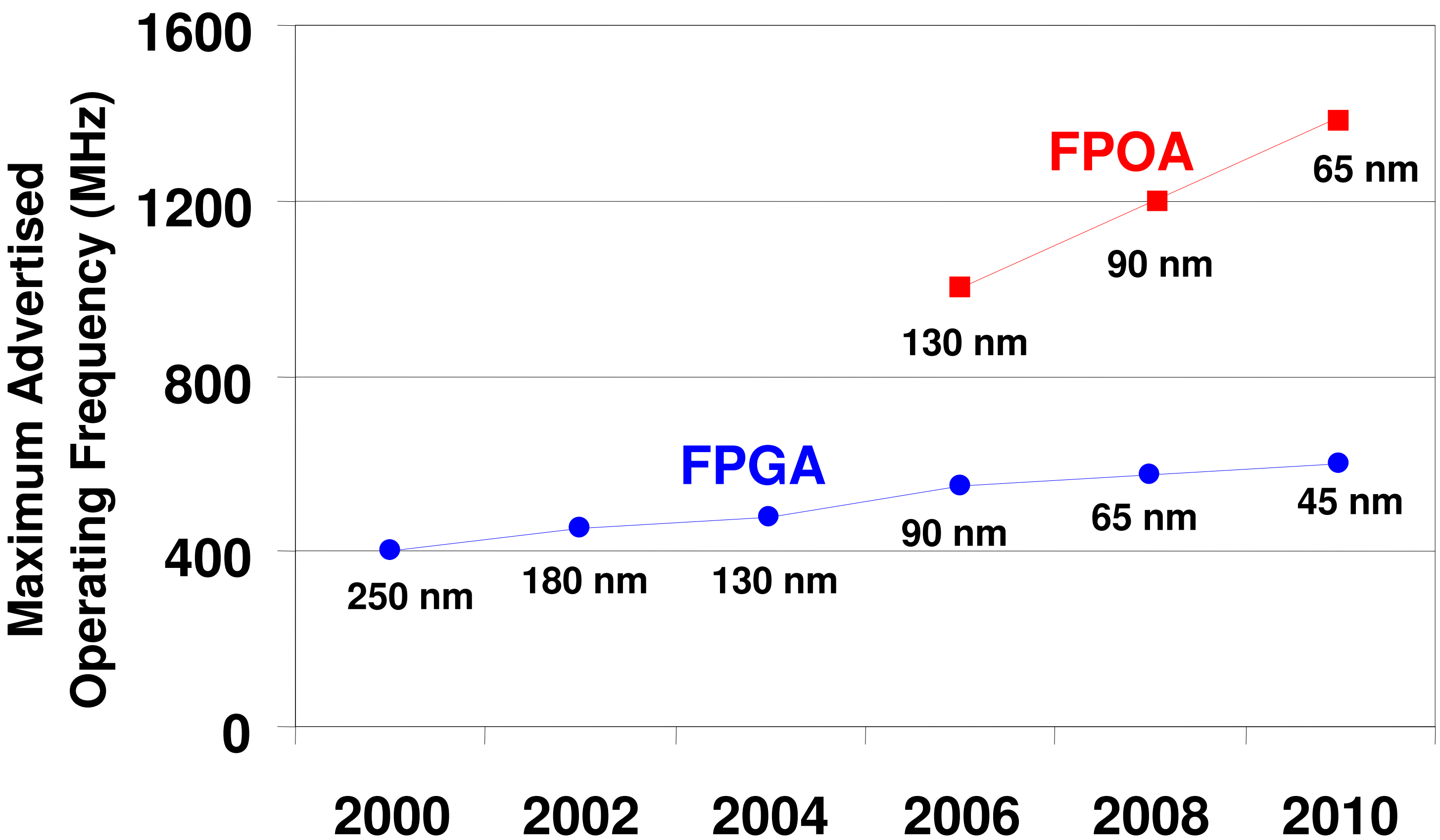

FPGA cites maximum advertised frequency, actual clock rates after timing closure are typically much lower than maximum
FPOA cites actual clock rates
All historical and forecasted numbers are estimates of MathStar, Inc.

What is Holding FPGAs Back?

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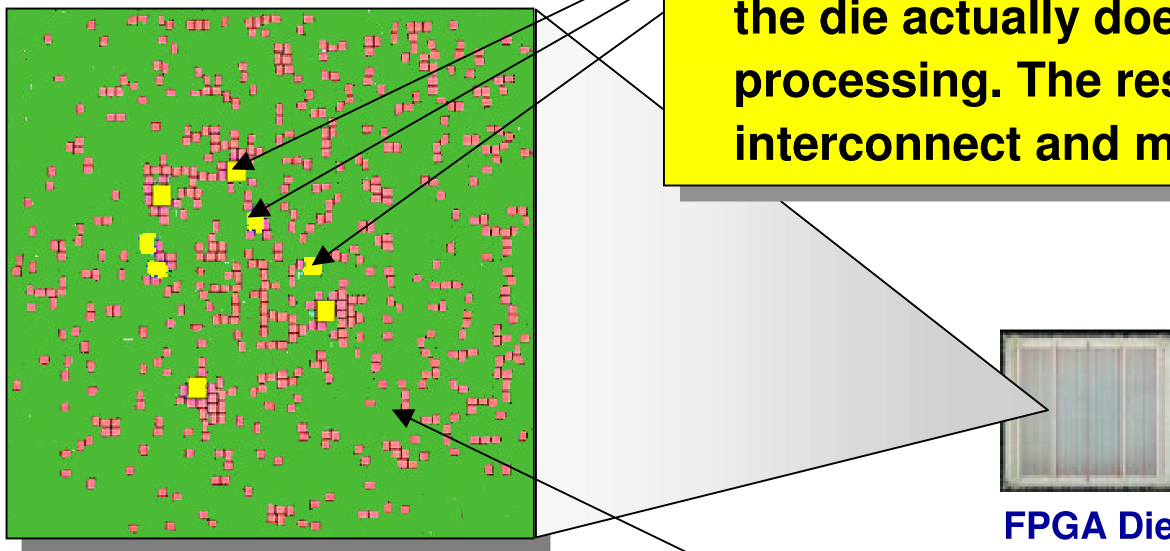
Expensive: A small fraction of the die actually does processing. The rest is interconnect and memory



FPGA Die

4X LUT4 Architecture Tile in FPGA*
35,462 μ² @ 0.18μ

- Buffer
- SRAM
- Multiplexer
- LUT
- Flip Flop
- Pass Transistor Switch
- Buffered Switch

Slow: Have to navigate a lot of interconnect to get to the logic.

*Source: "Automatic Transistor and Physical Design of FPGA Tiles from an Architectural Specification" - K.Padalia, Jonathan Rose, et al.

LG Electronics bets on MathStar

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FOR IMMEDIATE RELEAS

MathStar Collabor
Solution for Delive

HILLSBORO, Ore., March 20 semiconductor company special announced today that it is worki the migration to MPEG-4 high-d MPEG-4 is a multimedia standa (MPEG).

After an exhaustive evaluation p programmable object array (FPO deliver satellite HD programmin LG's transcoder reformats H.26 existing MPEG-2 receivers.

"MathStar's FPOA technology needed to effectively deploy hig are pleased to be working with LG Electronics, a long-time HD advocate, the lodging industry's market leader and a company that has always been at the forefront of video technology."

Richard M. Lewis, senior vice president, technology and research, for LG's U.S. R&D subsidiary, said, "Programmable logic technology from MathStar was critical to allowing our satellite transcoders to support a large installed base of legacy TV receivers. In turn, these transcoders are important components in LG's end-to-end solution for bringing HD content to guest rooms."

-more-

March 20, 2007

After an exhaustive evaluation process, LGE selected MathStar's Arrix™ field programmable object array (FPOA) technology for high-definition "transcoders" that deliver satellite HD programming to hotel rooms. Specifically, the MathStar chipset in LG's transcoder reformats H.264 MPEG-4 satellite signals so they may be displayed on existing MPEG-2 receivers.

MathStar's Integrated FPOA Product Platform

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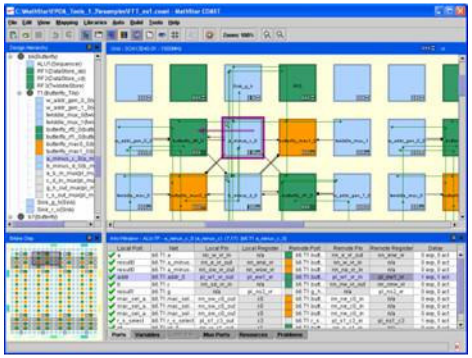
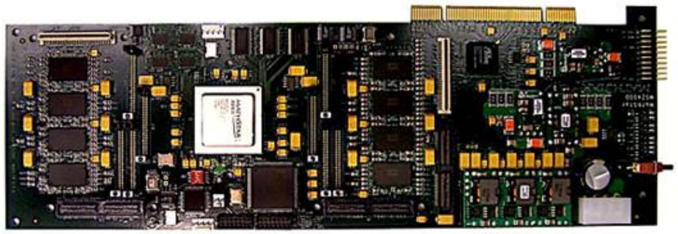
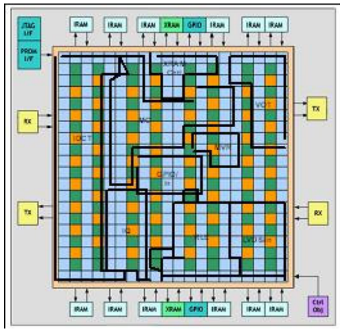
Arrix™ Family of FPOA chips
- Full production silicon shipping since Nov. 2006
- Yields and costs tracking to goals



FPOA Design Tools – version 2.0
- Mentor Graphics VisualElite™ front-end and simulator
- Integrated with MathStar COAST



FPOA Development System
- Integrated system containing tools, development boards & daughter cards to accelerate customer ramp



FPOA Application Libraries and IP Cores
- Professional video and machine vision
- Accelerate time to market, lower development costs

TTM For High Perf. Commercial Designs

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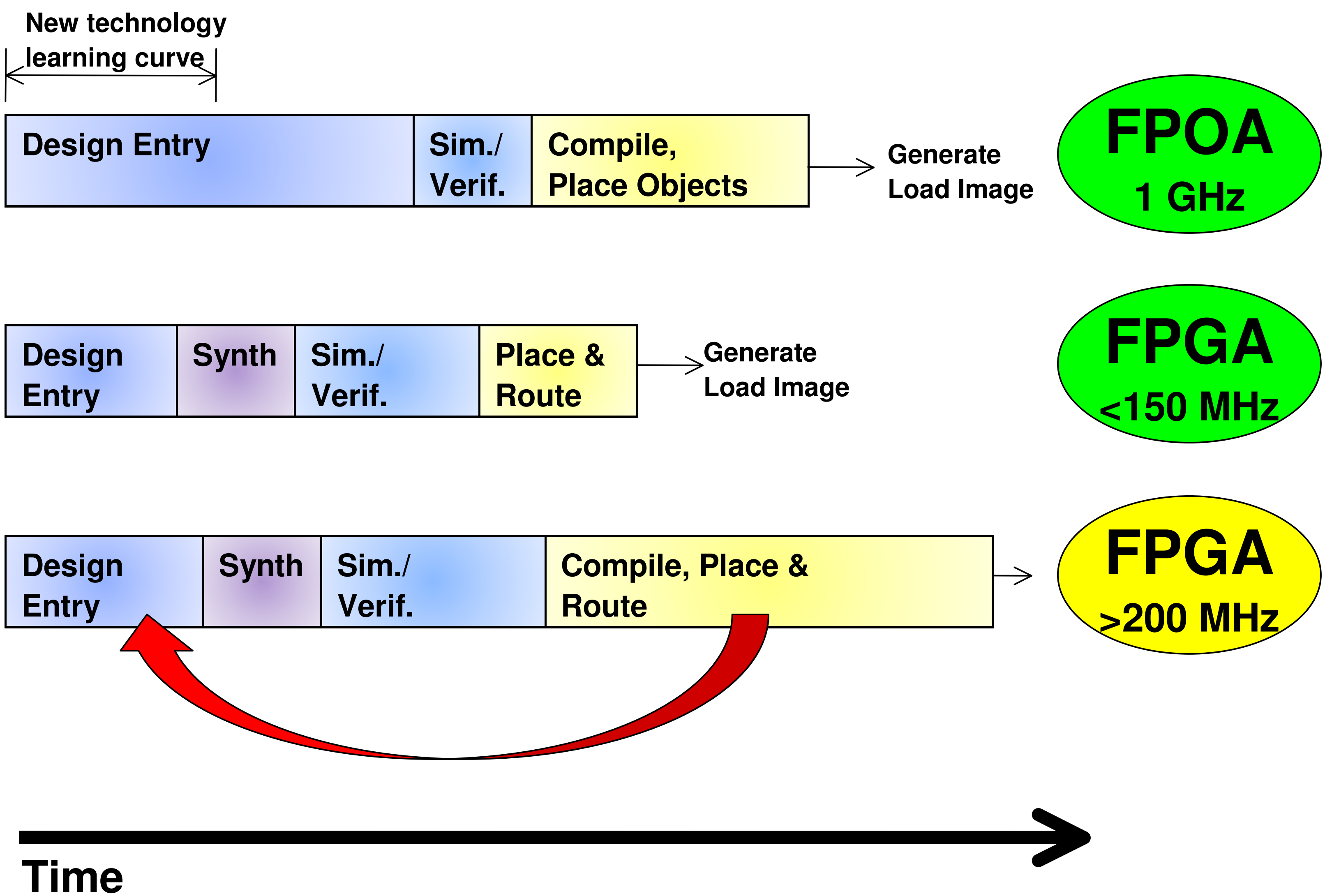

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MathStar FPOA Roadmap

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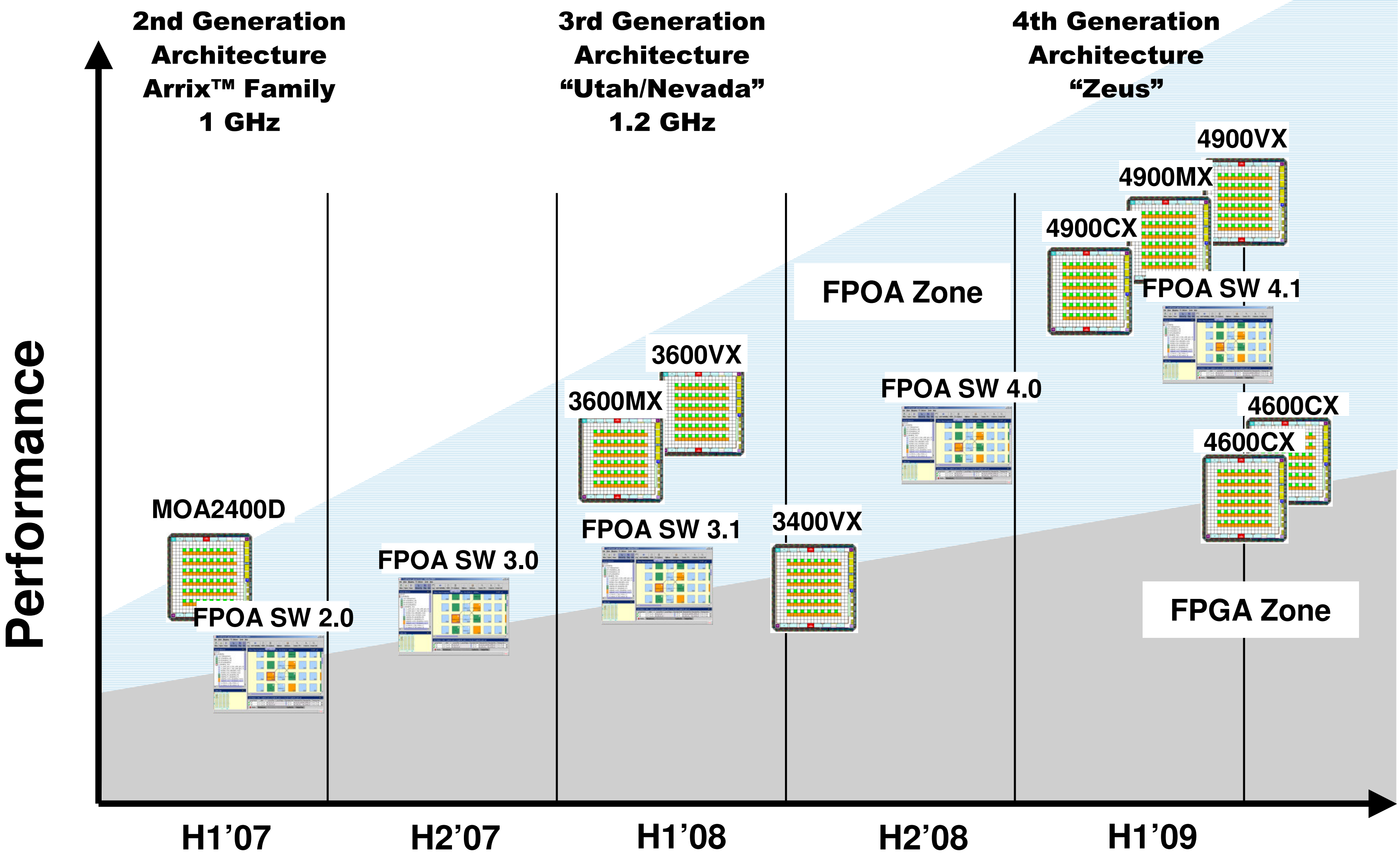

Note: Future device specifications and schedules are subject to change.

MathStar FPOA Roadmap

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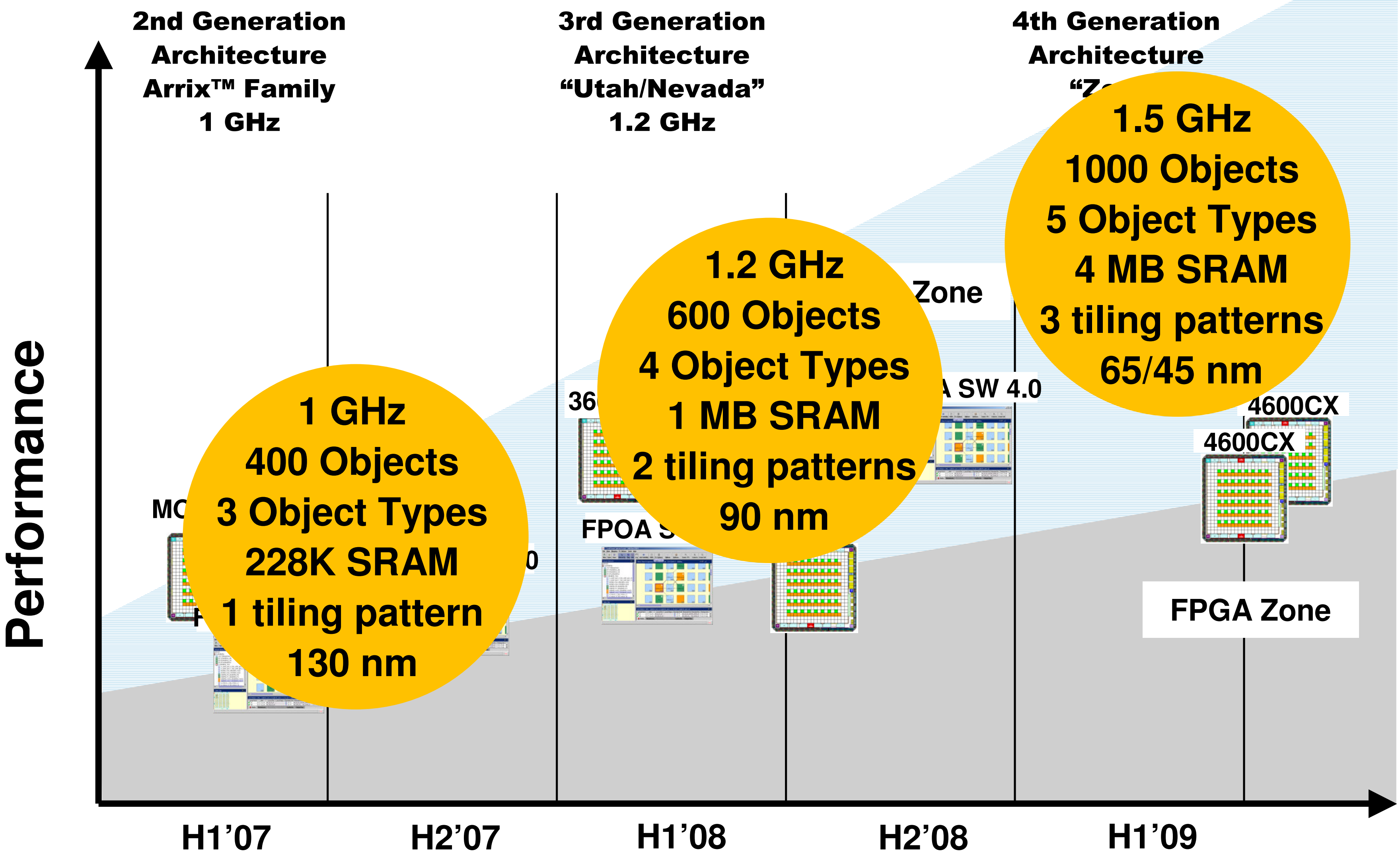

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Why is Honeywell interested in the FPOA for Space Applications?

FPOA Targeted Space Applications

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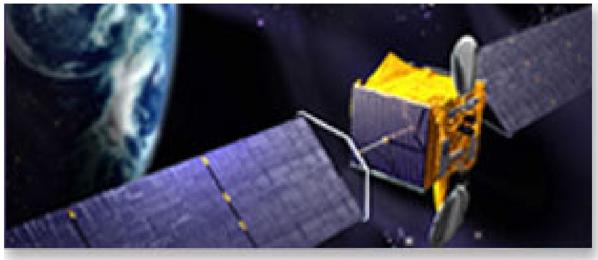

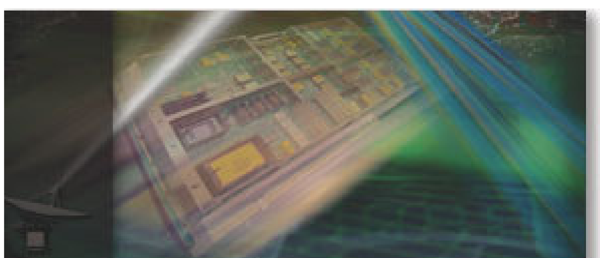

- EO/IR Sensor
  - Sensor Calibration
  - Spike Suppression
  - Temporal and Spatial Target Detection Processing
  - LOS Position and Amplitude Estimation
- Communications
  - PPF Analysis and Synthesis Filters
  - Beamforming
  - Limiting
  - FEC Encoding/Decoding
- Radar FEP
  - Subband Channelization and Recombination
  - Clutter Cancellation
  - Beamforming
- Compression & Downlink Data Management
  - Lossy Compression (Temporal/Spatial)
  - Lossless Compression (Rice)
  - Buffer Management

Advantages of FPGAs and ASICs

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FPOA has the potential to meet both technical and programmatic challenges in the high speed DSP area

FPGAs

- Reconfigurable
- Low Risk Device Availability
- Not performance-optimized
- Power Hungry
- Rad Soft
- Hard to Program

Custom ASICs

- Fixed Function
- Long, Serial Cycle Time
- Significant Design Risk
- Optimized for Performance
- Lower Power
- Rad Tolerant to Hard

FPOA

- FPGA Reconfigurability
- ASIC-like Performance
- ASIC-Like Power
- Low Risk, Cycle Time Design
- Easy to Program
- COTS, RT, and RH Paths

Technology	Example Suppliers	Development Costs	Time to Market	Die Size	Performance	Time in System (reconfiguration)
ASIC	IBM, LSI , Leopard Logic	High	Slow	Low	High	Low
Reconfigurable	picoChip, Quicksilver PACT, Elixent,	Low	Medium	Medium	Low	High
FPGA	Xilinx. Altera	Low	Fast	High	Low	High
Gate Array	RapidChip (LSI), HardCopy (Altera), LightSpeed	Medium	Better than ASIC	Medium	Medium	Low
FPOA	MathStar	Low	Fast	Medium	High	High

Technical and programmatic advantages.

Payload Processing IR&D Vision and Objectives

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- Investigate and evaluate rapidly emerging/new reconfigurable, processing, and networking technologies
- Evaluate and develop technology for space
  - Focus on technology and capability, not commodities
  - End goal is initiate efforts to understand and integrate new technologies into overall payload system concept
- Develop and maintain engineering technical capability, expertise, and credibility
- Maintain Honeywell's ability to rapidly respond to customer interest and needs through demonstration of capabilities
  - Demonstrate our technical capability and credibility with our customers
- Offer best technology solution for specific mission needs
  - System will be Honeywell architecture
  - Processing engine may be non-Honeywell product
    - Will select best technology for the specific mission

2005 Honeywell Mathstar Sizing Study IRAD

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- **Select MAC Object for study**
  - **Most complex of all current FPOA Objects**
- **Mathstar and Honeywell re-targeted MAC Object to HX5000 Rad-hard process**
  - **Logic Growth**
    - Conversion of dynamic logic to static logic
    - RH cells larger
  - **Metallization Growth**
    - Migration from 9 layer metal to 6 layer metal
- **Goal: sizing and performance estimate**
  - **How many objects in RHFPOA?**
  - **How fast can we clock it?**
  - **Is it viable?**

RHFPOA Performance Estimates-
Image Processing and FFT applications

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	Commercial FPOA	RHFPOA
Device Size	400 SO	256 SO
Image Processing App (input data limited)		
Throughput	10 MS/s	10 MS/s
Clock Frequency	400 MHz.	185 MHz.
Cycle Utilization	21%	47%
SO Utilization	51%	80%
IRAM Utilization	25%	25%
XRAM B/W (100 MHz. DDR)	49%	49%
Total Performance	17.9 Gop/s	17.9 Gop/s
FFT 1024pt		
Clock Frequency	1000 MHz	185 MHz
Compute time	1 us	8 us

RhFPOA 185 MHz clock frequency is worst case, 370 MHz typical ~ 4 usec compute time for complex 1024 FFT

Important Benchmark Comparisons

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1024 Complex FFT Benchmarks

Processor	Clock Frequency	Compute Time
Commercial FPOA	1 GHz	1 usec
Virtex 5	400 MHz	2.5 usec
RT 750 PPC SBC	133 MHz	500 usec
RH Vector Processor DSP24	50 MHz	50 usec
RhFPOA	Worst Case 185 MHz	8 usec
RhFPOA	Typical 370 MHz	4 usec

Projected that RhFPOA performs up to 125x faster than other space qualified processors

FPOA IRAD 2006 Rice: Project overview

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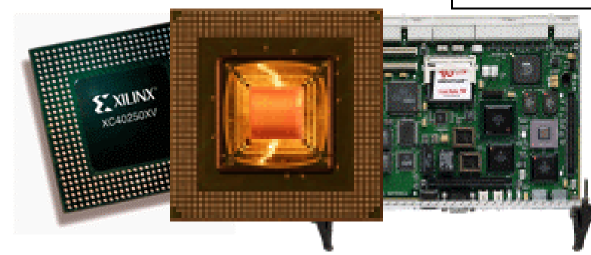
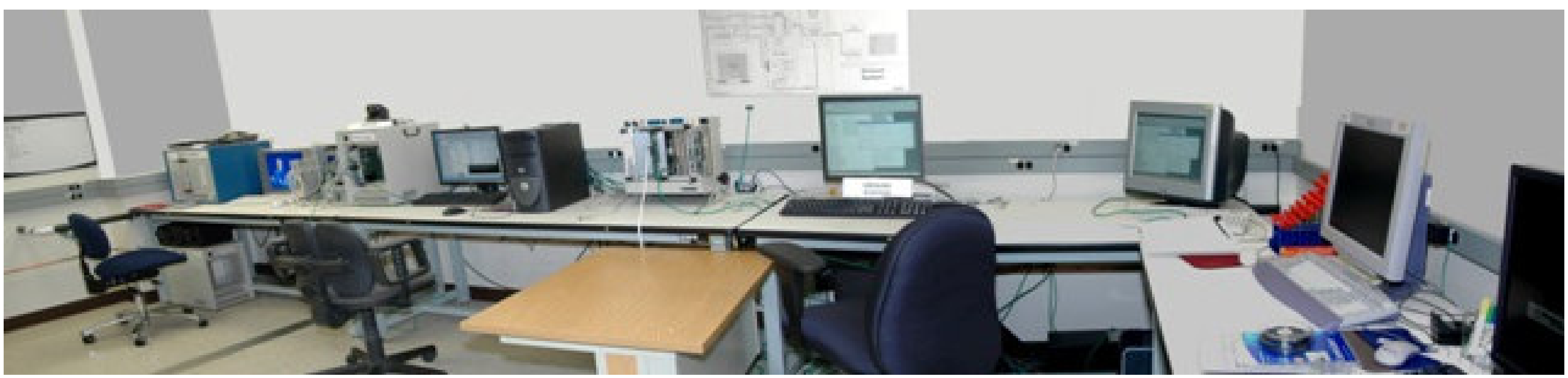


- Three technologies
  - FPGA – Fine grained
  - MathStar's FPOA – Medium grain
  - Microprocessor Array – Coarse grain
- A common basis across three different platforms
  - Display capabilities in three different technologies
  - Begin to form a common metric for cross-architecture benchmark
  - Solid examples on how the architectures differ and how they may be similar



FPOA RICE resource usage

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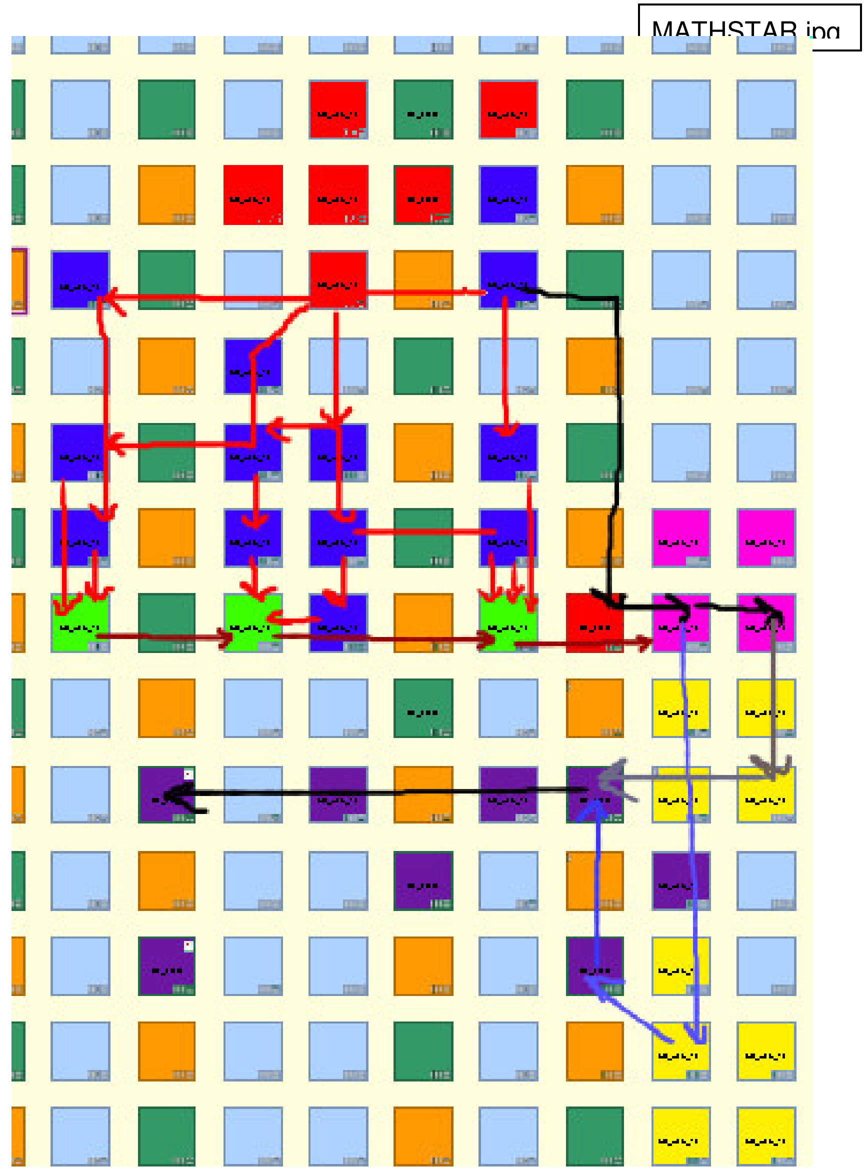
- **Red:** UDP
- **Blue:** Entropy Accumulators
- **Green:** Option Select
- **Magenta:** Bit split
- **Yellow:** FS/SB encoder
- **Purple:** CDS packetizer

- **Actual Resource usage**
  - 36 ALU's 18% utilization
  - 11 RFs 10% utilization



Project Results

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- **Rice core is capable of real-time video compression**
  - Requirement states >13.5Mpixel/s, actual compression rate =23MPixel/s
- **Target for 400Mhz core clock**
  - Design can be mapped at 1Ghz
  - 1Ghz imposes more stringent requirements than a 400Mhz mapping
- **Core validation**
  - Validated against a golden reference
  - Full circle validation
    - Simulator results ran through decoder and original image was retrieved

FPOA 2007- 2008 IR&D Plans

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- Software Defined Radio (SDR) algorithms/applications are being used to evaluate the latest processing architectures for Space applications.

- Key SDR algorithms noted…
  - Viterbi encoders/decoders
    - Rate ½, k=7
    - Rate ½, k=9
  - Reed-Solomon BCH encoders/decoders
    - CCSDS (The Consultative Committee for Space Data Systems) Waveform
      - (63,56) code
  - Turbo encoders/decoders
    - CCSDS Waveform
      - Information block length from k =1784 up to k = 16384
      - Rate ½, rate 1/3, rate ¼, rate 1/6
  - LDPC (Low Density Parity Checking) encoders/decoders
    - CCSDS Waveform
      - Shortened (8160, 7136) code
  - Full waveforms like Turbo-coded SOQPSK

FPOA 2007-2008 IR&D Plans

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- **Key Processing Architectures of interest**
  - **FPOA (Field Programmable Object Array) by MathStar**
    - "Revolutionary Processing Architecture"
    - Reconfigurable course grain processor that runs at 1 GHz
      - Moving to 1.2 GHz soon
      - Computes 1024 FFT in 512 ns
      - Up to 4x faster than any FPGA
      - Almost ASIC like speed
      - Programming at Object level, not Gate level
      - No timing closure, 1 GHz speed guaranteed
    - Commercial chips available today
  - **Achronix FPGA**
    - "Revolutionary Processing Architecture"
    - FPGA that runs at GHz speeds
      - Worst case performance matches other FPGAs
      - Patented pipelining architecture
      - Over 500+ algorithms/ cores available
      - Programming at Gate level, just like other FPGAs
      - Limited availability of test chips
      - Uses Industry Standard Design Tools
      - Asynchronous nature for reduced power

FPOA 2007-2008 IR&D Plans

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- Cell Processor
  - "Revolutionary processing architecture for multi-core processing"
  - Benchmarked Several Real Applications
    - Synthetic Aperture Radar (SAR)
    - Hyper-Spectral Imaging (HSI)
    - Rice Compression
  - Cell development environment in our labs

- ElementCXI
  - "Revolutionary processing architecture"
  - Coarse-Grain Reconfigurable
  - New technology of interest and active evaluation

- Tilera TILE64
  - "Revolutionary processing architecture"
  - Development environment in place
  - Active programs with Tilera baselined
  - Many-Core homogeneous processing architecture
  - Based on proven MIT RAW architecture

FPOA 2007-2008 IR&D Plans

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- **XILINX V5 FPGA**
  - **Not "revolutionary", but the Industry Standard**
  - **Speeds now pushing 500 MHz**
  - **SiRF (SEU Immune Reconfigurable FPGA) Program has AFRL backing and is making excellent progress**
    - Honeywell very much involved with this effort and supports it!
- **ACTEL FPGA**
  - **Competes with XILINX head-to-head**

- **Lots of "Revolutionary Technologies"- Need to understand which ones are best mapped to our various customers' needs.**

There is no silver bullet for every application!

University of Florida NSF / CHREC FPOA Preliminary Results Review

*Much more detail to be presented by UF at CHREC next week

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Benchmarks in Progress

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- **Complex Multiplication**
  - **A complex multiplier capable of handling streaming data**
    - 16-bit Real, 16-bit Imaginary
  - **This can form multiplication core for FFT/IFFT**
- **AltiVec results were gathered on MPC7447 testbed**
- **FPGA / FPOA results are based upon estimates from functional simulation**

	Time (ms)	Throughput (Mults/sec)	Speedup
Baseline PPC	2550.3	41	1
Altivec-Enabled	131.5	797	19.4
FPGA	349.5	300	7.3
FPOA	104.9	1000	24.3

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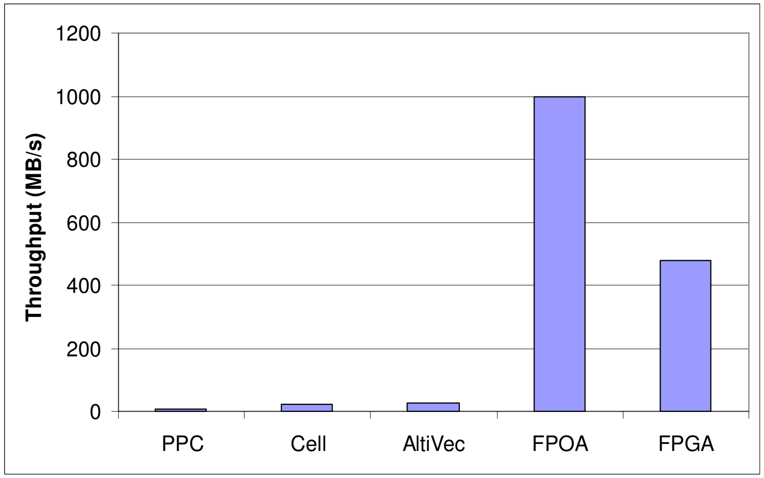
Device	Speedup
PPC	1
Cell	3.7
AltiVec	4.4
FPGA	80
FPOA	168

- **2D Convolution**
  - **Basic structure of convolution kernel is used in spatial filtering, edge detection, and other areas of image processing.**
  - **Scan a mask (the kernel) along an image generating a weighted sum for each pixel.**
- **Implemented on Cell, AltiVec, FPGA, and FPOA platforms with PPC baseline**
- **FPOA result is for streaming case; a limitation is image width (1,024 pixels)**



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FFT Implementation

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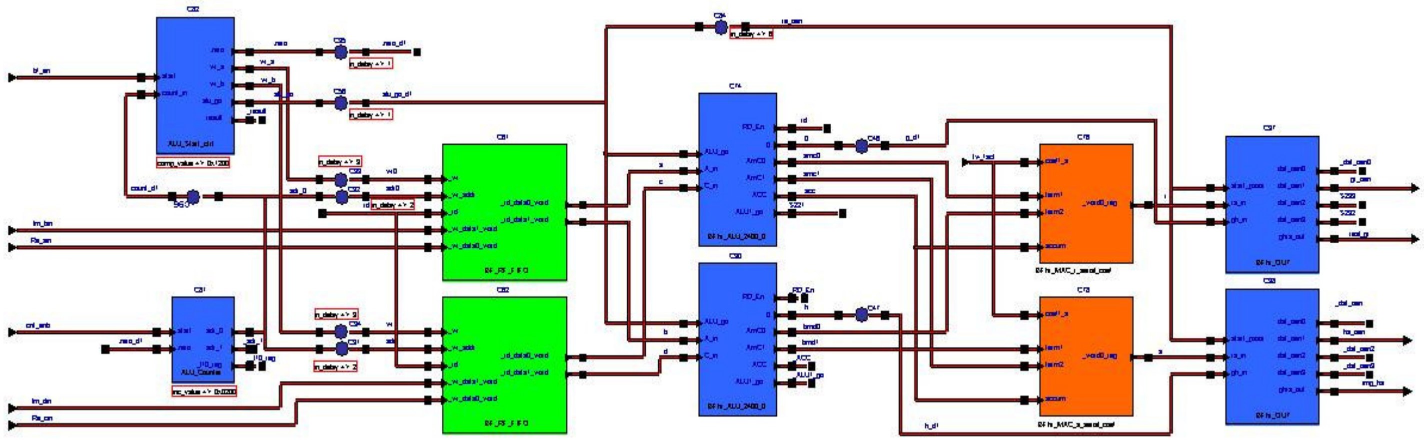
- Radix-2 DIF FFT
  - 32 point and 1024 point
- Basic Butterfly tile
  - 2 RFs, 6ALUs, 2 MACs
- Each butterfly has a throughput of 2 cycles per input pair sample



*Provided by Mathstar

Simulation Result

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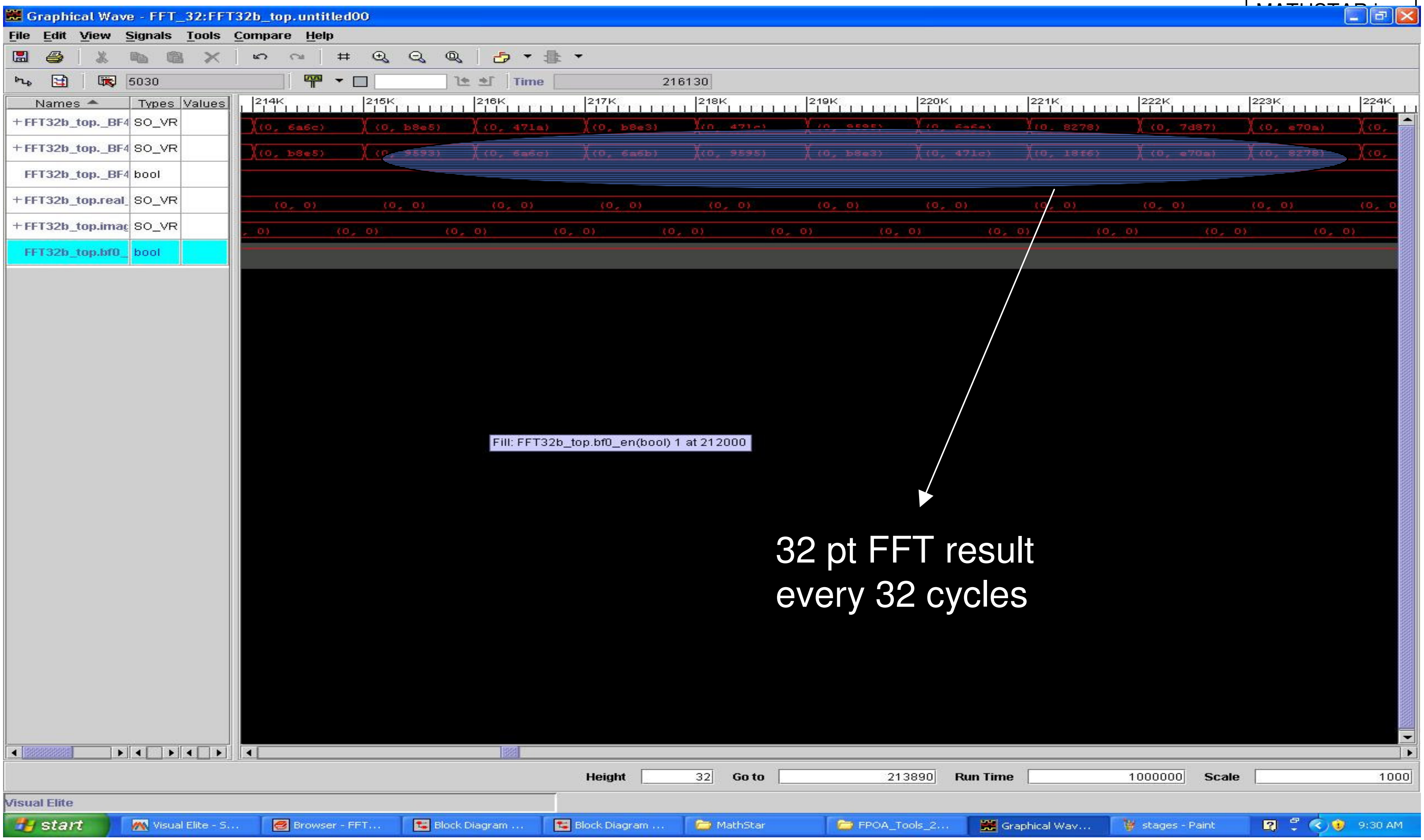

FPGA vs. FPOA (FFT cores)

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Device	MOA2400D	Virtex4LX100-12ff1148	MOA2400D	Viretx4LX100-12ff1148
FFT	32point	32point	1Kpoint	1Kpoint
Max F (MHz)	**1000.00**	**277.78**	**1000.00**	**281.06**
Latency (ns)	**160.00**	**588.70**	**10240.00**	**7777.40**
Throughput (MSamples/sec)	31.25	8.68	0.98	0.27
Speedup	3.60	1.00	3.62	1.00

*1Sample =1 32/1024 pt FFT

(yellow)	FPOA
(purple)	FPGA

CFAR Constant False Alarm Rate

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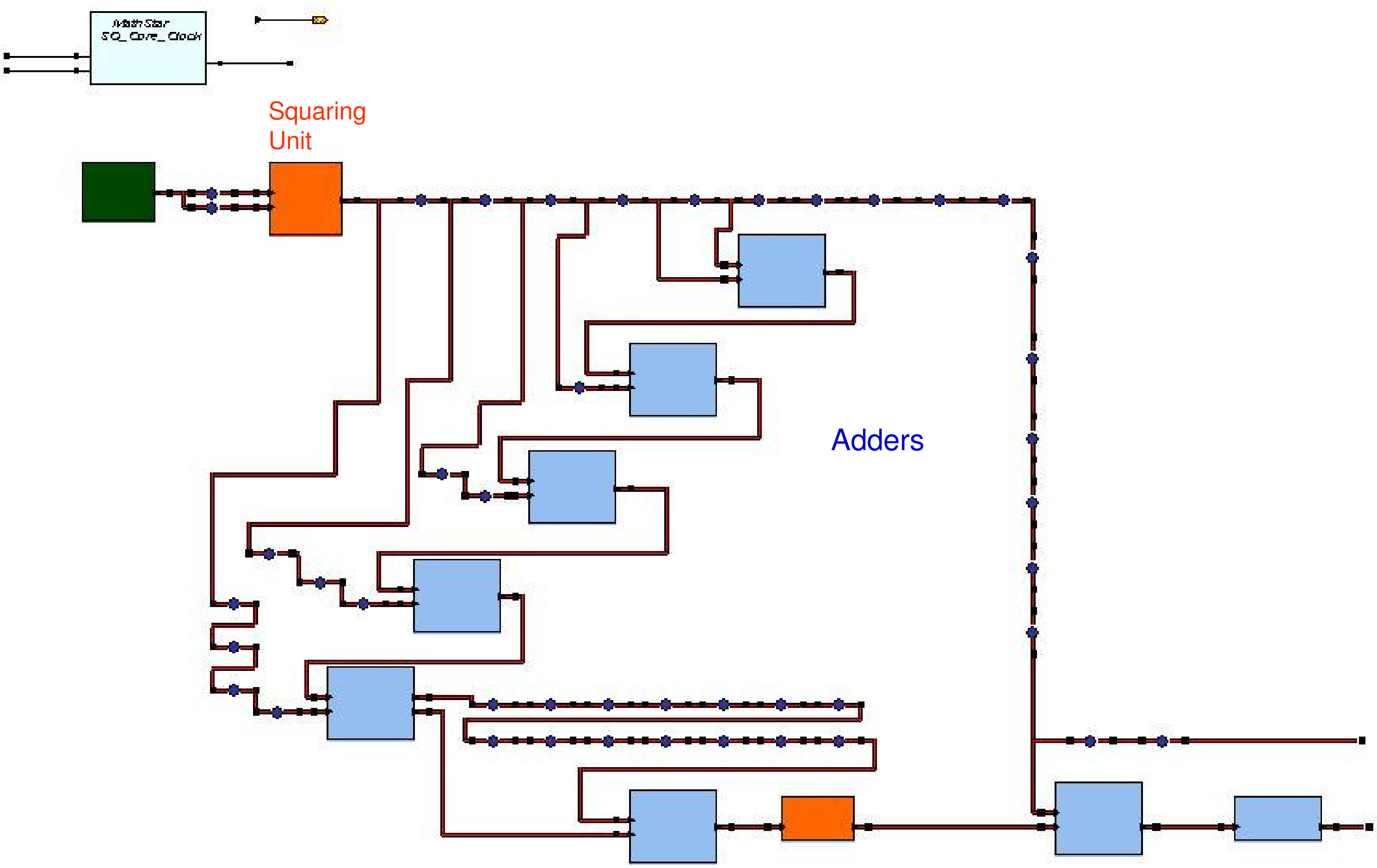

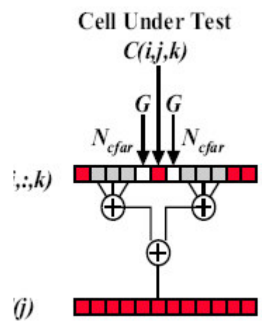

Mapped CFAR kernel

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Results

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- CFAR simulated, mapped and implemented on board
- Data set 0 (from HPEC challenge benchmark)
- 16 bit data (q15 format)
- Resource Utilization
  - 8 ALUs
  - 2 MACs
  - 3 IRAMS
  - Can fit upto 4 CFAR cores on this FPOA (limited by IRAMs)
- Latency-21ns
- Throughput : 2Gsamples/s (2 cores operating on 2 streams➔ IO throughput –32Gbps)
- CFAR Code Development Time
  - Xilinx FPGA ~ 8 Weeks
  - MathStar FPOA ~ 2 Weeks

Summary

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- MathStar FPOA Enjoying Commercial Success
- Independent Benchmarks Demonstrating FPOA Performance Superiority
  - Increased processing speed by 4X
  - 1 GHz FPOA FFT realizes ~ 50 GOPS
    - ~2.5 GOPS/Watt performance
  - 600 MHz FPOA FFT realizes ~ 30 GOPS
    - ~3.5 GOPS/Watt performance
  - Reduced development time by 4X
- Honeywell & MathStar investing in Rad-Hard FPOA Technology for Space Applications

Thank You!

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