A Comparative Study of Field Programmable Gate Array Error Cross Sections: Putting Data into Perspective

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Sponsors:

- *NASA Electronic Parts and Packaging (NEPP) Program and*
- Defense Threat Reduction Agency under IACRO# 06-4012I

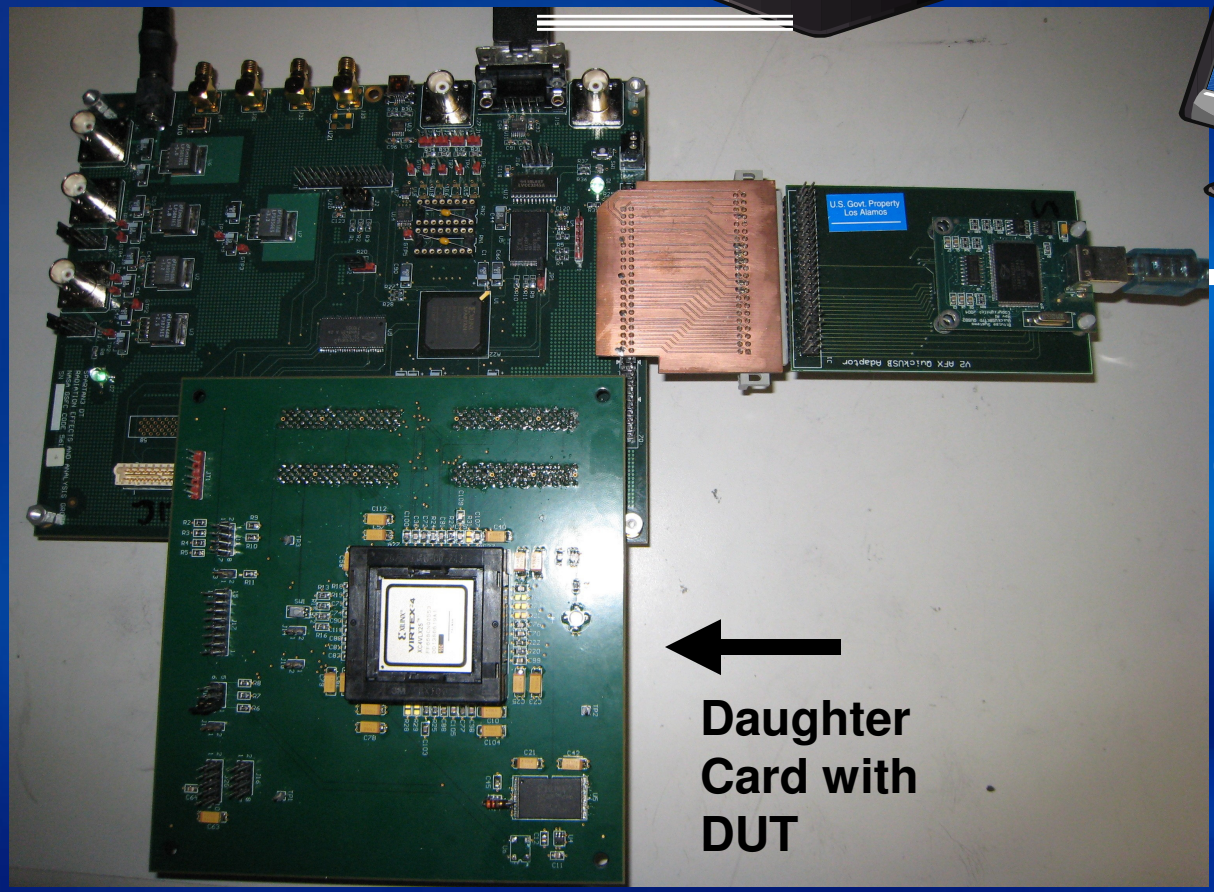
Outline

- Radiation Effects and Analysis Group (REAG) Low Cost Digital Tester
- Differentiating FPGAs
- Radiation Test Development
  - Antifuse FPGA Testing and Results
  - SRAM FPGA Testing and Results
- Expanding Evaluation Criteria
  - Limitations of Bit Error Rate Calculators
  - SET Performance Degradation Metric
  - Availability Calculation

NASA-GSFC Low Cost Digital Tester (LCDT)

RS232
CONNECTION

LCDT Board

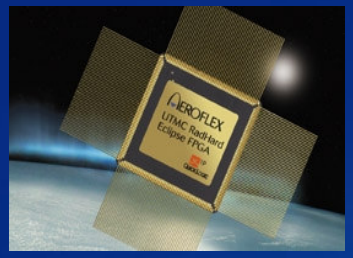


Daughter
Card with
DUT

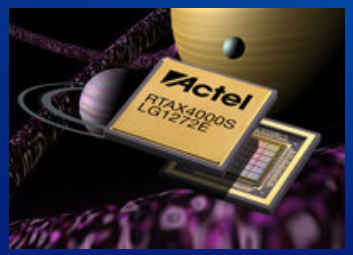
HIGH-SPEED
USB
CONNECTION

Just Some of Our Success Stories

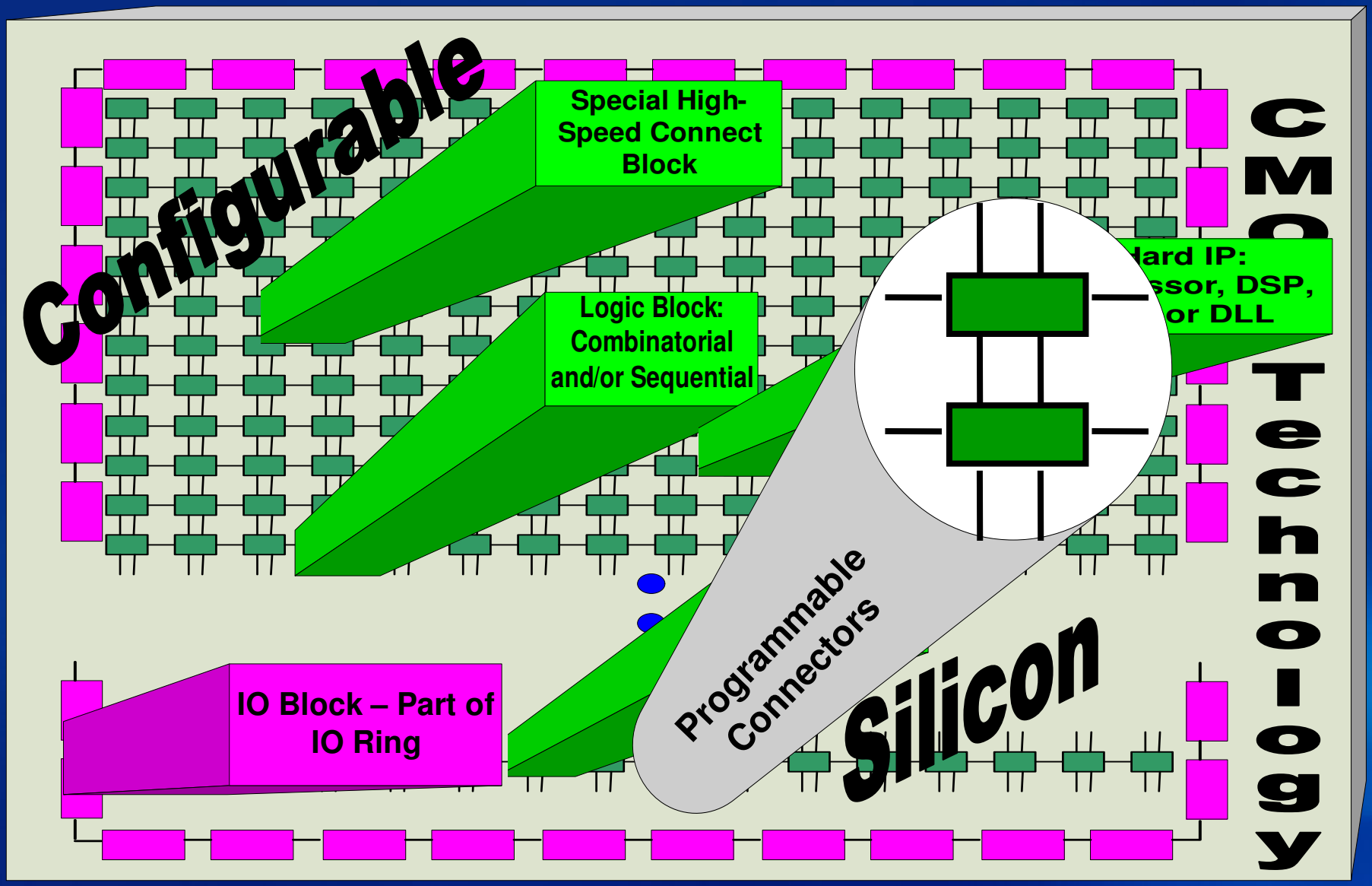
- Maxwell SDRAM
- Actel RTSX & RTAX
- SRAM & SDRAM (for NSWC Crane)
- DRAM (for NRL)
- LSI Arithmetic Logic Unit
- Micron and Samsung Flash Devices
- Aeroflex Eclipse
- Boeing HBD Test Chip
- Xilinx SPARTAN III
- Xilinx Virtex 4 (LX and FX)
- Samsung and MICRON 1G High-Speed DDR2 SDRAM
- TI ADC



FPGA Characterization: Understanding the Differences to Develop an Efficient Test Suite



General FPGA Architecture



Configuration: A Major Difference between FPGA Classes

- FPGAs contain groups of preexisting logic
- Configuration:
  - Arrangement of pre-existing logic
  - Defines Functionality
  - Defines Connectivity
- Common types
  - One time configurable
  - Re-configurable

CONFIGURATION TYPES

One Time Configurable → Antifuse

Re-Configurable → SRAM - Based

Re-Configurable → FLASH - Based

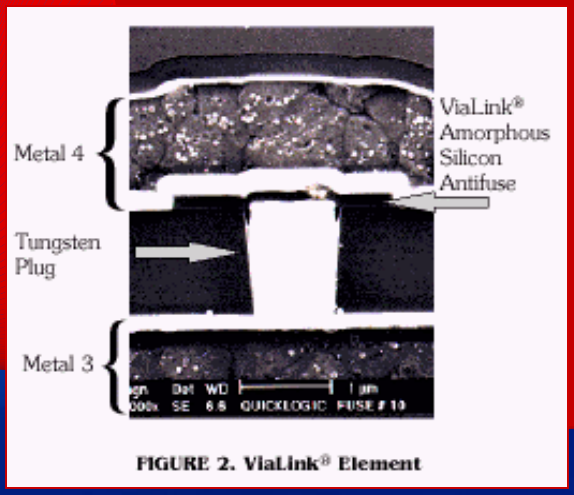
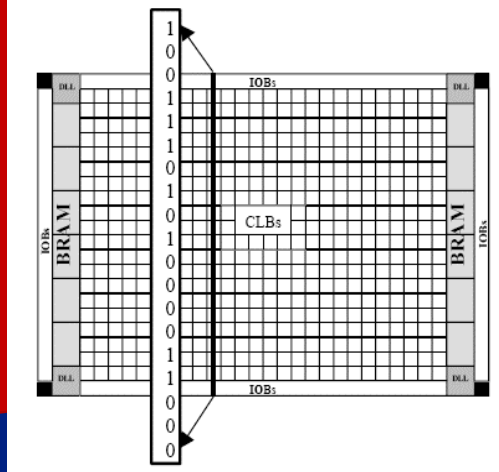


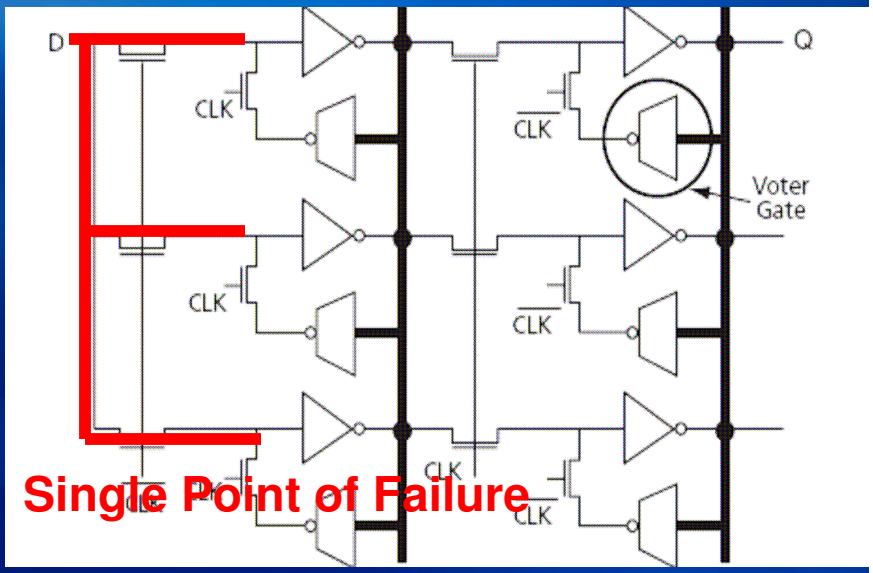
FIGURE 2. ViaLink® Element



Antifuse FPGA Devices (Actel and Aeroflex)

- Pros:
  - Most common FPGA devices utilized for space missions - heritage
  - Configuration is fused (no transistors) and is thus "HARDEND" – not affected by SEUs
  - Logic has embedded mitigation at each DFF (either TMR or DICE) – eases the design phase
- Cons:
  - One time programmable – can complicate the design/debug phase
  - Very expensive

RCELL in hardened Actel devices



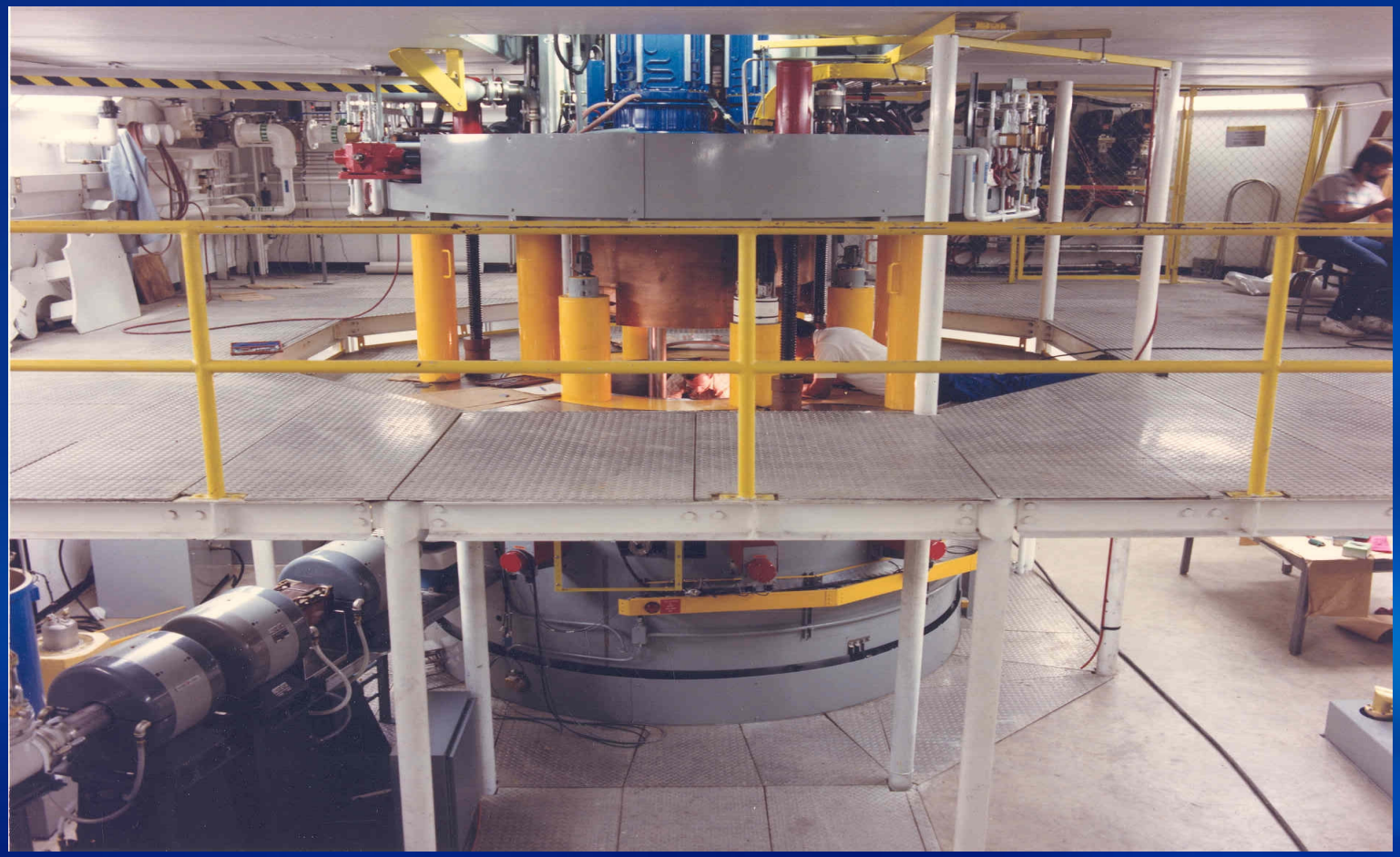
SRAM Based FPGAs (Xilinx)

- Reconfigurable – configuration is stored in internal SRAM.
- Configuration is soft (sensitive to SEUs and MBUs)
- Logic is also sensitive and contains no embedded mitigation
  - Based on radiation test data and project requirements, the mission will decide what level of mitigation to implement
  - Mitigation logic must be added by the designer

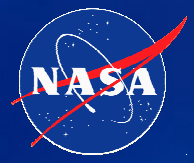
Why Use SRAM-Based FPGA's?

- **Pros**:
  - The ability to reconfigure a function while in-flight is of great advantage to many missions
  - Device is Less expensive
  - Easier to debug/correct (with no mitigation)
  - Performance:
    - Speed
    - Increased User Device Resources
- **Cons:**
  - Configuration is SRAM-based – increased sensitivity to radiation (vs. antifuse)
  - Additional design complexity necessary for mitigation
  - Additional hardware necessary for (re)configuration

Radiation Testing

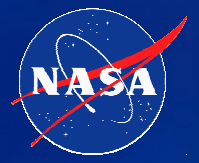


Goal: Investigate Radiation Effects and Fault Analysis



- Determine Bit sensitivity
  - Flip Flops
  - Configuration (SRAM based technology)
- Availability analysis
  - Given a function to implement – what is the percentage of time the output is correct vs. incorrect
  - Determine an availability rating that considers
    - Operational Frequency
    - Fluence
    - Repair time
    - Burst time

What Function to Implement for Testing?



Simple Architecture

- No functional Masking
- Easy to base-line across FPGAs
- Reduces Test time
- increases state space coverage

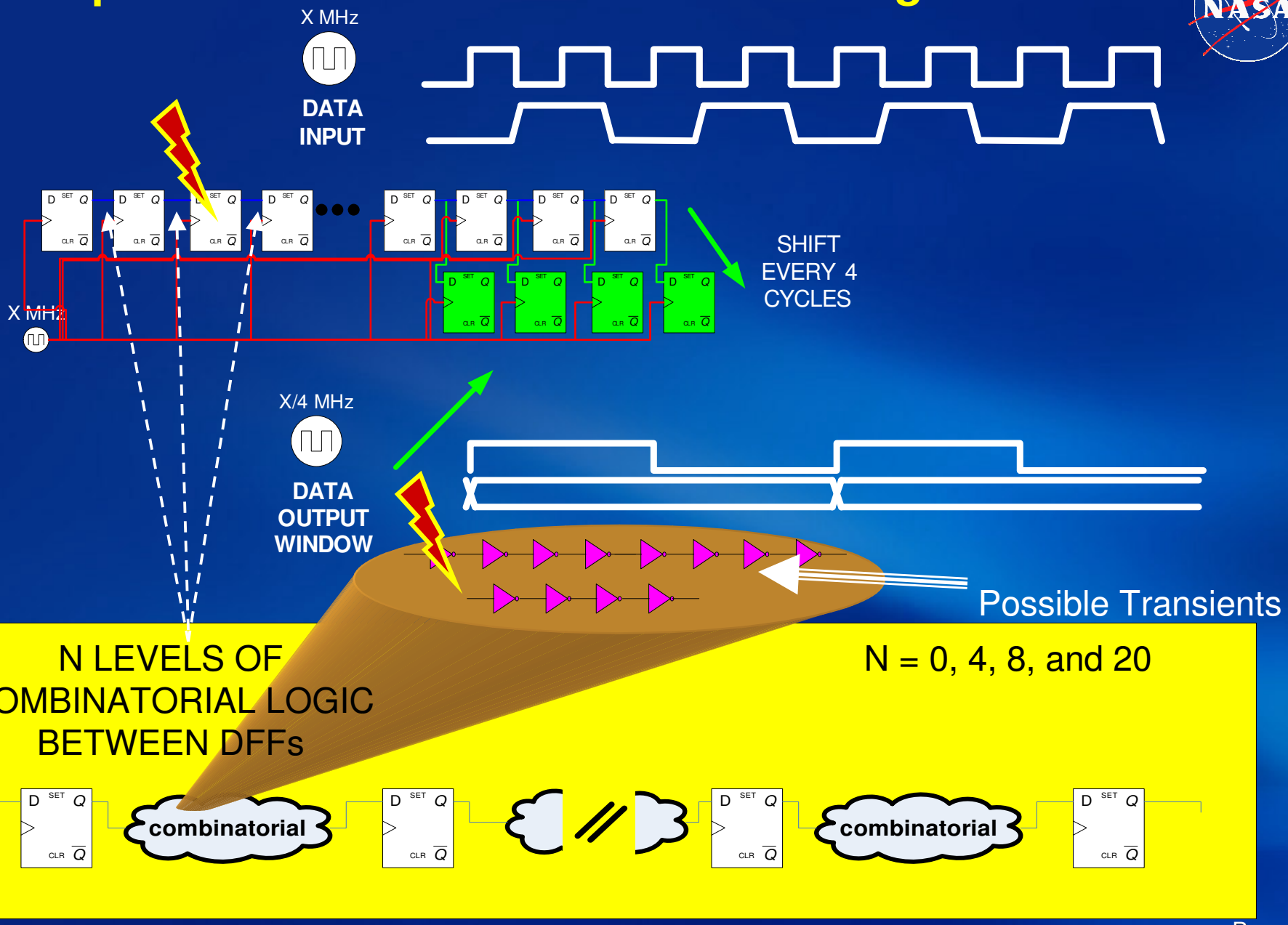
Complex Architecture

- Functional Masking
- Minimal state space coverage (short test runs – reset upon error)
- Only significant for specific design

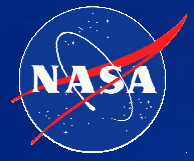
Actual flight Architecture

- Usually not available at test time
- Can be very expensive to test
- Can not cover a significant amount of state space while testing
- Usually have to start from scratch at every error event

Simple Architecture: Windowed Shift Register



Testing Anti-fuse Devices



- No extra mitigation is required during testing *(most space missions do not add mitigation to antifuse implementations)*
- Check for frequency dependency
  - Test across a wide range of frequencies: varying combinatorial logic chains assists in analysis
  - Push design…Static Timing Analysis – 10% critical path margin
- Analyze data pattern effects
  - Static vs. dynamic
  - Switching rate
  - Value
- Monitor fuse reliability
- Monitor potential latch-up
- Monitor potential speed degradation
- Tester must capture data every cycle:
  - have the ability to determine bursts
  - Time stamp every error

Calculating Error Cross Sections

Traditional error calculation

$$\sum \frac{Events}{Fluence}$$

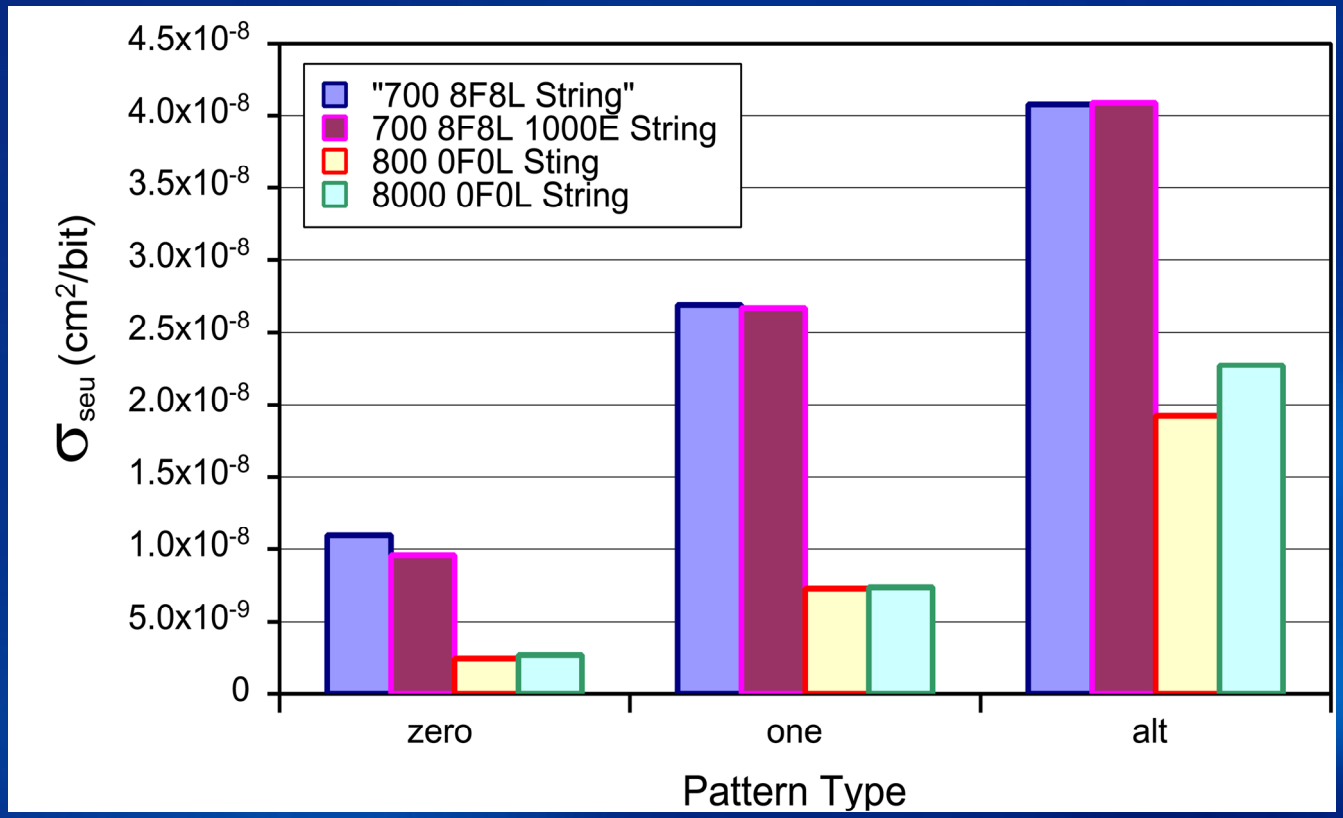
- TF: Total Effective Fluence
- TB: Time in Burst
- Flux: particles/second

Error calculation: Bursts within data

$$\frac{\sum Events}{TF - (TB * FLUX)}$$

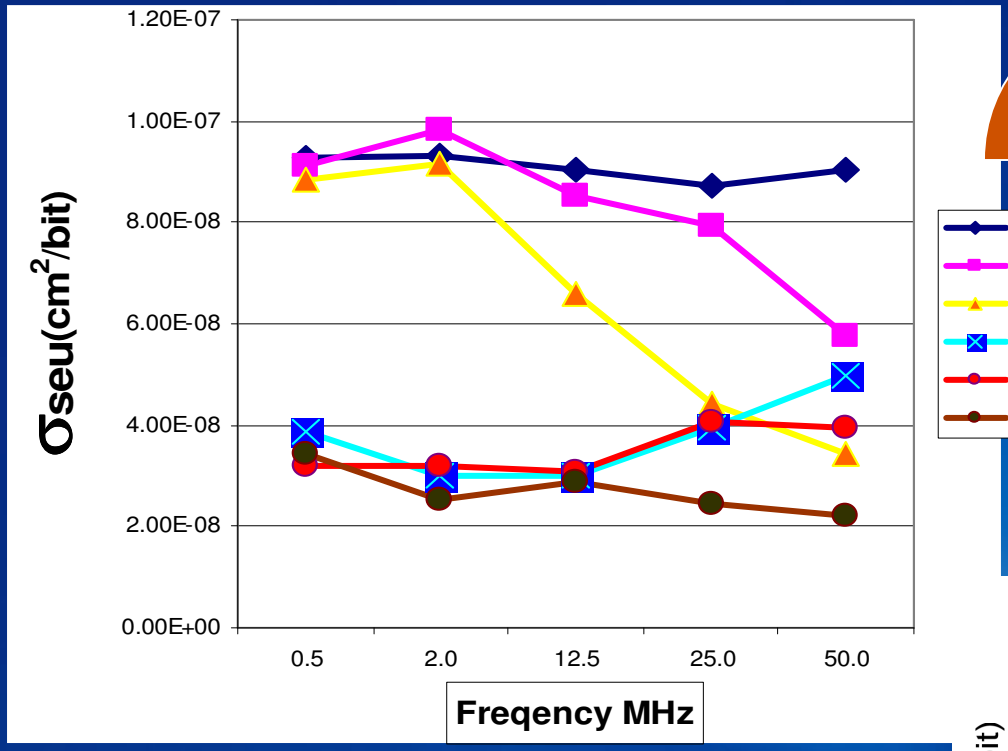
- **Analysis of event frequency**
- **cross-section fed to error rate calculator: based off of a cumulative distribution probability function (P(T>t))**
- **We are not analyzing how long we are in error**

Data Pattern Effects: Actel @ 150MHz



- 700 8F8L: 700 DFFs with 8 inverters (8L)
- 800 0F0L: 800 DFFs with 0 inverters
- 8000 0F0L: 8000 DFFs with 0 inverters

Clock Frequency Effects 54MeV*cm²/mg:



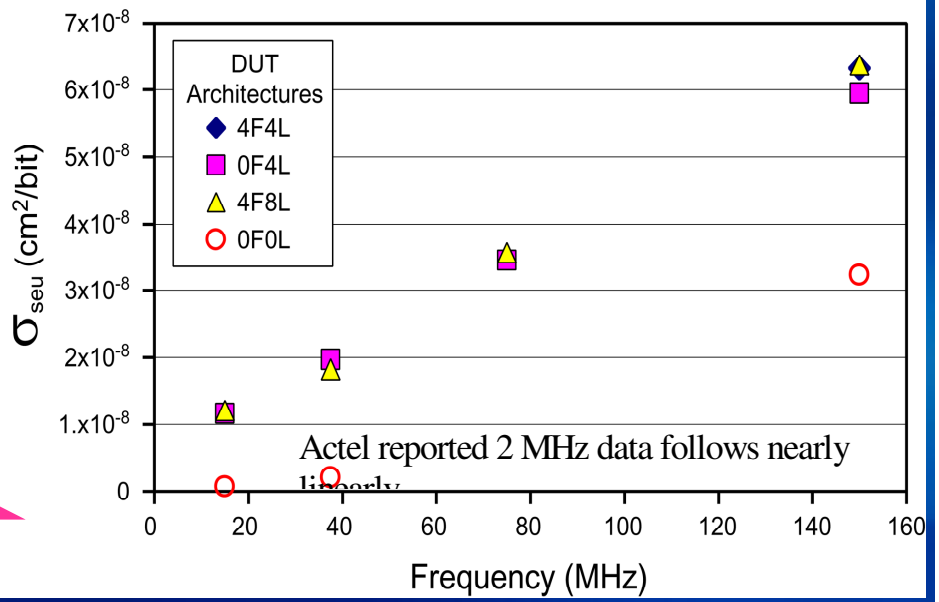
Aeroflex:

σ decreases as Frequency increases

Most significant with larger chains of combinatorial logic and data pattern fluctuation

Actel:

σ decreases as Frequency decreases



Error Cross-Section Results Prove for Antifuse Devices…

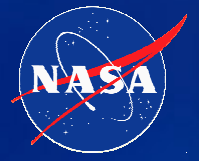
- Static testing is not sufficient
- Static simulation is not sufficient
- Assumptions of frequency response can not automatically be made
  - Actel produced expected (traditional) response
  - Aeroflex – unexpected… combinatorial logic acts as transient filter

REAG Testing of Xilinx SRAM-Based FPGAs.

Xilinx Radiation Testing: Goals

- Analysis of user implemented mitigation strategies:
  - Evaluate cross sections with and without scrubbing
    - External Scrubbing
    - Internal – self scrubbing
  - Evaluate cross sections with and without XTMR
- Monitor frequency Effects
- Monitor Data Pattern Effects
- Error Cross Section Calculations
- Determine function Availability

Scrubbing Facts



- Scrubbing is a form of error correction for Configuration memory
- Scrubbing does not reduce the probability of an upset occurring
- Scrubbing can reduce the amount of time the upset is present in the configuration memory
- The system is fully operational.
- Unable to scrub everything

REAG Investigation of Scrubbing:

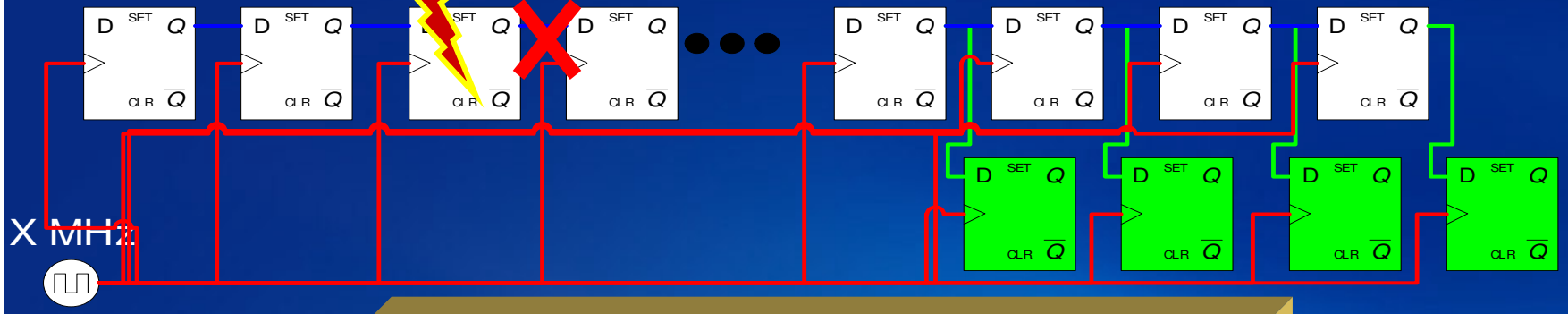
- **No scrubbing – scrub machine is turned off**
- **Internal Scrubbing (Xilinx proprietary)**
  - Instantiate Xilinx Cores
  - Core has ability to write and read configuration memory
- **REAG External Scrubbing**
  - Utilizes SelectMap Interface: 30 MHz 8bit parallel mode
  - Requires alternate devices
    - Tester + memory in our case
    - Hardened FPGA + memory within a mission
  - Writes Frame independent of error states (does not require read-back)
  - Tester uses readback for analysis purposes (via separate USB interface)

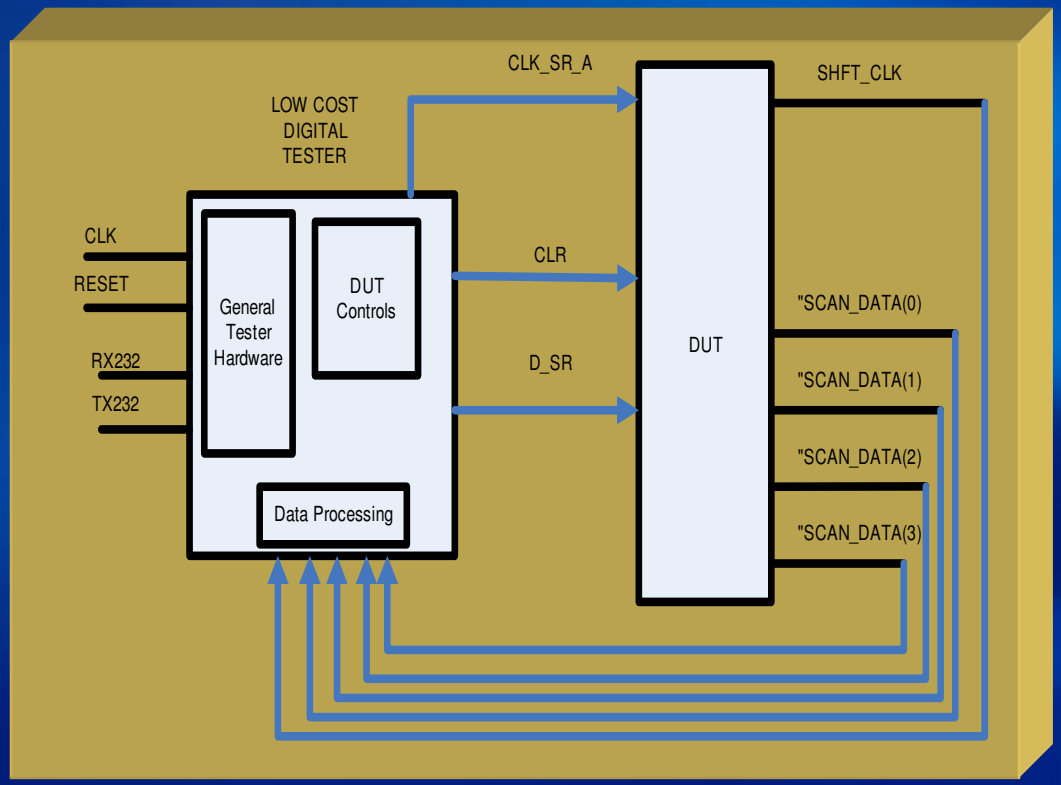
2 Architectures

- 6 strings of windowed shift registers
  - 2 strings @ N=0
  - 2 strings @ N=8
  - 2 strings @ N=20
  - Implemented with 300 and 80 DFF length strings
- TMR'd version of 6 windowed shift registers
  - Each string containing 80 DFFs
  - Could not implement triplicated version of 300 DFFs in Xilinx V4-LX25

Non-TMR Windowed Architecture

N levels of logic between DFFS … 2 strings each; N = 0, 8, and 20



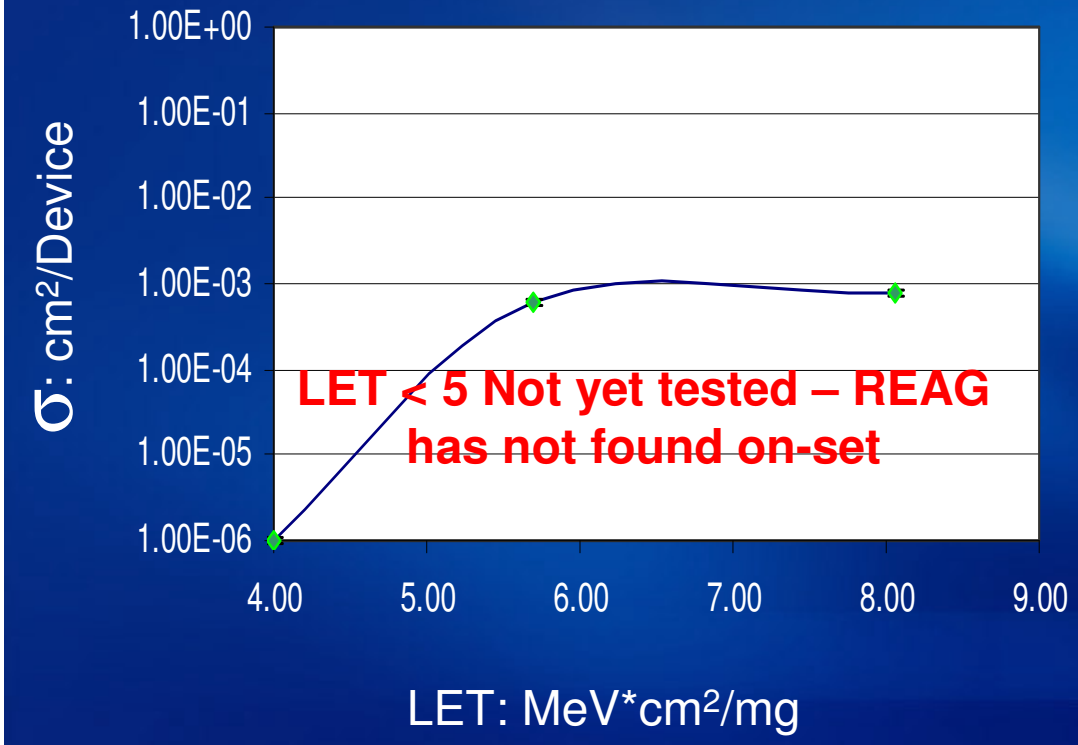


Long string of '0's or '1's:

We use alternating data inputs to achieve accurate cross-sections

Error Cross Section Calculation: Dealing with Bursts

$$\sigma \cong \frac{NE}{TFL - (TB * FLUX)}$$



- Cross-section based off of functional upsets (shift register)
- Count burst as one error event
- Burst can potentially mask faults
  - could have a much higher frequency of events
  - just masked by burst
  - Will be further investigated by fault injection

Limitations with Error Cross Sections as sole Evaluation Criteria

- Frequency Effect Analysis and Successful Operations per second:

DUTA:@100MHz over 1E07 fluence: no bursts 10 errors

DUTB:@ 50MHz over 1E07 fluence: no bursts 5 errors

$\sigma A = 2^* \sigma B$; Assumes constant error rate per frequency

Common Interpretation: Cross Section increases with Frequency – Decrease Clock Rate for Critical Missions

- However, B has to run twice as long as A to complete the same number of successful operations.
- Illustrates that per number of completed operations, each has the same probability to accumulate an equivalent number of errors

In this case:Slower Clock does not influence errors per successful operation

Limitations with Error Cross Sections as sole Evaluation Criteria (Continued)

- Burst Analysis:
  - Cross section probability calculation is based off of Event frequency (not event duration).
  - Cross section does not consider burst or repair time (availability)

Bit Error Rate Misconceptions:

- Given a Bit Error rate of 5e-08, what does this mean???

- **AntiFuse**
  - **Bit Error Rate is based on DFFs**
  - **Number of DFFs will be from a few hundred to 10's of thousands**
  - **Comes out to about 1 error every 10,000 days or better**

- **SRAM**
  - **Generally pertains to configuration bit rate**
  - **If for example 1e7 bits can affect the design upon upset – then can have 1 upset every 2 days**

SET Performance Degradation Metric:

Performance Degradation per NMOPS = C* Percentage of Downtime

- Can be used to compare functional performance across FPGA manufacturers
- Includes bursts/repair time (ECi)

Normalization Constant

Percentage of downtime

$$\approx \frac{N_{MOPS}}{fk} * \frac{1.0}{Acc} * \left(\sum_{i=1}^{n} \frac{ECi}{TotCyc}\right)$$

- NMOPS: Number of Millions of operations per second
- F*k: operational frequency * number of operations per cycle
- EC*i*: Number of clock cycles of error per event i
- TotCyc: Total number of operational clock cycles during irradiation
- Acc: Acceleration Factor

Performance Degradation per 100MOPS: 8 LET MeV*cm^2/mg

	F*K	ECi/TotCyc	Degradation
RTAX	150MHz*2000	$1.2*10^{-9}$	$(1.0/AccR)*4.0*10^{-13}$
Aeroflex	100MHz*140	$8.77e^{-11}$	$(1.0/AccA)*6.0*10^{-13}$
Xilinx	100MHz*1800	$1.2e^{-3}$	$(1.0/AccX)*6.0*10^{-7}$

Degradation Measurement: We want the number to be low

$$AccR \approx AccA \approx 10^4 AccX$$

Conservative : See Ed Peterson 1998 TNS

Availability

$$A = \frac{MTTF}{MTTR + MTTF}$$

A = 1 is a perfect system

A: Steady State Availability

LET = 8MeV*cm2/mg	MTTR	MTTF	A steady State
RTAX @150MHz	$6.67*10^{-9}$	$3.6*10^{6}$*AccR	$(3.6*10^{6}$*AccR)/ ($6.67*10^{-9}$ + $3.6*10^{6}$*AccR)
Aeroflex @ 100MHz	10^{-8}	$6.0*10^{5}$*AccA	$(6.0*10^{5}$*AccA)/ (10^{-8} + $6.0*10^{5}$*AccA)
Xilinx @ 100MHz	$1.6*10^{-2}$	41*AccX	(41*AccX)/ ($1.6*10^{-2}$ + 41*AccX)

Mission Device Selection

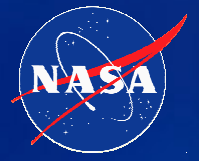
- Xilinx showed a relatively low availability rating at 100MHz.
  - If used at full rate, may achieve much higher operations per second.
  - Higher MOPS can include scheduled downtime and may be a great fit
- Criticality and reliability play a major role in device selection
  - Missions have traditionally chosen antifuse devices for critical specifications.
    - Actel has been in the forefront
    - Aeroflex is very promising with its combinatorial transient filitering.
  - For less critical functionality, SRAM devices are being heavily investigated

Summary

- Differences between FPGA types strongly influence test beds
- Sensitivity calculations must be provided to missions to assist in the selection process.
  - Test to determine additional mitigation schemes required per FPGA
  - Bit Error calculations
  - Availability and degradation analysis
- Formulae have been presented:
  - Adjust Bit error calculations due to long bursts
  - SET Performance degradation Metric
  - Availability
- FPGA will be chosen by mission based on mission specifications:
  - Reliability
  - Availability
  - Cost
  - Successful Operations per second

Summary (Continued)

- Example was provided: Testing the SRAM-Based Xilinx Device
  - SRAM-Based Device will need some level of configuration memory error correction
  - Error correction categorization
    - Partial reconfiguration
    - Scrubbing
  - REAG compared 3 modes of scrubbing
    - No scrubbing
    - Internal scrubbing
    - External scrubbing
  - Test Results proved external scrubbing has the best performance
  - Information can be misleading…Further investigation must be taken on reporting analysis data.



Thank You ….
Questions?