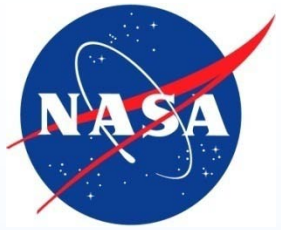
NEPP Electronic Technology Workshop
June 22-24, 2010

National Aeronautics
and Space Administration



Packaging And Embedded Electronics For The Next Generation

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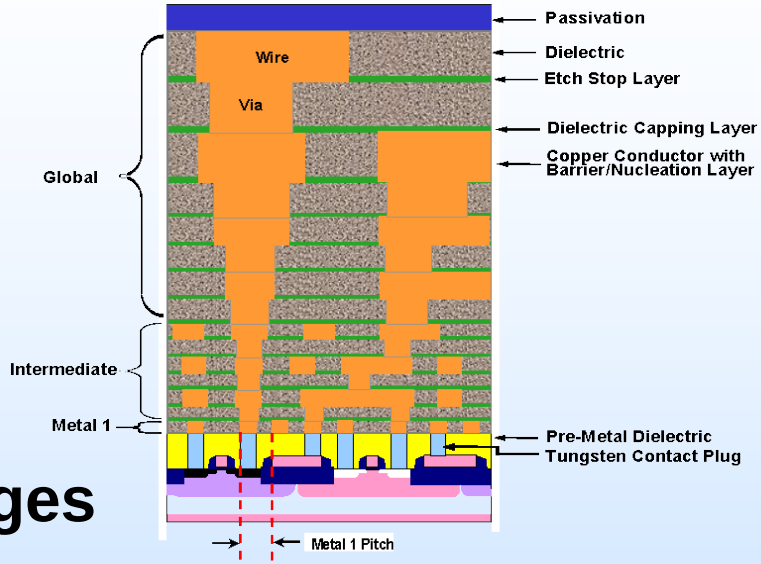
Outline

- What is Electronic Packaging?
- Why Package Electronic Parts?
- Evolution of Packaging
- General Packaging Discussion
- Advanced non–hermetic packages
- Discussion of Hermeticity
- The Class Y Concept and Possible Extensions
- Embedded Technologies
- NEPP Activities

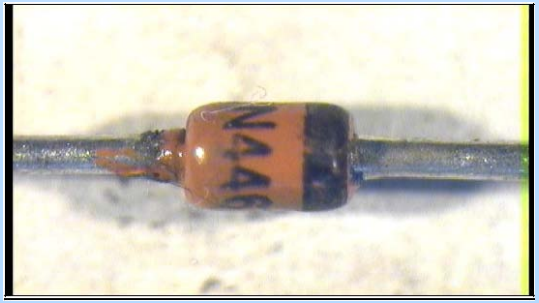


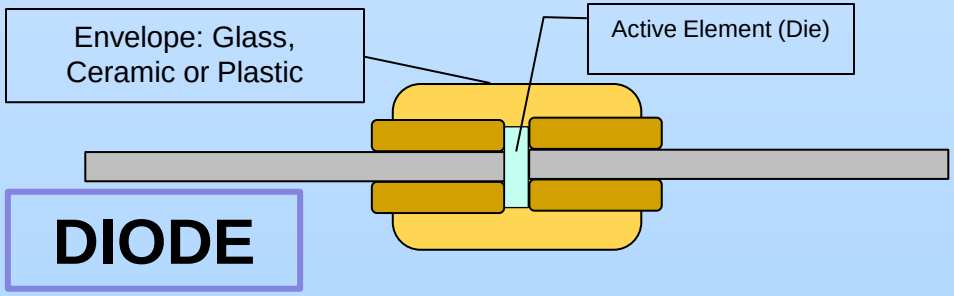
What is Electronic Packaging?

- It is not cardboard boxes and bubble wrap
- Electronic “Packaging” can have two basic meanings:
  - First (Part) Level: The “envelope” of protection surrounding an active electronic element, and also the termination system to connect it to the outside world
  - Second and Higher Levels: The assembly of parts to boards, boards to slices, slices to boxes, boxes to systems, instruments and spacecraft
- This discussion will cover examples of both

Why Package Electronic Parts?

- To protect the active element against:
  - Handling
  - Shock and vibration
  - Contamination
  - Light penetration or emission
- To provide a suitable system to make connection between the element and the printed wiring board
- To prevent conductive parts of the element from coming in contact with other conductive surfaces, unless intended





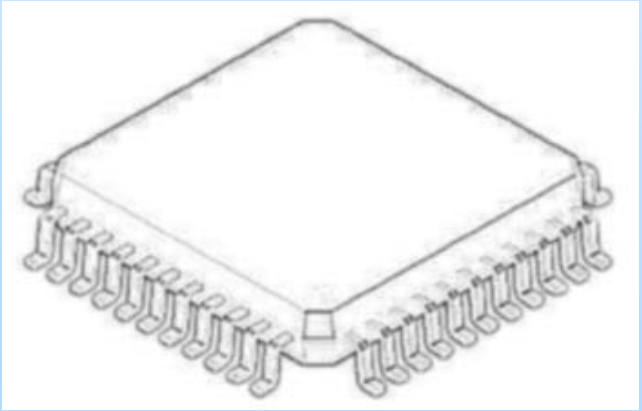
Package Options – Hermetic?

- Once, hermetic packages were the preferred option
- Now, few hermetic options for latest package technologies
  - Development of new hermetic options unattractive
    - Very high Non Recurring Expenses
    - Very high technical difficulty
    - Very low volume
    - Demanding customers
- Market is driven by consumer products
  - Low cost
  - High volume
  - Rapid turnover
  - "Green"
  - Minimized size

= Non hermetic, mostly plastic

The “General” Package

- **Typically, packages consist of the same basic features but achieve them in many ways:**
  - **Functional elements - active die, passives etc.**
  - **Interconnects between elements (2 or more elements)**
  - **A substrate**
  - **Interconnects to the external I/O of the package**
  - **A protective package**
  - **Interconnects to the next higher level of assembly**

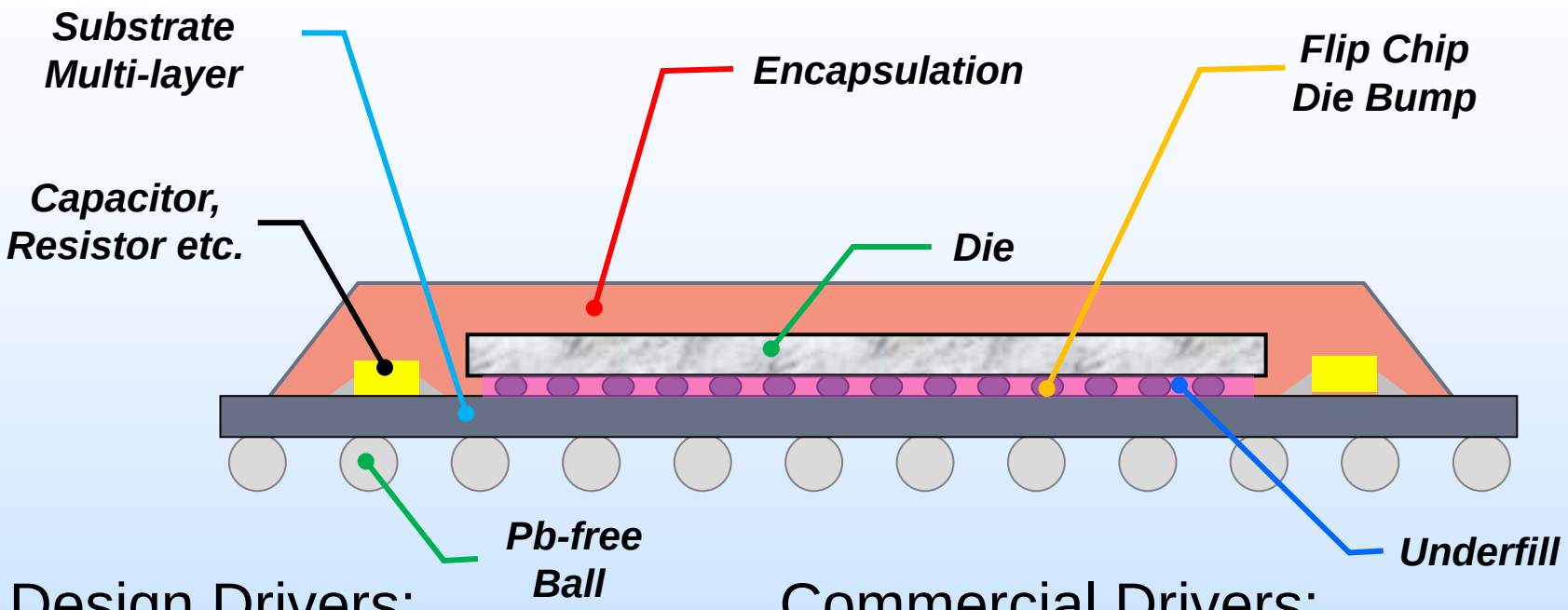


Continuous Packaging Challenges

- I/O s, increasing number, decreasing pitch
- Heat Dissipation, (especially in space)
- Manufacturability
- Materials
- Mechanical
- Installation
- Testability
- Inspectability
- RoHS (Pb-free)
- (Space Environment)

–*Lunar Reconnaissance Orbiter (LRO), Built at GSFC, Launched with LCROSS, June 18,2009*

Commercial, Non-hermetic Package (PBGA)



Design Drivers:

- High I/O count
- Large die
- Environmental protection
- Performance/Speed
- Ancillary parts

Commercial Drivers:

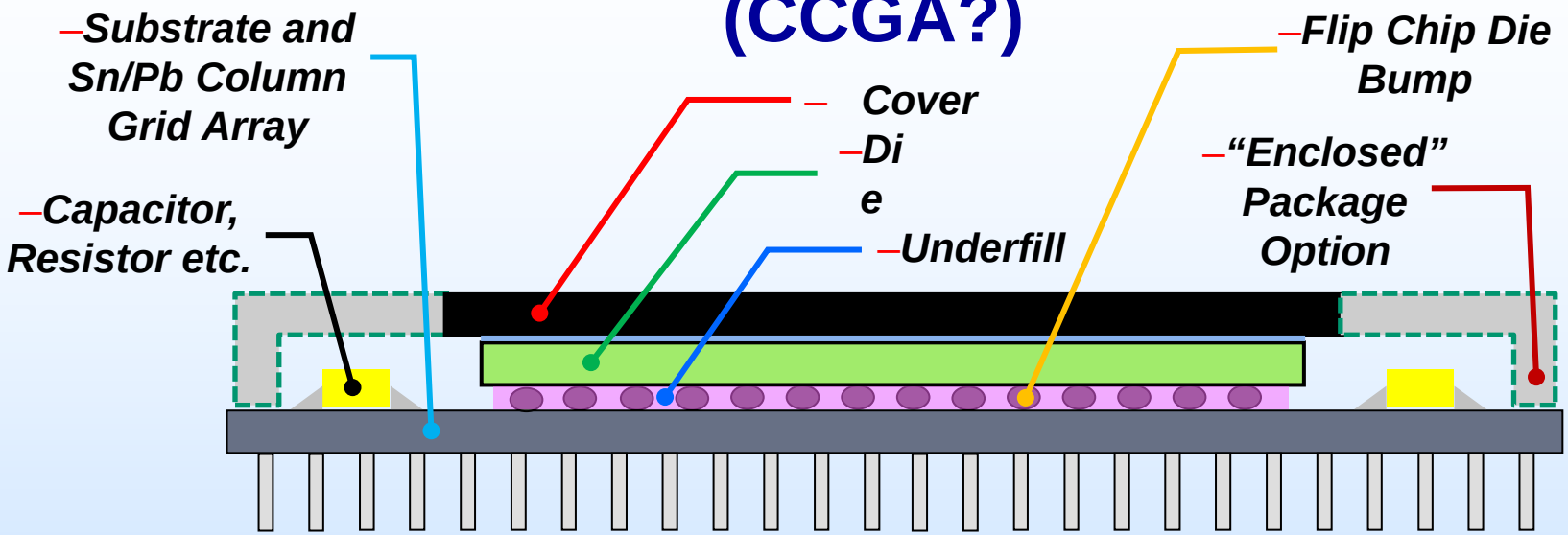
- Low cost
- High volume
- Limited life
- Automated installation
- Compact

Space Challenges for Complex Non-hermetic Packages

- **Vacuum:**
  - Outgassing, offgassing, property deterioration
- **Foreign Object Debris (FOD)**
  - From the package threat to the system, or a threat to the package
- **Shock and vibration**
  - During launch, deployments and operation
- **Thermal cycl**ing
  - Usually small range; high number of cycles in Low Earth Orbit (LEO)
- **Thermal management**
  - Only conduction and radiation transfer heat
- **Thousands of interconnects**
  - Opportunities for opens, intermittent - possibly latent
- **Low volume assembly**
  - Limited automation, lots of rework
- **Long life**
  - Costs for space are high, make the most of the investment
- **Novel hardware**
  - Lots of “one offs”
- **Rigorous test and inspection**
  - To try to find the latent threats to reliability

ONE STRIKE AND YOU’RE OUT!

Non-hermetic Package, With"Space" Features (CCGA?)



Space Challenge	Some Defenses
Vacuum	Low out/off-gassing materials. Ceramics vs polymers.
Shock and vibration	Compliant / robust interconnects - wire bonds, solder balls, columns, conductive polymer
Thermal cycling	Compliant/robust interconnects, matched thermal expansion coefficients
Thermal management	Heat spreader in the lid and/or substrate, thermally conductive materials
Thousands of interconnects	Process control, planarity, solderability, substrate design
Low volume assembly	Remains a challenge
Long life	Good design, materials, parts and process control
Novel hardware	Test, test, test
Rigorous test and inspection	Testability and inspectability will always be challenges

Hermeticity

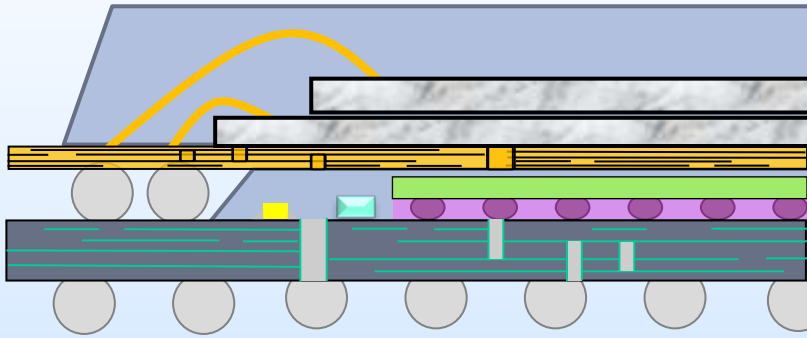
- **NASA prefers hermetic packages for critical applications**
- **Hermeticity is measureable, assuring package integrity**
- **Only 3 tests provide assurance for hermetic package integrity:**
  - **Hermeticity – nothing bad can get in**
  - **Residual or Internal gas analysis – nothing bad is inside**
  - **Particle Impact Noise Detection – no FOD inside**
- **NON-HERMETIC PACKAGE INTEGRITY IS HARD TO ASSESS - NO 3 BASIC TESTS**
- **Non-hermetic packages expose materials' interfaces that are locked away in hermetic ones**

But What is Hermetic?

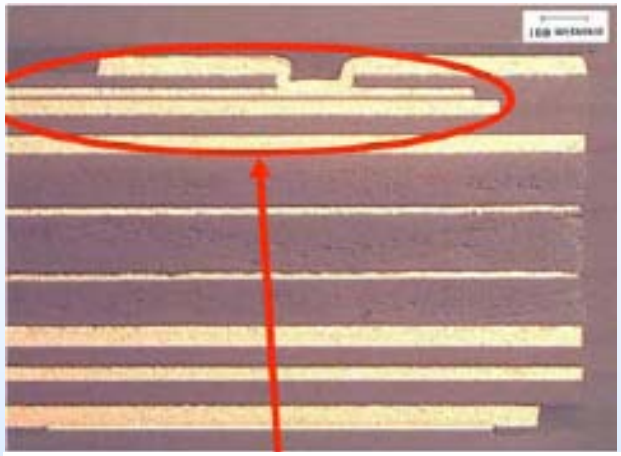
- **Per MIL-PRF-38534 Appx E and 38535 Appx A, hermetic packages must consist of metals, ceramic and glass in combinations ONLY, no polymerics**
- **Meets aggressive leak rate test limits**
  - **Verifies low rate of gas escape/ atmospheric interchange**
  - **Even so, small volume packages meeting "tight limits" theoretically exchange their atmosphere very quickly:**
    - **0.001 cc, exchanges 93% in 1 month at $5X10^{-8}$ atmosphere/cc/sec!**
    - **1.0cc, 96% in 10 years at $1 X 10^{-8}$**
  - **Even large packages with quite small leaks can surprise**
    - **10 cc, 96% in 1 year at $1 X 10^{-6}$!**
- **For applications in space vacuum why care?**
  - **Risk for contamination on the ground**
  - **Risk for outgassing in vacuum**

Non-hermetic Package Variations

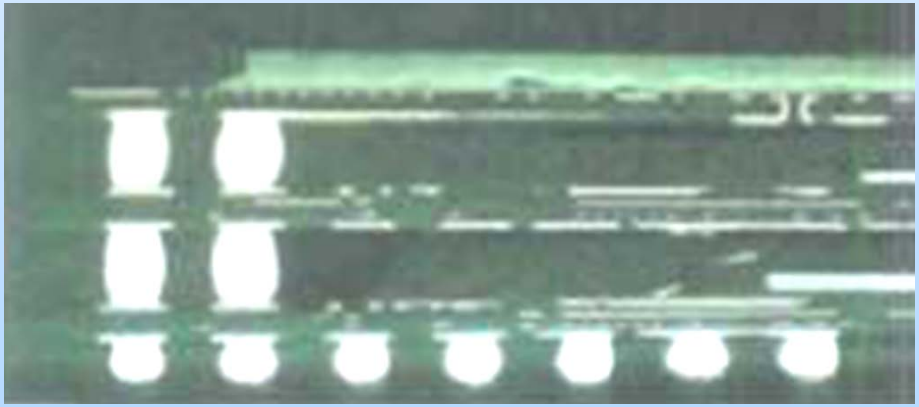
- **Current and future package options mix and match elements in almost infinite combinations**
- **Elements include:**
  - **Wire bonds**
  - **Ball interconnects**
  - **Solder joints**
  - **Conductive epoxies**
  - **Vias**
  - **Multi-layer substrates**
  - **Multiple chips, active and passive (hybrid?)**
  - **Stacking of components**
  - **Embedded actives and passives**
  - **Polymers**
  - **Ceramics**
  - **Enclosures/encapsulants**
  - **Thermal control features**

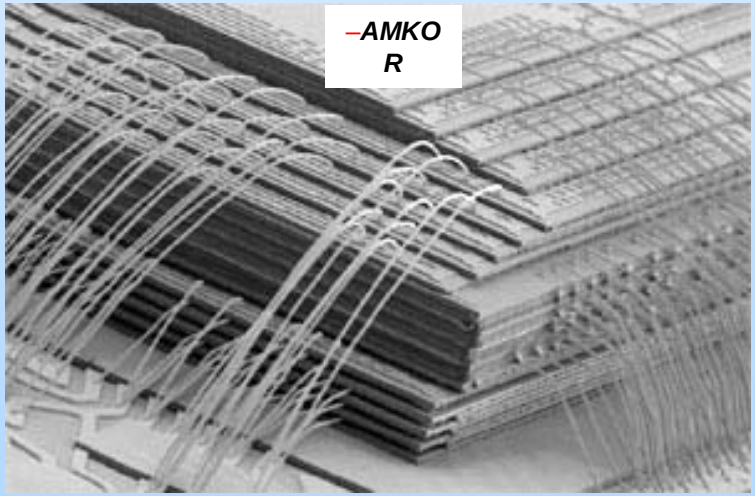


Some Large Device Package Options



Embedded Capacitor





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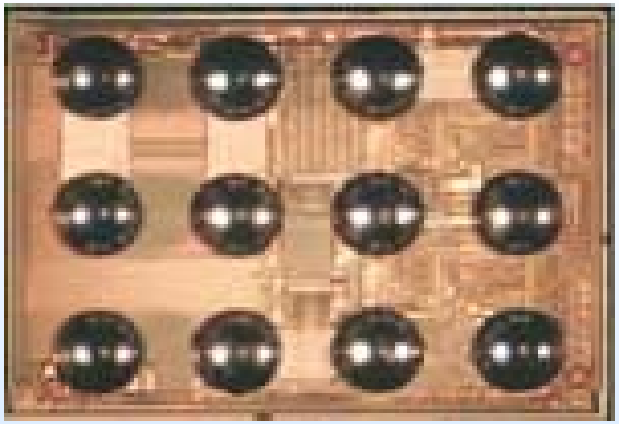
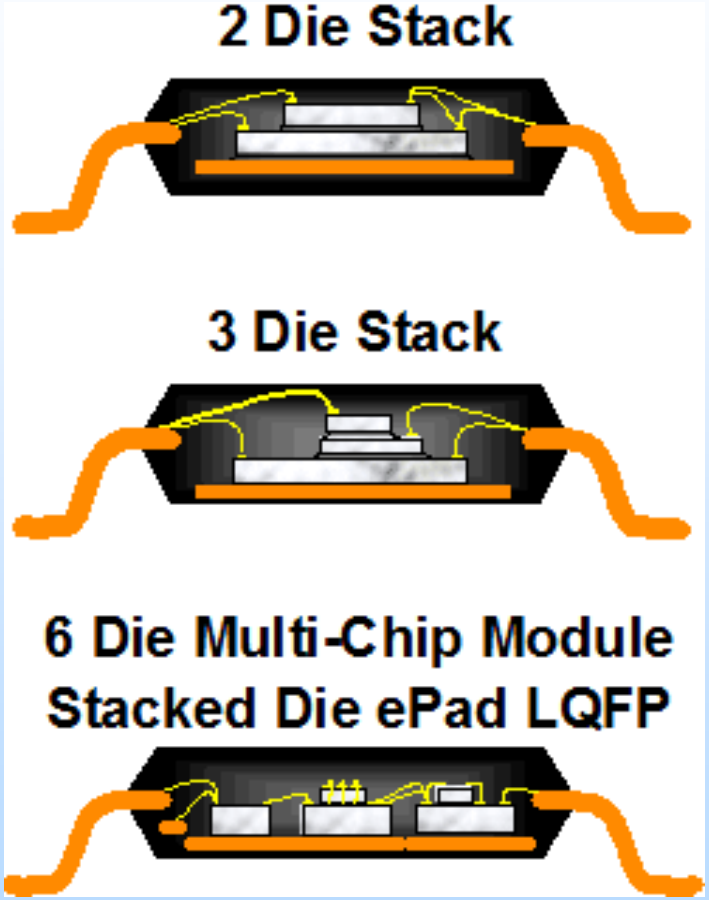




From Amkor's Website http://www.amkor.com/go/packaging

More Complexity is Coming

- **Stacking of chips to provide a third dimension of density and complexity**
  - **Stacking of Field Programmable Gate Arrays (FPGAs) appears imminent**
  - **Stacking of memory die is “old hat”**
  - **Through-silicon vias instead of bond wires**
    - **Maintain speed and allow lots of I/Os**
    - **High volumetric efficiency**
  - **Significant manufacturability challenges**
    - **Material and dimensional interfaces**
    - **Testability**
  - **Significant usability challenges**
    - **Design complexity**
    - **Handling, testing, rework/replace, risk management**
    - **Cost versus benefit trades**

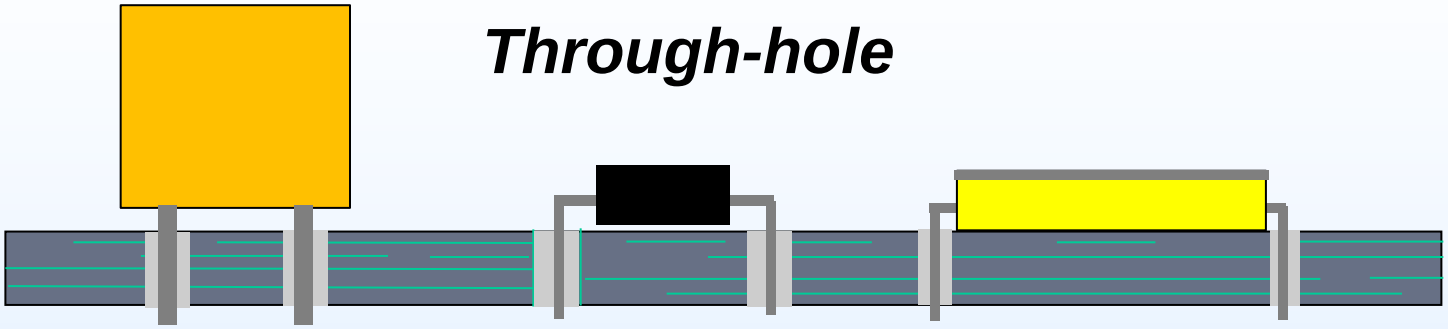
MIL-PRF-38535, Class Y

- **Y Not Non-hermetic for Space?**
- **Proposed new class for M38535, monolithic microcircuits**
- **Class Y will be for Space level non-hermetic**
- **Class V will be defined as hermetic only**
- **Addition to Appendix B, "Space Application"**
- **Package-specific "package integrity" test requirements proposed by manufacturer, approved by DSCC and government space**
- **The Package Integrity Test Plan must address:**
  - **Potential materials degradation**
  - **Interconnect reliability**
  - **Thermal management**
  - **Resistance to processing stresses**
  - **Thermo-mechanical stresses**
- **G12 Task Group established 01/13/01**

Level 2 Packaging Evolution

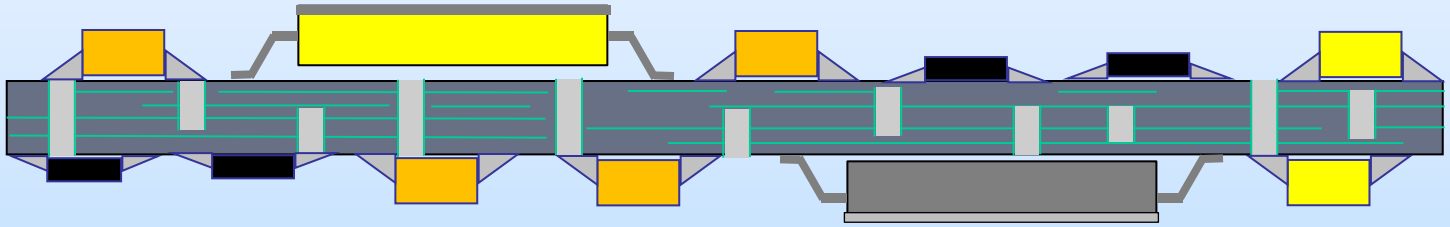
Increasing Density

Through-hole



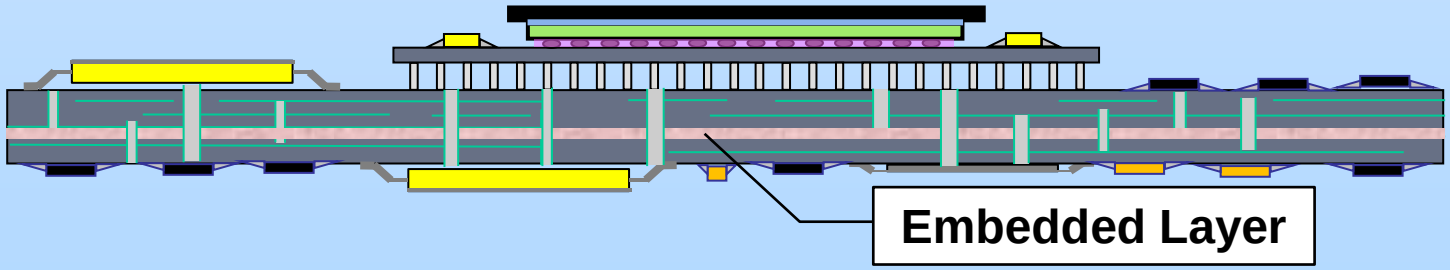
1950's

Surface Mount



1980's

Surface Mount with Embedded C or R Layer



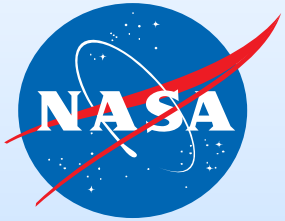
1990's

Embedded Technologies + and -

- **Advantages:**
  - Increases volumetric efficiency – reduces parts count on Printed Wiring Board (PWB) surface
  - Enhances performance – speed
  - Increases reliability (reduces number of solder joints)
  - Distributes heat more evenly
  - Aids high volume production and reduces cost
- **Challenges:**
  - Design/layout – introduces constraints, complicates re-spin
  - PWB quality – more difficult PWB fabrication
  - PWB robustness – material mismatches
  - Testing – can't access individual parts
  - Rework and repair – problems buried inside PWB
  - "One-offs"

NEPP Activities

- Continuous surveillance of emerging trends
- Have evaluated embedded passives
  - Partnering with Navy Crane
  - Quite mature technologies, bulk capacitive layer
  - Works but “space” low quantities a challenge
- Have tried to evaluate a novel, flexible, embedded active-die technology
  - Considerable promise
  - Beset by technical problems, particularly die thinning
  - Consider revisiting as technology improves
- Initial evaluations of technical readiness of die thinning, through-hole vias and advance die stacking are needed
- Continue development of Class Y concept



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To be presented at the 1st NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop June 22-24, 2010, NASA GSFC, Greenbelt, MD.