Memory Overview – Technologies and Needs

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Abstract

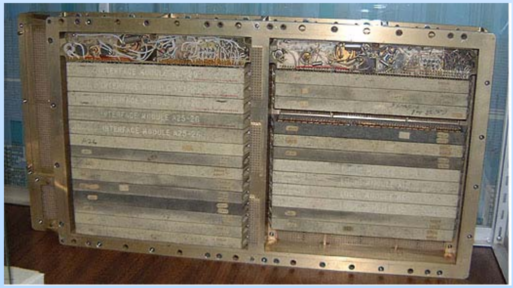
- As NASA has evolved it's usage of spaceflight computing, memory applications have followed as well. In this talk, we will discuss the history of NASA's memories from magnetic core and tape recorders to current semiconductor approaches. We will briefly describe current functional memory usage in NASA space systems followed by a description of potential radiation-induced failure modes along with considerations for reliable system design.

Outline of Presentation

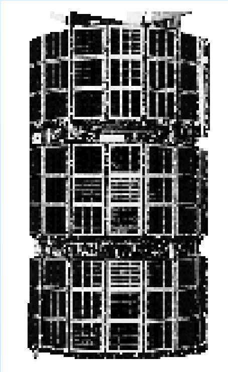
- Introduction – The Space Memory Story
  - A look at how we got here
- General Applications of Memories in Space Systems
- Requirements and Desirements
- Example: SDRAMs
  - Radiation Failure Modes – Single Events
  - Design Approaches
- Reliability Considerations
- Summary

Once upon a time…

- There once was a fledgling memory used for space
  - It started out as core memory (60's-70's)
  - Grew into magnetic tape (70's-80's)
  - And has settled into "silicon" solid state recorders or SSRs (90's and beyond)
    - *While this is true for mass data storage, silicon has been used since the 70's for some memory applications such as computer programs and data buffers*
    - *Both volatile and non-volatile memories (NVMs) are used*



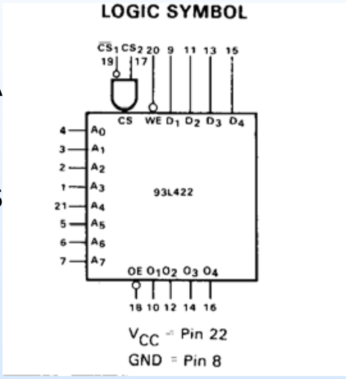
Apollo Guidance Computer
- 4 kB of Magnetic core r/w memory



P87-2 circa 1990
- 1st known spaceflight SSR

Sample Single Event Upset (SEU) hiccups along the way

- **An original space SEU detector, the 93L422 – bit errors in space**
  - **TDRS-1 anomalies, for example**
    - **“Solved” by use of error detection and correction (EDA codes**
    - **Used as “gold standard” on multiple flight experiments (CRRES and MPTB)**



- **Single event functional interrupts – SEFIs**
  - **Device has a functional anomaly**
- **Stuck bits**
- **Multi-bit/multi-cell upsets**
- **Block errors**
- **Small probability events**
  - **Proton ground test of 3 samples**
  - **Flight SSR had > 1000**
  - **Anomaly in-flight traced to low-probability event**

Categories of Memory Usage for Space

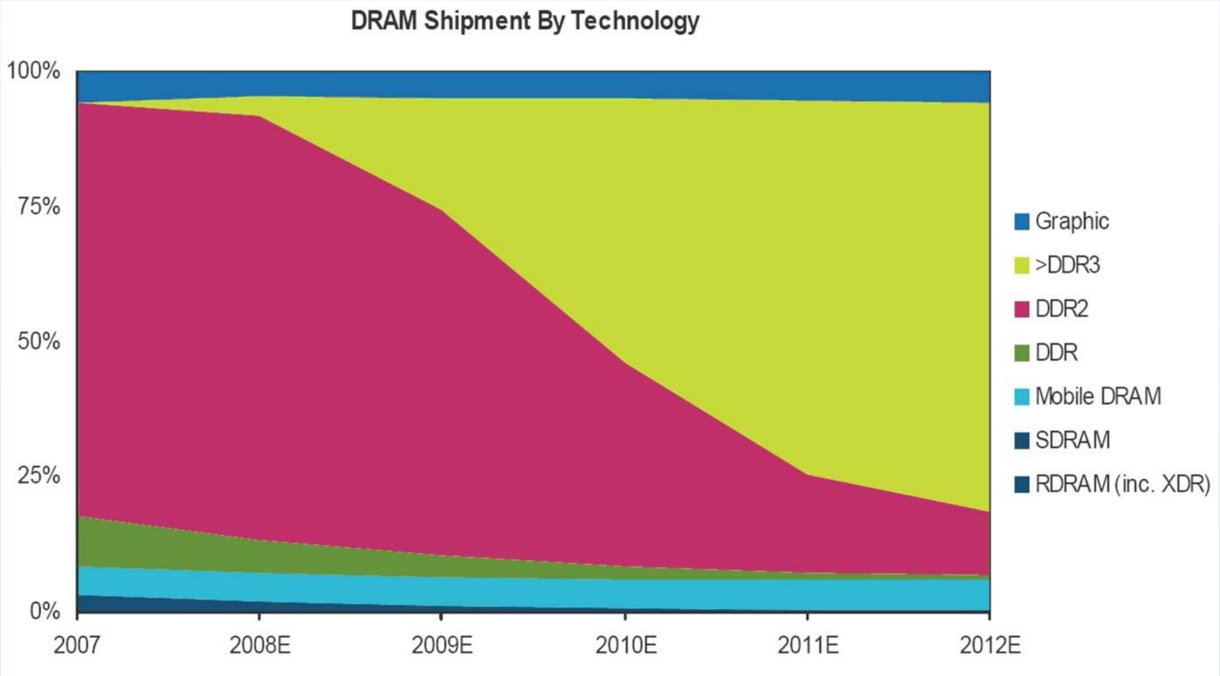
- **Computer program storage**
  - **Boot, application, safehold**
  - **Often a mix of volatile and non-volatile memories**
    - **Store in NVM, download on boot to RAM, run out of RAM**
      - **Size, Weight, and Power (SWaP) – RAM is faster than NVM**
- **Temporary data buffers**
  - **Accommodates burst operations**
- **Data Storage such as SSR**
  - **E.g. mass storage area for science or spacecraft telemetry**
  - **Usually write once an orbit, read once an orbit**
  - ***Trend to want to use NVM for SSR***
- **Configuration storage for volatile Field Programmable Gate Arrays (FPGAs)**
  - **Becoming a *bigger* problem as FPGAs increase their needs**

The Volatile Memory for Space

- Rad Hard Offerings are limited to SRAM
  - 16 Mb maximum single die
  - These tend to be medium speed and relatively high power when compared to commercial equivalents
    - For comparison, first SSR in 1990 used 256 kb commercial die
  - Still used extensively in rad hard computer offerings, but many designs have transitioned to DRAM options
- Mid-1990's = transition in SSRs from commercial SRAM to DRAM
  - SDRAM are in-flight and many current designs have begun to use dual data rate (DDR) and DDR2

The SDRAM Quandary

- **Many space designs are baselining/using DDR and DDR2 interfaces for hardware builds**
  - **Problem: *DDR3 expected to dominate commercial product starting in 2010!***
- **Do we support current system designs or product development timelines?**
  - **Will DDR2 be obsolete by system readiness dates?**



DDR Performance Metrics

	DDR	DDR2	DDR3
Data Rate	200-400Mbps	400-800Mbps	800-1600Mbps
Interface	SSTL_2	SSTL_18	SSTL_15
Source Sync	Bidirectional DQS (Single ended default)	Bidirectional DQS (Single/Diff Option)	Bidirectional DQS (Differential default)
Burst Length	BL= 2, 4, 8 (2bit prefetch)	BL= 4, 8 (4bit prefetch)	BL= 4, 8 (8bit prefetch)
CL/tRCD/tRP	15ns each	15ns each	12ns each
Reset	No	No	Yes
ODT	No	Yes	Yes
Driver Calibration	No	Off-Chip	On-Chip with ZQ pin
Leveling	No	No	Yes
	1.5V	***1.25V***	***1.0V***

The Non-Volatile Memory for Space

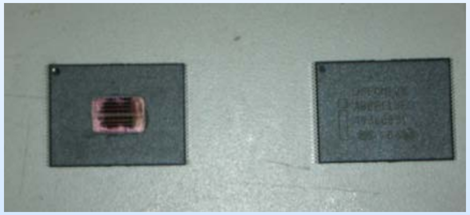
- Rad Hard offerings are limited to small SONOS or CRAM devices
  - Used in many RH processor systems that do not have large program memory space requirement – 4-16 Mb per die maximum
- Evolution of commercial NVM in space
  - PROMS
    - Older commercial PROMS were reasonably good, but one-time programmable (OTP)
  - EPROMs
    - Used in a few systems in the 90's, but had TID issues
  - EEPROMs
    - In use from the 90's to today, despite both TID and SEE (write mode) concerns
      - SEEQ 256 Mb (now obsolete)
      - Hitachi 1 Mb (now sold through re-packaging/screening houses)
  - Flash
    - The latest "in vogue" commercial NVM due to density (64Gb die now available)
      - Much improved TID than older EEPROMs
      - SEFI and SEL still issues
    - Some space system primes are planning on using these in SSR applications

"In summary, the Signetics PROMs are recommended (given previous total dose studies) for usage as are the SEEQ EEPROMs during read operations. It is not recommended, pending further investigation, to use the SEEQ EEPROMs for in-flight programming. "

- LaBel, Nov 1990 Test Report

Alternate Material NVMs

- Alternate material NVMs – evaluated as devices become available
  - Expect cell integrity to perform fairly well under irradiation on most NVMs
  - LaBel's Truism:
    - *There are ALWAYS more challenges in "qualifying" a new technology device than expected*
- Phase change memories (PCM)
  - Density, speed, and power look promising
    - Temperature is the challenge
  - Ex., Samsung, Numonyx – initial data taken
- CNT
- MRAM
  - Spin Torque appears to improve SWaP metrics
  - Ex., Avalanche Technologies
- Resistive Memories
  - Ex., Unity Semiconductor, HP Labs
    - Unity's talking about a 64Gb device by next summer!
- NVSRAMs
  - Ex. Cypress



Numonyx PCM –
Tech transfer opportunity?

The Changing World of Radiation Testing of Memories -

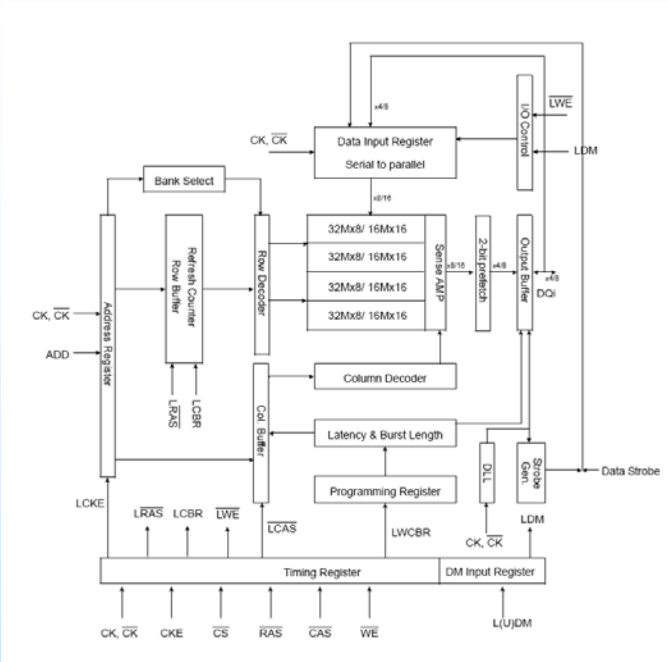
Comparing SEE Testing of Commercial Memories – 1996 to 2006

- **Device under test (DUTs): Commercial Memory**
  - For use in solid state recorder (SSR) applications
- **1996**
  - SRAM memory
    - 1 um feature size
    - 4 Mbits per device
    - <50 MHz bus speed
    - Ceramic packaged DIP or LCC or QFP
- **2006**
  - DUT: DDR2 SDRAM
    - 90 nm feature size
    - 1 Gbit per device
    - >500 MHz bus speed
    - Plastic FcBGA or TSOP
    - Hidden registers and modes
    - Built-in microcontroller

- **Sample Issues for SEE Testing**
  - Size of memory
    - Drives complexity on tester side for amount of storage, real time processing, and length of test runs
  - Speed
    - Difficult to test at high-speeds reliably
      - Need low-noise and high-speed test fixture
    - Classic bit flips (memory cell) extended to include transient propagation (used to be too slow a device to respond)
    - Thermal and mechanical issues (testing in air/vacuum)
  - Packaging
    - Modern devices present problems for reliable test board fixture, die access (heavy ion tests) requiring expensive facility usage or device repackaging/thinning
    - Difficulty in high-temp testing (worst-case)
  - Hidden registers and modes
    - Functional interrupts driving "anomalous data"
      - Not just errors to memory cells!
  - Microcontroller
    - Not just a memory

Commercial memory testing is a lot more complex than in the old days!

Can we test anything completely?



Commercial 1 Gb SDRAM

68 operating modes

operates to >500 MHz

Vdd 1.8V external, 1.25V internal

Sample Single Event Effect Test Matrix

full generic testing

Amount	*Item*
3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

66096 Hours

2754 Days

7.54 Years

and this didn't include temperature variations!!!

Test planning requires much more thought in the modern age as does understanding of data collected (be wary of databases). Only so much can be done in a 12 hour beam run – application-oriented

The "Perfect" Space Memory

- SWaP rules!
  - No power, Infinite density, Fast (sub 2 ns R/W access)
    - Oh, and Rad Hard (RH)
- Okay, so this isn't happening!
  - Speed:
    - Needs to be fast enough for burst data capture and not a bottleneck for processor interfaces
  - Power:
    - This is a trade space that includes thermal (stacking, for example)
    - NVM is good since no power consumed when not being accessed
  - Density:
    - Gb regime per die – anything beyond 100 Mb is acceptable!
    - Biggest RH devices currently ~16 Mb regime
      - Note: 1st SSR used 256 Mb commercial SRAMs 20 years ago!!!
- And a personal diatribe: how many operating modes do we really need?
  - Byte/nibble and page modes
    - Erase for NVM

Radiation Requirements (and trends)

- How radiation hard to we really need?
  - TID
    - >90% of NASA applications are < 100 krads-Si in piecepart requirements
      - Many commercial devices (NVM and SDRAMs) meet or come close to this.
      - Charge pump TID tolerance has improved ~ an order magnitude or more over the last 10 years
    - There are always a few programs with higher level needs and, of course, defense needs
  - SEL
    - Prefer none or rates that are considered low risk
      - Latent damage (“non-destructive” event) is a bear to deal with
    - As we’re packing cells tighter and even with lower Vdd, we’re seeing SEL on commercial devices regularly (<90nm)
      - Often in power conversion, I/O, or control areas
  - SEU
    - It’s not the bit errors, it’s the SEFIs and uncorrectable errors that are the biggest issues
      - Scrubbing concerns for risk, power, speed…

Reliability Considerations

- **Besides the usual CMOS concerns, memories have a few other considerations**
  - Data retention
    - Long-term holding of values and/or requirement to refresh values
  - Endurance
    - Ability to read and write values N times (10^5 cycles is typical commercial NVM spec, for example)
  - Bit disturb (usually with Flash)
    - I.e., read/write/erase of bit A disturbs values on adjacent bit-line
  - Note: Many memories have "bad bits" to begin with that are mapped
- **Now add in unique space requirements**
  - >10 year mission life
  - Colder and hotter temperatures (-55 to +125C)
  - Radiation

NEPP and Memories

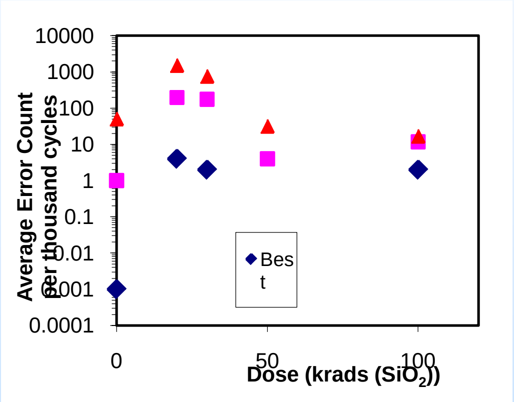
- **Top level agenda**
  - **Evaluate scaled commercial SDRAMs and NVMs**
    - **Radiation tests first**
      - ***If reasonable, reliability and combined radiation/reliability***
  - **Work with new memory technologies and manufacturers considering entry into Mil/Aero market**
    - **PCM**
    - **MRAM**
    - **RRAM**
    - **DDR3, and so on**
  - ***We do not QUALIFY devices, but evaluate suitability of devices and determine appropriate qualification methods and physics of failure***

NEPP Radiation Evaluations - NVM

- Commercial Flash Memories
  - Manufacturers evaluated (1-8 Gb per device)
    - Micron, Samsung, Hynix, …
    - TID is mostly > 50 krads-Si
      - Biased/unbiased tests
      - Low and high dose rate tests (only Samsung showed significant improvement at low dose rates)
    - Most NVM cells have fairly good SEU tolerance and it's the surrounding circuits that have SEU sensitivity
      - SEL varies by manufacturer
        - » Current spikes noted during some heavy ion tests are being evaluated
      - SEFIs are a prime issue
    - Focus has been on Single Level Cell - SLC
      - Multi Level Cell - MLC has lower cell margins and data shows typically less radiation tolerance
  - Further scaled, MLC and SLC, and higher density to be evaluated in FY10
    - 64Gb Micron die in hand!
- Continue working with PCM, MRAM, CNT, etc.. as available

Combining Radiation and Reliability - NVMs

- **FY09 began new studies on Flash memories combining TID with endurance**
  - **Result: TID did NOT degrade endurance properties at room temperature**
- **Considerations for FY10**
  - **Perform TID and lifetime/data retention tests**
    - **Must be carefully planned since high temperature typically used for accelerated life/retention tests has two inherent issues with Flash/NVM**
      - **Anneals radiation damage**
      - **May cause bit flips above commercial operating temperatures**
    - **May require lower temperatures, voltage acceleration or other to be considered**



FY10 NEPP - Volatile Memory Efforts

- We have been debating this topic internally
  - Current in-house radiation tester is “borderline” for 1.0V, >400 MHz DDR3 SDRAMs
    - New tester design under development (Spartan-6)
  - Difficulty in obtaining test samples for “shrunk” DDR2s and new DDR3s
    - You can’t test what you can’t get
      - Elpida, Micron, Samsung,…
      - Possibility of split-epi from Mfr A?
  - The Quandary returns: DDR2 or DDR3 to evaluate???
    - We need to consider new reliability tests as well
- QDR and ASRAMs are being evaluated from Cypress
  - Alternates to Rad Hard?

Considerations

- Technology changes in memories engender challenges
  - Impact of new materials and manufacturing methods on radiation response and modeling
  - Increasing difficulty in die accessibility
  - Increasing operating speeds and operating modes
  - More hidden "features" and limited testability
  - Multi-level storage cells (Flash, for example)
  - Unique reliability concerns
- We need to invest to keep ahead of the curve
  - DDR3 tests now?
  - PCM
  - ST MRAM
  - Reliability on RRAM, etc…
- It's the challenges the keeps us employed!

We are always open to working with others