NEPP Electronic Technology Workshop
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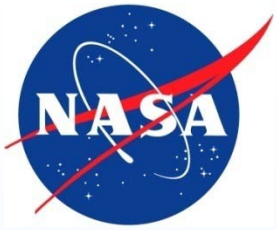
National Aeronautics
and Space Administration



NAND Flash Memory Latency Dependence on Cycling

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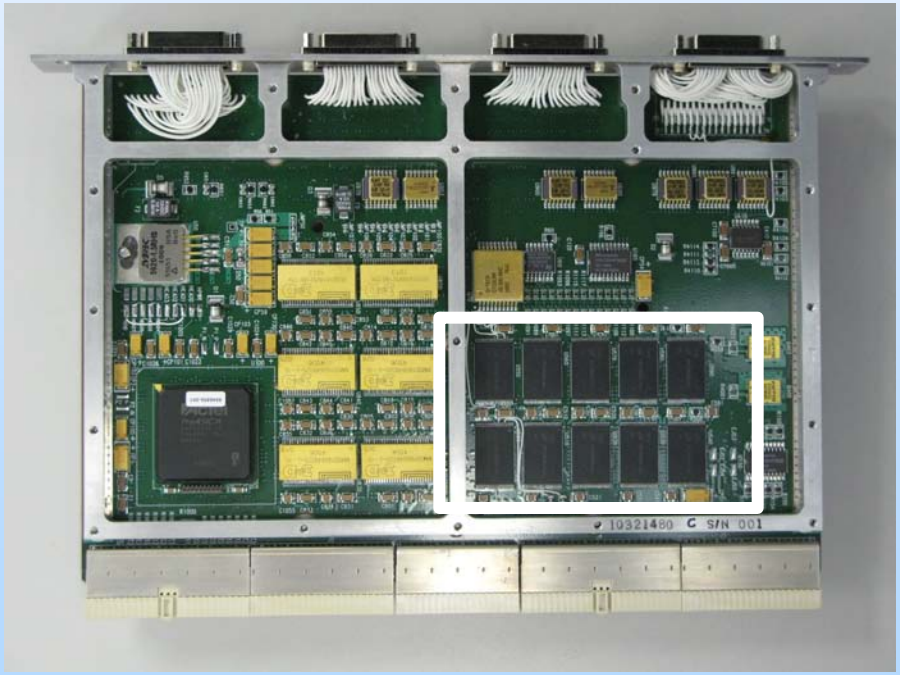
Note: Please submit the NASA Form 1676: NASA Scientific and Technical Information (STI) Document Availability Authorization (DAA) and the GSFC 25-49: GSFC STI Public Disclosure Export Control Checklist (or equivalent) for your oral presentation charts (or poster) as we will be posting these on the NASA NEPP web site.

Uses of NAND Flash

- NAND Flash is used as mass storage memory in commercial markets (iPhone, MP3, digital camera, laptop) as well as space (radar, camera).
- Flash chip density in consumer products are typically 2-64 Gb.
- Densities flown in space to date are closer to 256 Mb – 8 Gb (~10x smaller).
- However, space missions' appetites are growing…

Missions Want More Memory

- Space missions are utilizing higher densities of NAND Flash and in larger quantities (>1Tb worth of 32 Gb MLC on SMAP).
- Storing radar and radiometer data.
- Spacecraft making several orbits per day.



Ten 128Gb devices (12.8 Tb) on a single board

How long does it take to write 128 Gb?

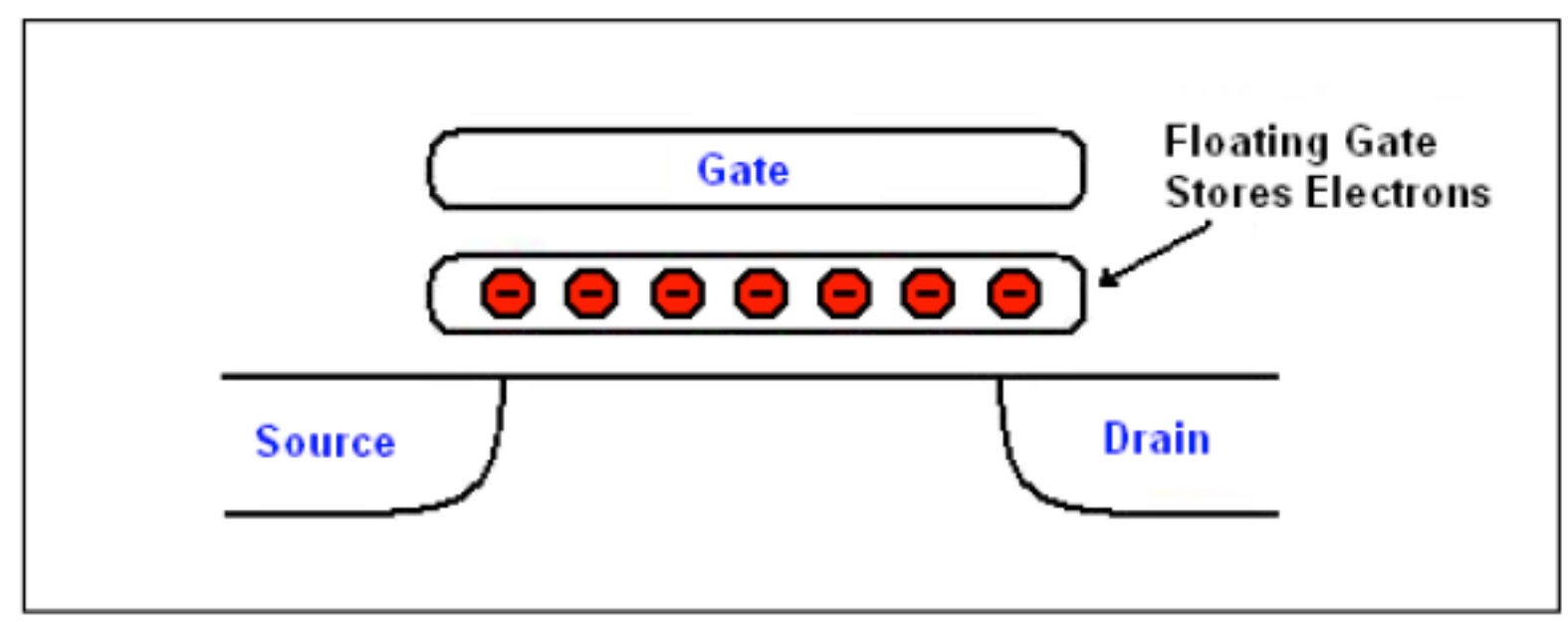
- **Worst case:**
  - **50 MHz**
  - **Max datasheet spec tBERS, tPROG, tR**
  - **To erase, program, and read a 128 Gb device... 3 hours**

- **Typical beginning of life:**
  - **50 MHz**
  - **Typical datasheet spec tBERS, tPROG, tR**
  - **To erase, program, and read a 128 Gb device… 1 hour**

These numbers matter when you're trying to cycle ten devices multiple times in a day. These calculations also assume no ECC overhead. ECC overhead is significant. BCH algorithms (recommended for these devices in commercial application) increases these times significantly (2x-3x). Parallel operation, plane interleaving, and die interleaving become necessary.

Understanding what tBERS, tPROG, and tR look like EOL is very important.

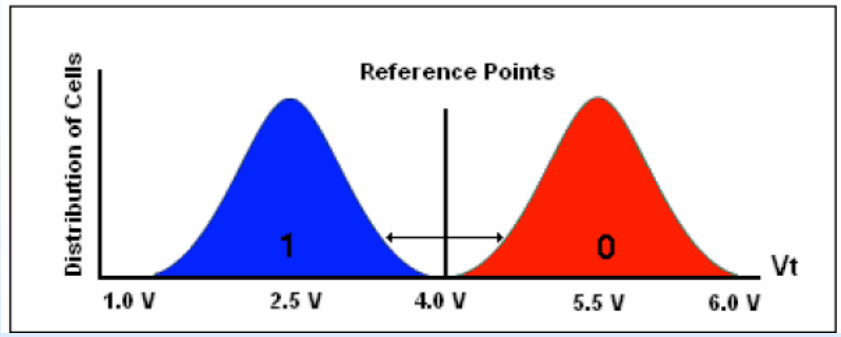
NAND Flash Technology



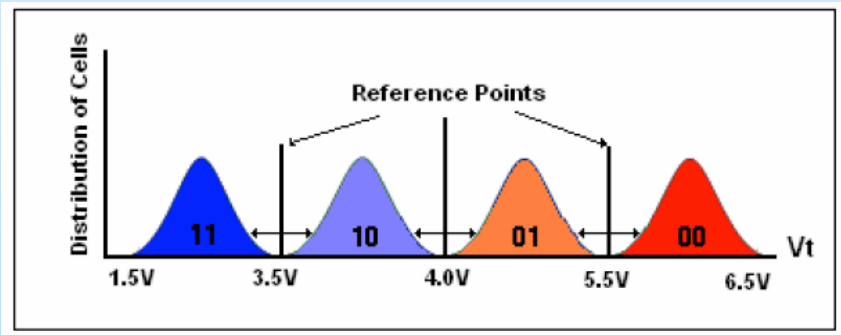
- **Memory states are stored as charge in floating gate of single-transistor cell.**

SLC & MLC

SLC:



MLC:



Leading Failure Mechanisms

- **Primary failure mechanism is gate oxide degradation due to high voltage program and erase operations (Fowler-Nordheim Tunneling).**
- **Limits number of erase/program/read cycles.**
- **Transistor threshold voltage (Vt) shift.**

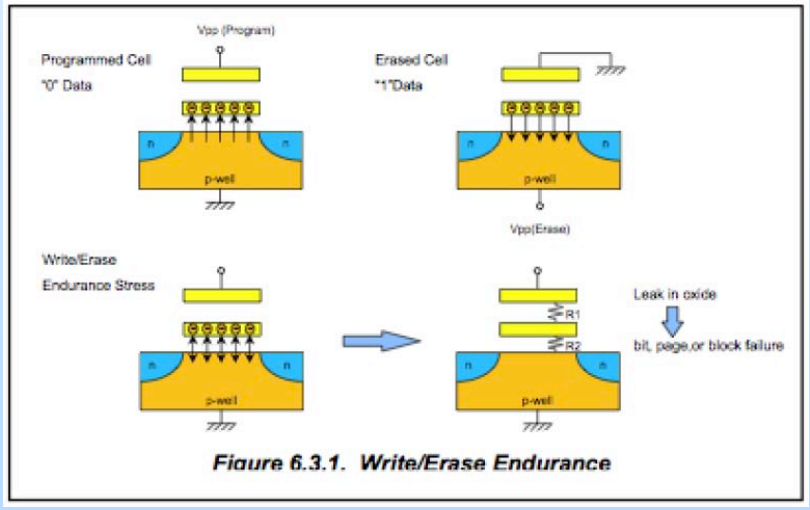


Figure 6.3.1. Write/Erase Endurance

Vt Shift Changes EOL Performance

- **Shifting threshold voltages leads to changes in time it takes to erase (longer) or program (shorter) a cell.**
- **Understanding how these program, erase, and read latencies change is important to NASA missions needing to understand EOL performance.**

Task Mission: Is Latency (Performance) Still Acceptable after Cycling (at EOL)?

- As the NAND is cycled (erase/program/read) many times, degradation of the memory cell will affect the times needed to do these operations and the associated latencies will change.

- Projects must consider the trade-offs between:
  - How much data does our science team require us to record?
  - How much ECC is required to reliably use a given technology?
  - Does our design provide enough performance to support the science and reliability requirements?

- To answer these questions, it is important to understand how read, program, and erase latencies can change with cycling.

NEPP Task

Description:

– ***Evaluate Flash memory latency as a function of endurance cycling.***

FY10 Plans:

– For multiple manufacturers and densities of NAND Flash, measure tR, tPROG, and tBERS as a function of erase/program/read cycling.

– Latency characterizations will be performed at 0 cycles, 0.5x specification and 1x specification on 12 blocks from 4 die of each part type (48 blocks total per device type).

– Nominal Vcc (3.3 V). 25 C.

– Part Numbers:

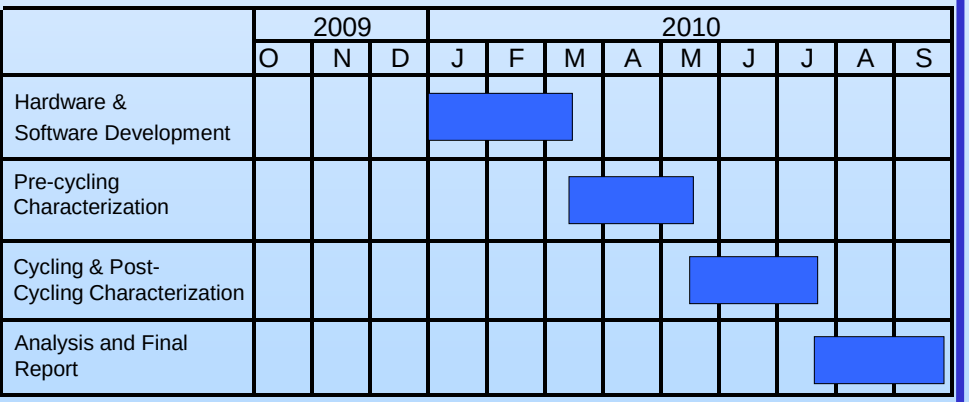
  – Micron, 128G MLC (32Gx4 die), MT29F128G08CJAAA

  – Micron, 8G SLC, MT29F8G08AAA

  – Samsung, 8G MLC, K9G8G08UOM

  – Samsung, 8G SLC, K9F8G08UOM

Schedule:



Deliverables:

– Final report including characterization data, plots, and analysis.

– Final report shall give NASA missions a better picture of EOL performance of these Flash devices.

Goals

- **Goals (FY10):**
  - **Measure dependence of read, write, and erase latencies as a function of erase/program/read cycles.**
  - **Share this information with flight projects interested in using high density NAND Flash memories.**

Expected Impact to Community

- **By characterizing EOL Flash performance and demonstrating reliable operation (especially in MLC NAND devices), NASA flight missions will have an order of magnitude greater memory density in a single chip, saving size, weight, and power.**

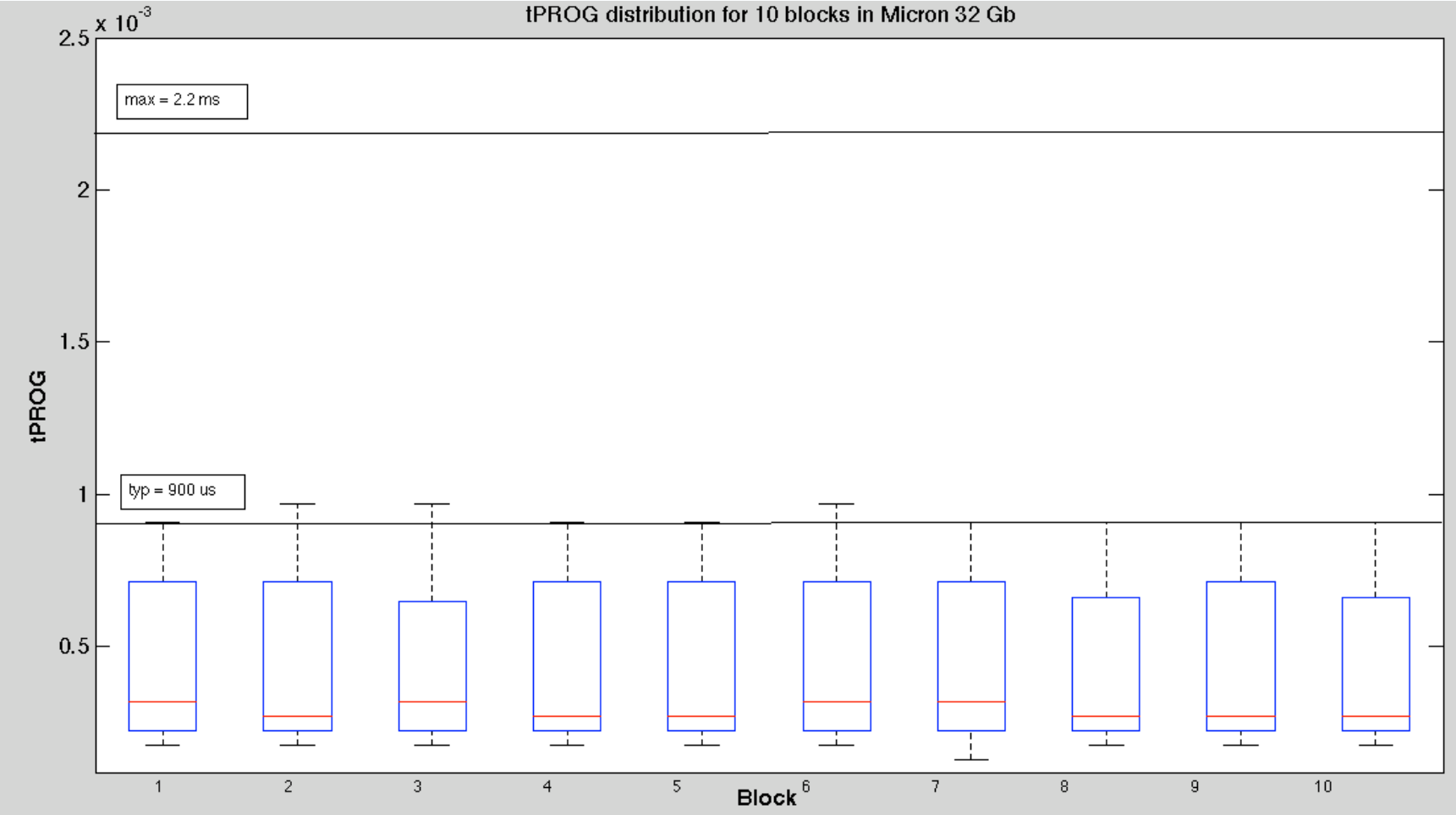
- **Flight projects wishing to utilize high density NAND Flash with significant ECC requirements will have a better understanding of the EOL performance of the devices.**

Status/Schedule

- **Pre-cycling characterization completed.**

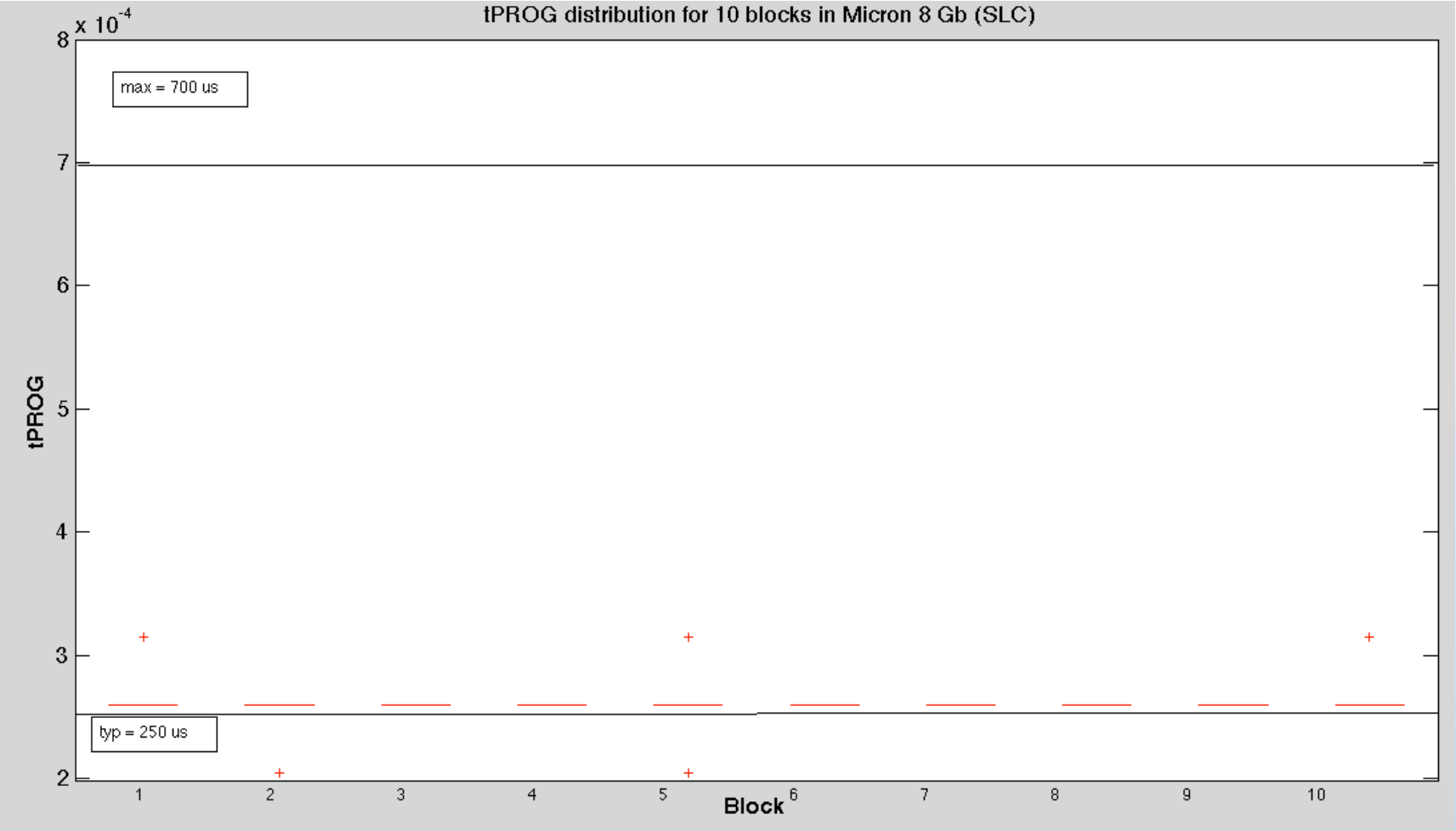
Manuf.	SLC/ MLC	Density	Pre-Cycling Characterization	Cycling & Post-Characterization
Micron	MLC	32G	X	
	SLC	8G	X	
Samsung	MLC	8G	X	
	SLC	8G	X	

32 Gb tPROG (Pre-Cycling)



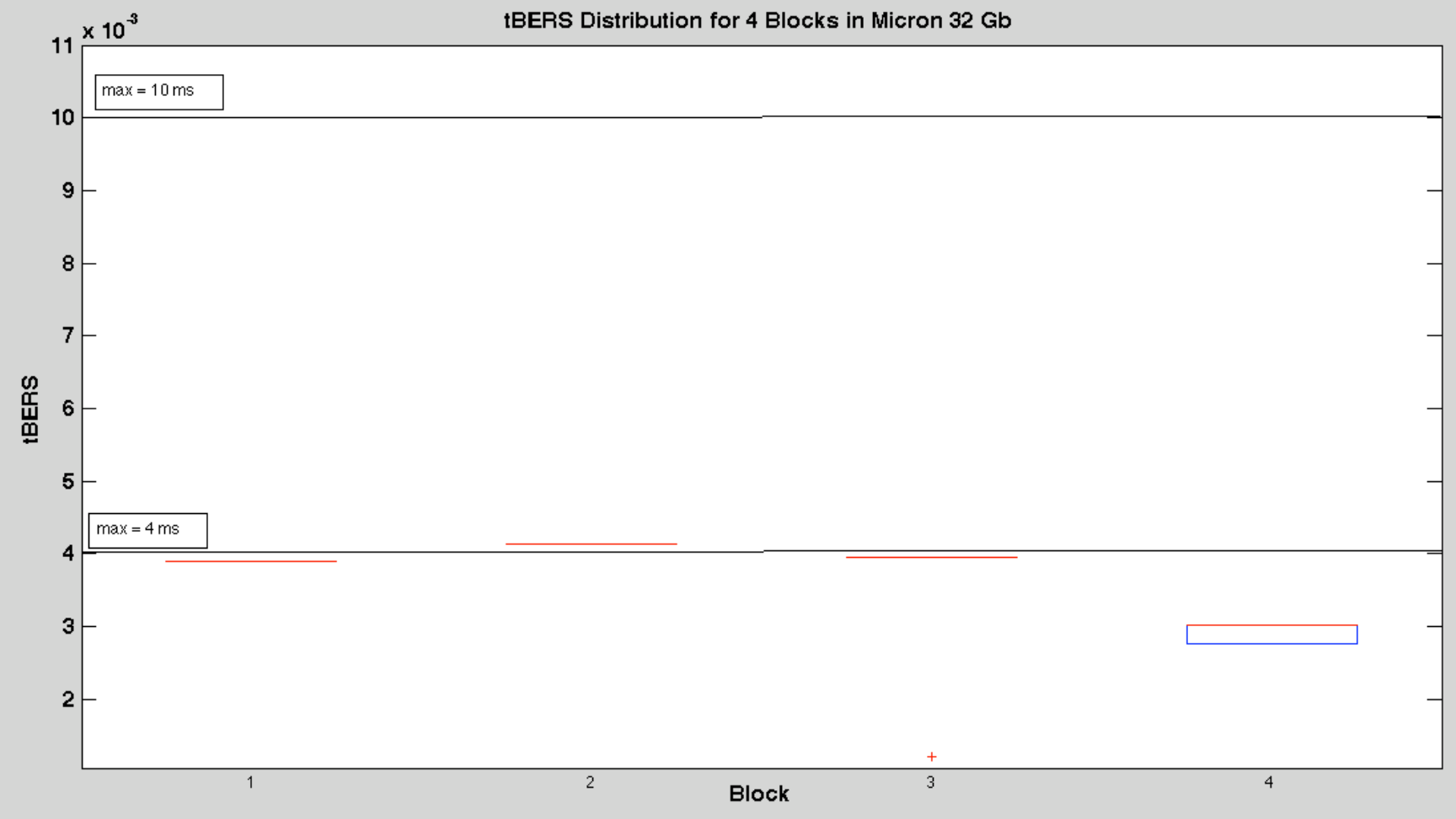
Distribution of tPROG for 32 Gb (pre-cycling) showing variation across pages within a block.

8 Gb tPROG (Pre-Cycling)



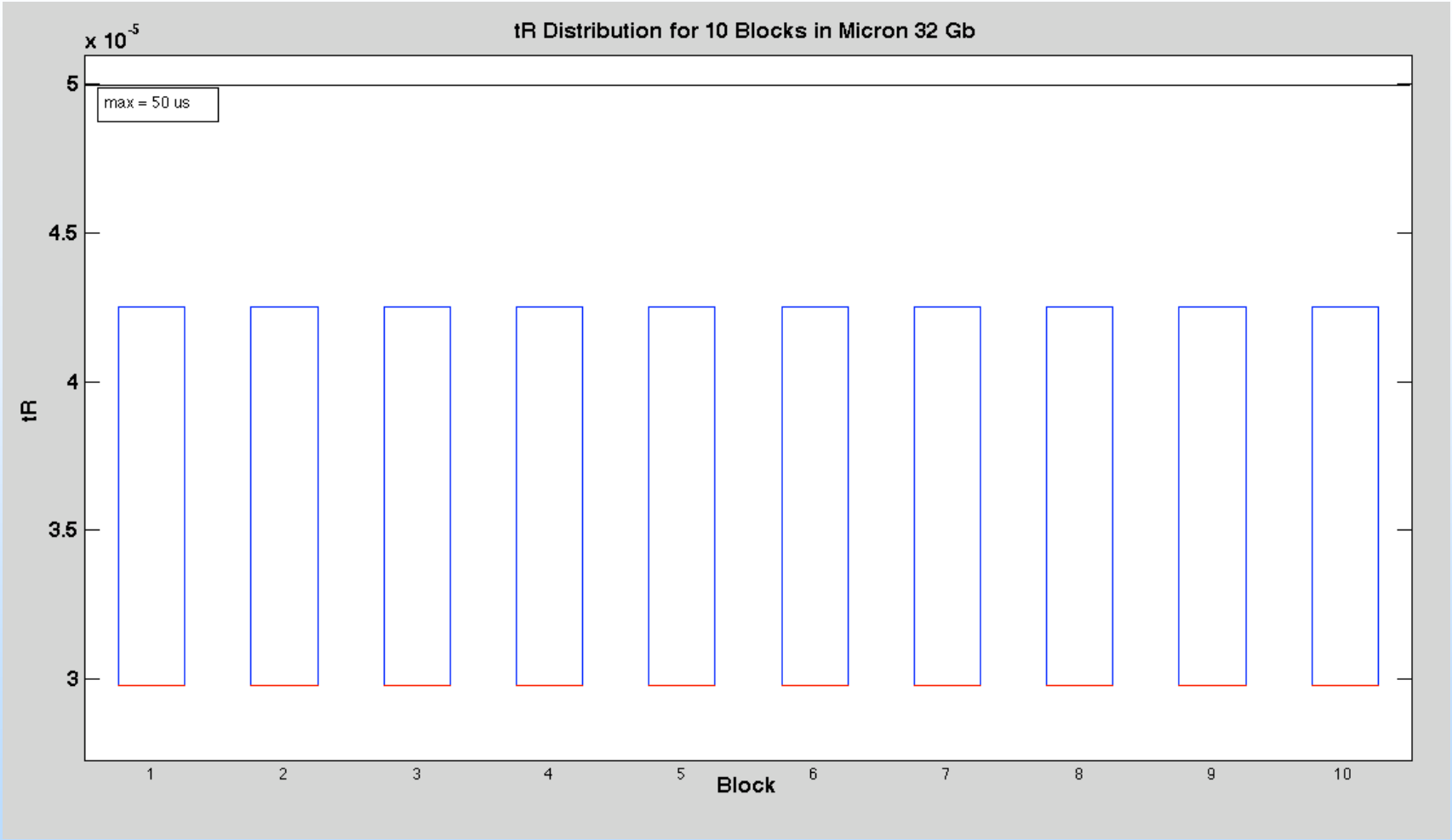
tPROG distributions in this SLC is much tighter than MLC from same manuf. (pre-cycling)

32 Gb tBERS (Pre-Cycling)



tBERS values are almost always the same for a given block, (pre-cycling). This is true for SLC and MLC.

32 Gb tR (Pre-Cycling)



For this device, tR is always 29.75 us or 42.5 us. (pre-cycling)

Plans (3Q-4Q FY10)

- **Cycle devices.**
- **Perform post-cycling characterization.**