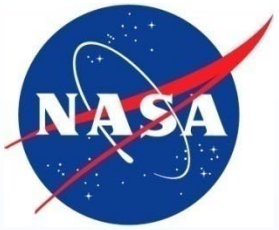
NEPP Electronic Technology Workshop
June 22-24, 2010

National Aeronautics
and Space Administration



CMOS Reliability Challenges - The Future of Commercial Digital Electronics and NASA

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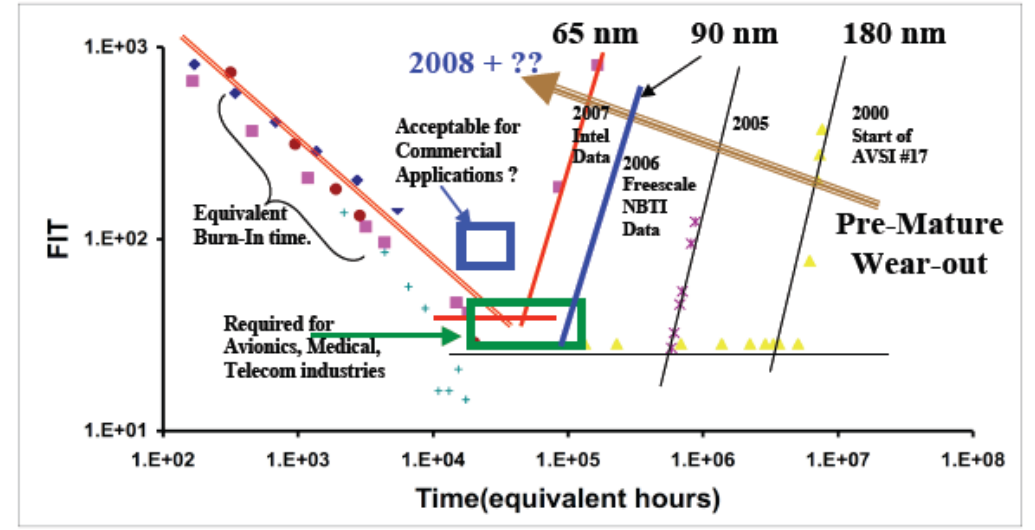
Why is Scaled CMOS of Interest?



Technology trend shows significant decrease in lifetime of modern devices… but this is also coupled with significantly decreased design lifetime.

- **Failure rates in modern CMOS devices are accelerating.**
- **Manufacturers design products to last around 3 years (and are often aged-out by the customer by choice).**
- **Trends in temperature and voltage response of basic structures suggest significant degradation with stress testing.**
- **Application of single-temperature, single-voltage testing (Std Mil Spec flow) is not particularly perceptive in addressing reliability and margin of prospective commercial devices.**
- **Application use conditions must be considered.**
- **Derating of these devices is very important for use.**
- **But there is a silver lining – margin. … and fault tolerance.**
- **Testing of radiation degradation improves confidence.**

Intro

Modern CMOS devices pose increasing reliability risks to NASA missions as they are designed for very short cycle time and benign environments.

The NEPP Scaled CMOS task addresses reliability questions related to use of devices outside of their design lifetime, and in harsh environments such as extreme temperatures and radiation.

In order to accomplish this, several efforts are required. Reliability data must be gathered on devices of interest. This requires continually improving test capabilities and actually engaging industrial partners. Data must be analyzed for critical reliability parameters. Extracted parameters are used to build temperature, voltage, and radiation models to predict device reliability.

These efforts are used to develop recommended practices for use of next-generation devices (which will are reported in a guideline). The impact is often specific to each device type necessitating device-based recommended practices. For many devices the recommendations are *margin and fault tolerance*.

NEPP Task

Description:

– CMOS technology scaling has posed increasing parts reliability concerns which affect the whole bath tube curve regions, i.e., infant mortality region, constant failure rate region, and wear-out region.

–Infant mortality increases with scaling in feature size

–Failure rate increases with scaling feature size

–Wear-out mechanism induced parts failure may become visible during parts operating life

–Understanding the scaling impact on parts reliability and the limitations of progressively scaled CMOS technologies from a PoF standpoint will lead to improved reliability prediction and will help projects more effectively mitigate risk.

–Successful technology insertion is premised on improved reliability prediction modeling, and efficient and meaningful screening and qualification protocols.

–Historical one temperature pass/fail screening/life test approach may be missing important degradation mechanisms and may fail to catch the dominant failure mechanism.

FY10 Plans:

–Evaluate a best practice for evaluating future technologies such as 45 and 32nm. These results will then be analyzed with respect to previous technology nodes where the reliability is now known and a methodology will be developed for extrapolating from previous missions to future mission reliability prediction.

–Continue testing including High Voltage, High Temperature, Low Voltage, High Temperature, and High Voltage Low Temperature active life tests on ring oscillator structures and on SRAM cores for 65nm and 45nm technology built into commercial products manufactured at TSMC.

–Perform a statistical analysis verifying the randomness of the projected failure times and fit the results to accepted PoF models for lifetime degradation. The models will include HCI, NBTI, TDDB and EM. Evaluate if any of these lead to failures for long-life missions such as required by NASA.

–Continue testing 6/7Xnm SDRAMs and investigate data retention degradation trends and general models as a function of stress conditions.

–Collaborate with AVSI Consortium on microelectronics reliability modeling & lifetime evaluation of progressively scaled devices.

–Coordinate reliability prediction methodology results with JEDEC/G12/Aerospace Corp. to develop improved Standards and Guidelines.

Schedule:

	2009			2010								
Scaled CMOS Reliability	O	N	D	J	F	M	A	M	J	J	A	S
Accelerated stress testing on scaled technologies (6X/7Xnm)	X	X	X	X	X	X	X	X	X			
Data analysis on reliability tests									X	X	X	
Modeling - Reliability prediction							X	X	X	X	X	
JEDEC/G12/Aerospace Coord.			X	X	X	X	X	X	X	X	X	X
Standards Development			X	X	X	X	X	X	X	X	X	X
Guideline Update												X

Deliverables:

–IRPS/TDMR technical paper on results

–Updated NASA guidelines

–JEDEC/G-12 Coordination, Stds. Development

External Partners:

–Aerospace Corp.

–JEDEC/G-12 Committee Coordination

–OEM Test Support

–Freescale, TSMC

–AVSI Consortium

–Aerospace Corp. Boeing Phantom Works, Lockheed Martin, Navy-Crane, DLA, Honeywell, Goodrich, GE, FAA, Airbus

Goals

- **Goals (FY10):**
  - **Continue development of the Scaled CMOS guideline for evaluating the reliability of CMOS devices for NASA missions. "Scaled CMOS Reliability User's Guide", JPL Publication 09-33 01/10.**
  - **Participate in aerospace industry efforts to coordinate CMOS reliability research.**
  - **Continue testing of devices towards higher integration parts operating in more modern circuits, including multiple device types.**
  - **Develop capabilities to enable testing of the next generation of devices.**
  - **Perform preliminary evaluation of radiation effects using reliability physics methods, as a way to expand the reliability user's guide.**

Goal #1: Reduce the risk of using highly scaled devices in NASA missions by providing custom data, models, and usage guidelines relevant to NASA mission environments.

Expected Impact to Community

- **Recommendations**
  - **Derived from operation & analysis in reliability environment.**
  - **Margin, margin, and fault tolerance – device specific.**
- **Guideline**
  - **Provides test data**
  - **Provides models for part degradation**
  - **Provides predicted FIT rates for technology**
  - **Develops usage guidelines to minimize risk**
- **Significant Community Collaboration**
  - **JEDEC/G12 Committee**
  - **AVSI Consortium**
    - SRAM & Ring oscillator structure wear out calculator partially supported by NEPP.
  - **Industrial Collaborators:**
    - Aerospace Corp. Boeing Phantom Works, Lockheed Martin, Navy-Crane, DLA, Honeywell, Goodrich, GE, FAA, Airbus
- **Provides means for improved technology research capabilities (laboratories) at NASA**

Reduce risk through recommendations, community feedback, and by updating test, model, and predictive methods.

Status/Schedule

- 2007 – Physics of Failure study and application to modern CMOS devices.
- 2008 – Examined 90 and 65 nm ring-oscillator structures and SRAM cores. (Partners)
- 2009 – Developed models for predicting failure rate of DDR devices (90-130nm). Also developed methods for predicting FIT rate in these devices. Tested these devices (Via partners).
- 2010 – Improving data collection methods to enable testing of 78nm DDR2 devices by NASA.
  - Currently on track to have 1000 hour stress of 2 manufacturers at room temperature and elevated temperature.
  - Also beginning analysis of radiation effects on wear out.
  - Beginning 1000 hour stress with proton exposure (starting 06/29/2010).

Qual. Recommendations I

- **Scaling of CMOS is creating reliability questions in terms of operating voltage, temperature, frequency, leakage current, and device lifetime.**
- **A multi-variable stress test approach provides much better resolution into pertinent acceleration and derating factors and actual margin for a given application.**
- **Consider accelerated temperature and voltage tests to qualify newer generations of scaled technologies.**
- **Historical one temperature pass/fail approach may be missing important degradation mechanisms or trends.**

Qual. Recommendations II

- **General observations:**
  - Commercial (0C to 70C) rated parts seem to perform well over full mil-spec temperature range.
  - Parts seem to operate and remain within spec to at least 1.4x rated voltage.
  - Parts seem to operate and remain within spec well below min. operating frequency.
  - Progressively scaled parts have tighter process controls, and for same memory density and stress conditions, have better reliability and quality characteristics.
  - Trade-offs must be considered for higher densities, higher levels of integration per unit area, and operating stress conditions, including overall power dissipation.
- **Reliability assessment of scaled microelectronics must be an ongoing effort.**
  - Accelerated testing of devices focusing on degradation effects at multiple conditions is best way to assess temperature and radiation driven failure mechanisms. This will lead to improved reliability predictive models.
- **SRAM is different than Flash is different than SDRAM…**

Study Targets

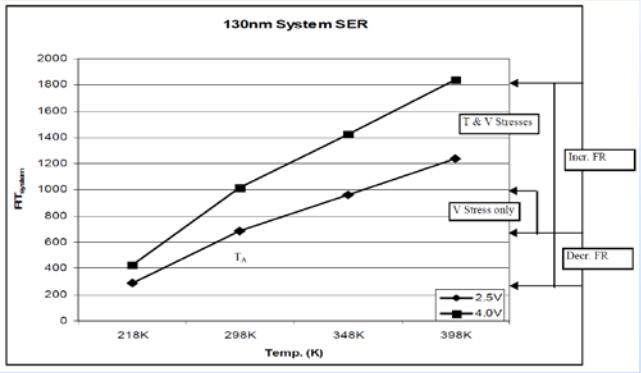
- **SDRAM Devices (130nm & below)**
  - Target of study for technical details later in this presentation.
  - Spacecraft are starting to transition to DDR2
  - Preparation for next generation requires understanding reliability issues of DDR2 and early efforts on DDR3
  - DDR devices have held a stagnant position in the commercial market which has kept even DDR3 above the 45nm point.
- **SRAM Cores (45 & 65nm)**
  - These are the building blocks of many other devices.
- **Other Devices**
  - Oscillator Test Structures
  - Flash memory

Need to study next-generation, 45nm and below structures is high. But we use DDR devices above 45nm due to limited device availability.

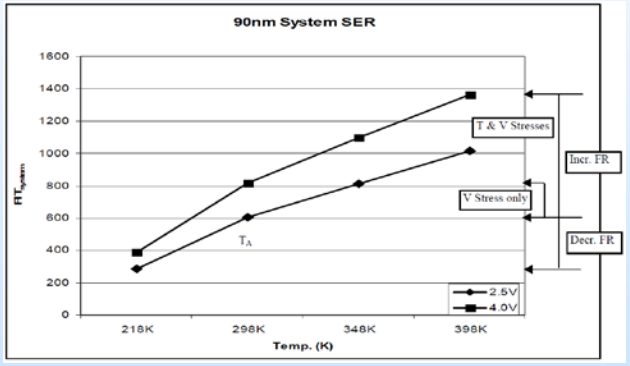
Physical Soft Error Failure Model

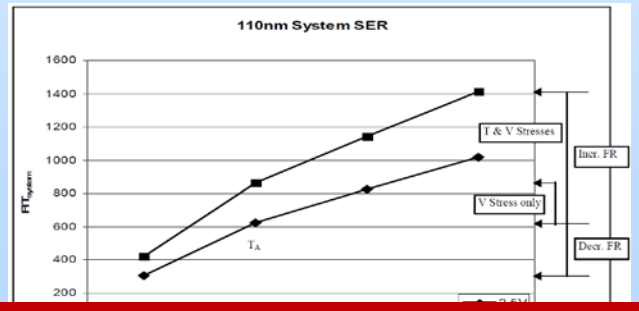
- Acceleration model (product of AF's using the Power Law for AFv) best fits the DRAM retention time data.
- The thermal element is the main contributor to Tret breakdown degradation, the voltage element contributes to the thermally activated mechanism by slightly increasing the junction temperature.

$$AF2 = \frac{\lambda(T_2, V_2)}{\lambda(T_1, V_1)} = AF_T \cdot AF_V = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)(V_2 / V_1)k)$$



Part degradation Acceleration Factors and Derating Factors may be calculated as a function of Temperature and Voltage for a given application.





–110nm 512Mb part reliability better than 130nm parts

–90nm 512Mb part reliability better than 110nm parts

Model combines Temperature and Voltage sensitivity. Being expanded to include radiation sensitivity.

Previous Results for FIT Rate

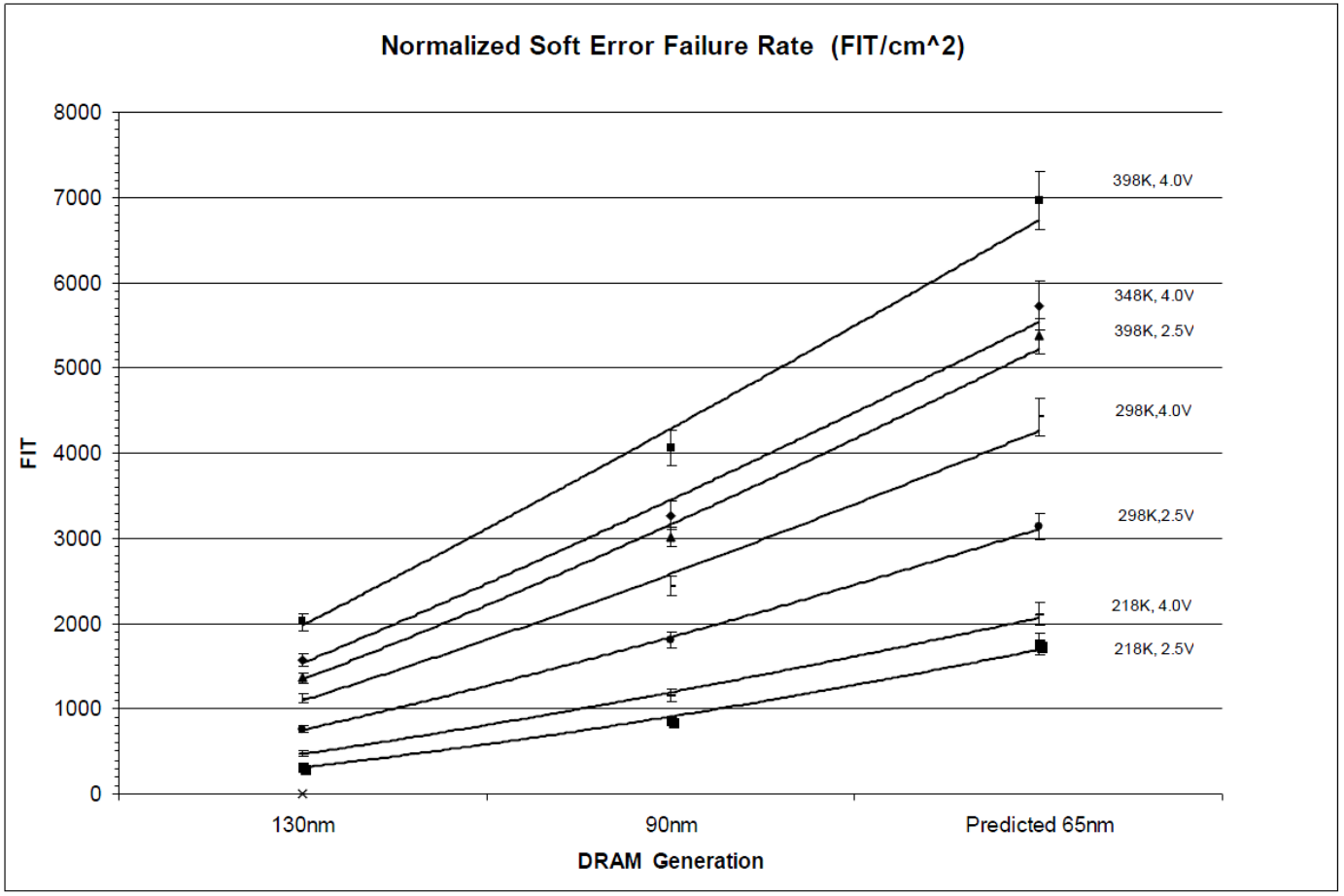
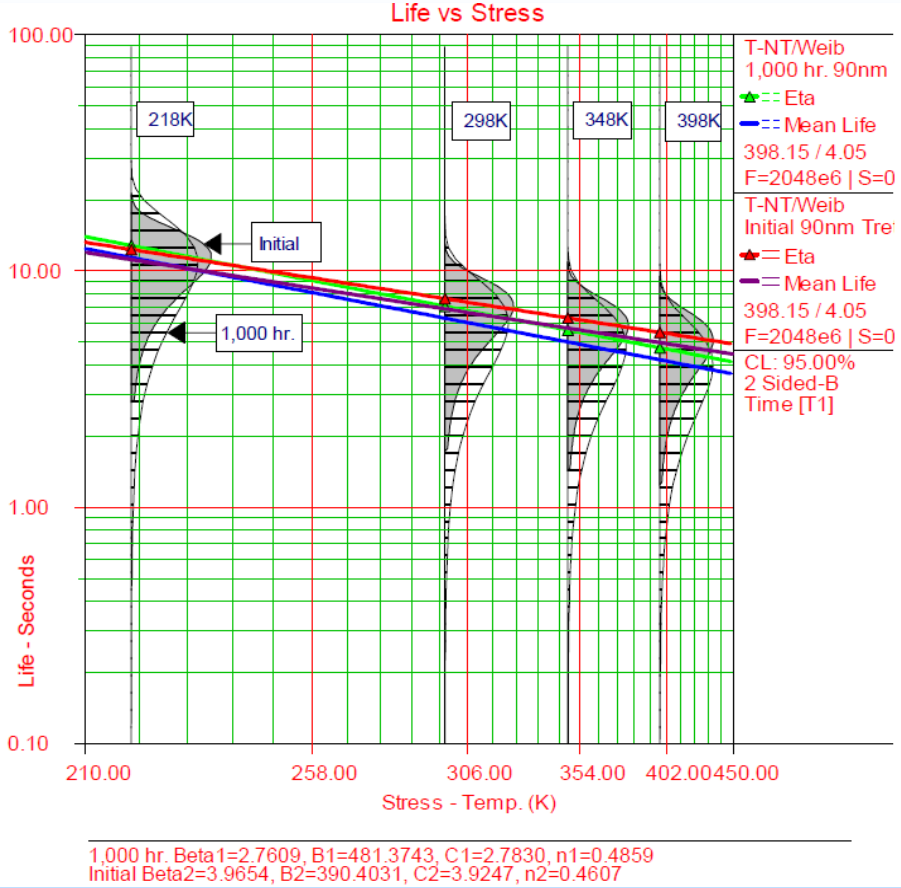


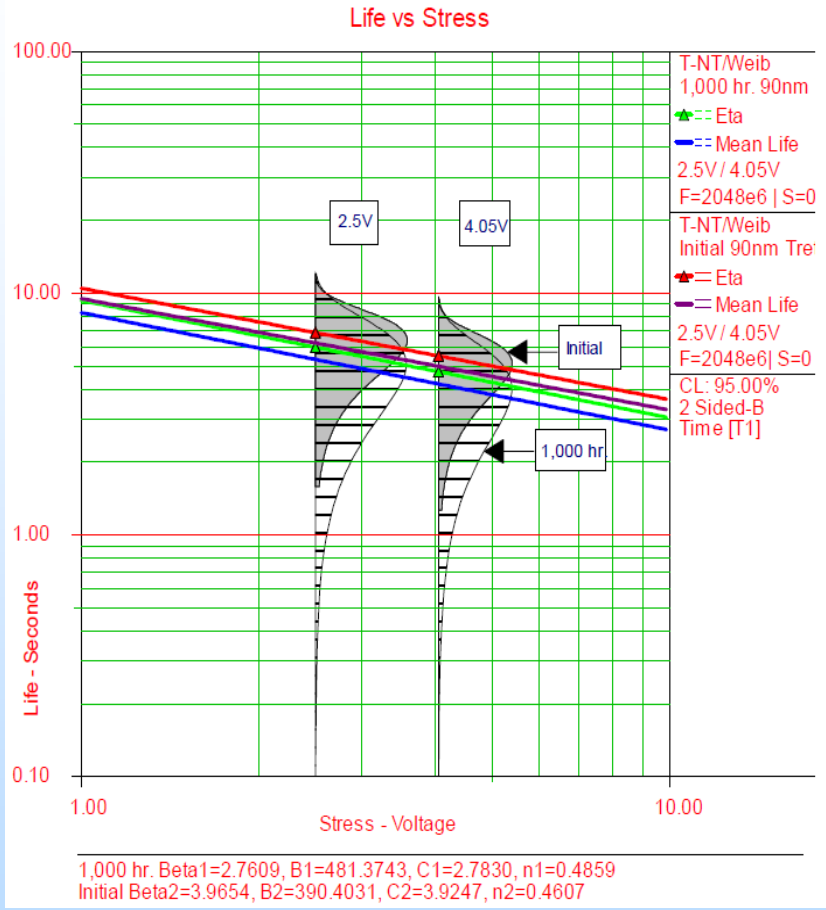
Figure 38. Normalized Soft Error Failure Rate for Scaled DRAM (FIT/cm^2).

FIT rate is increasing with feature size scaling, temperature, and operating voltage. Impact of radiation under investigation.

90nm Characteristic Life – Stress Relationship
Experimental Results



90nm T-NT/Weibull Initial and 1,000 hr.
Tret Stress Plots at Fixed Voltage

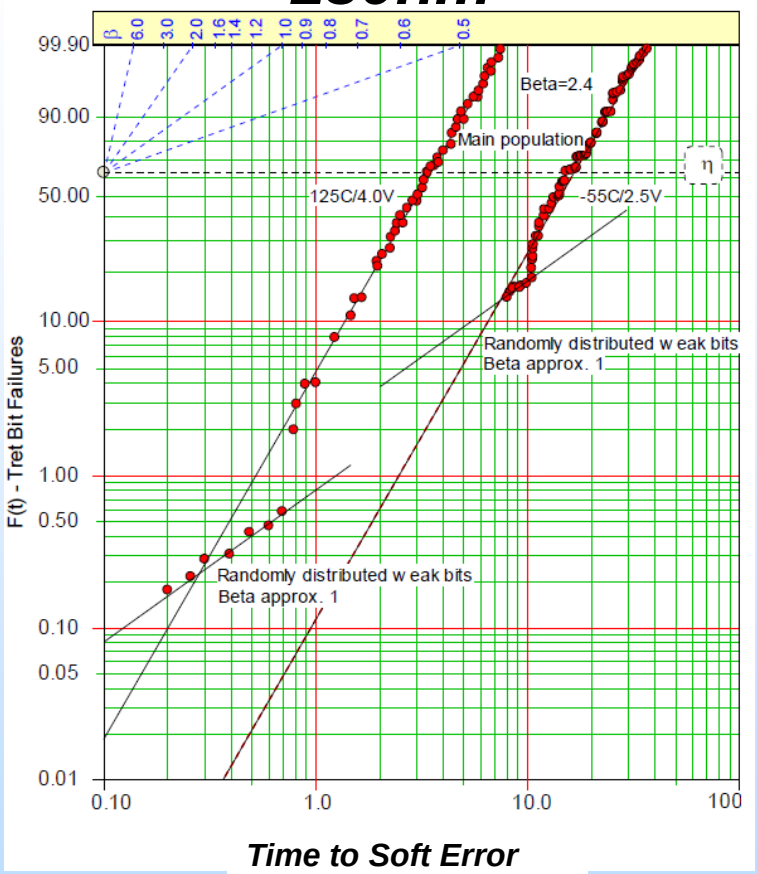


90nm T-NT/Weibull Initial and 1,000 hr.
Tret Stress Plots at Fixed Temp.

Bit lifetime/retention after stress indicates population spreading and isolates impact of temperature or voltage stress.

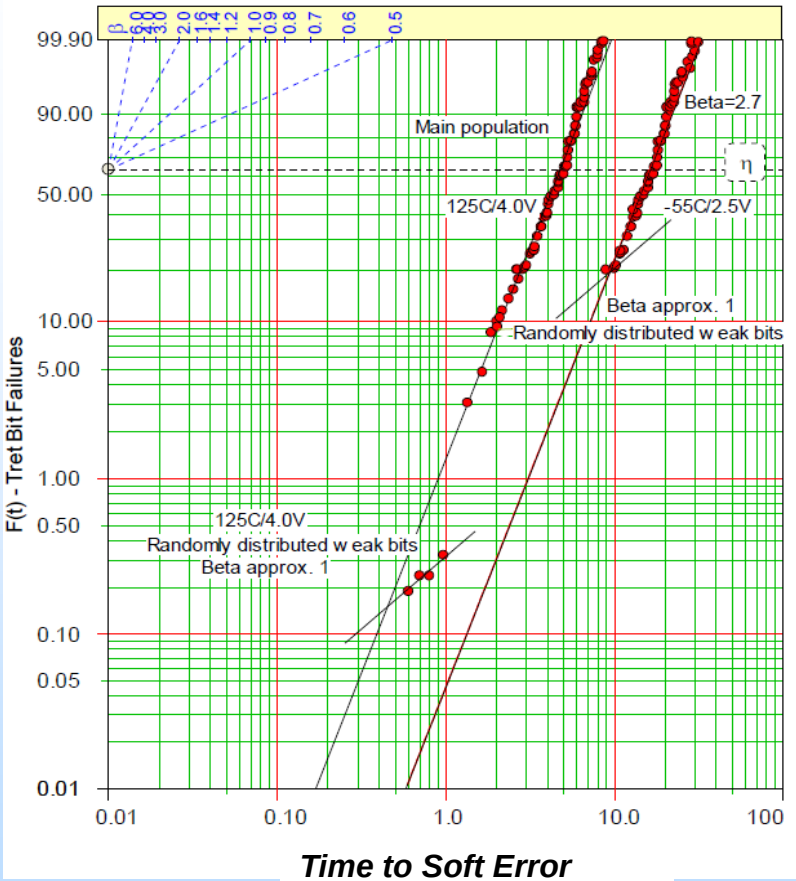
Comparison of DRAM Generations

130nm



Time to Soft Error (1,000 hrs.) – Secs.

90nm

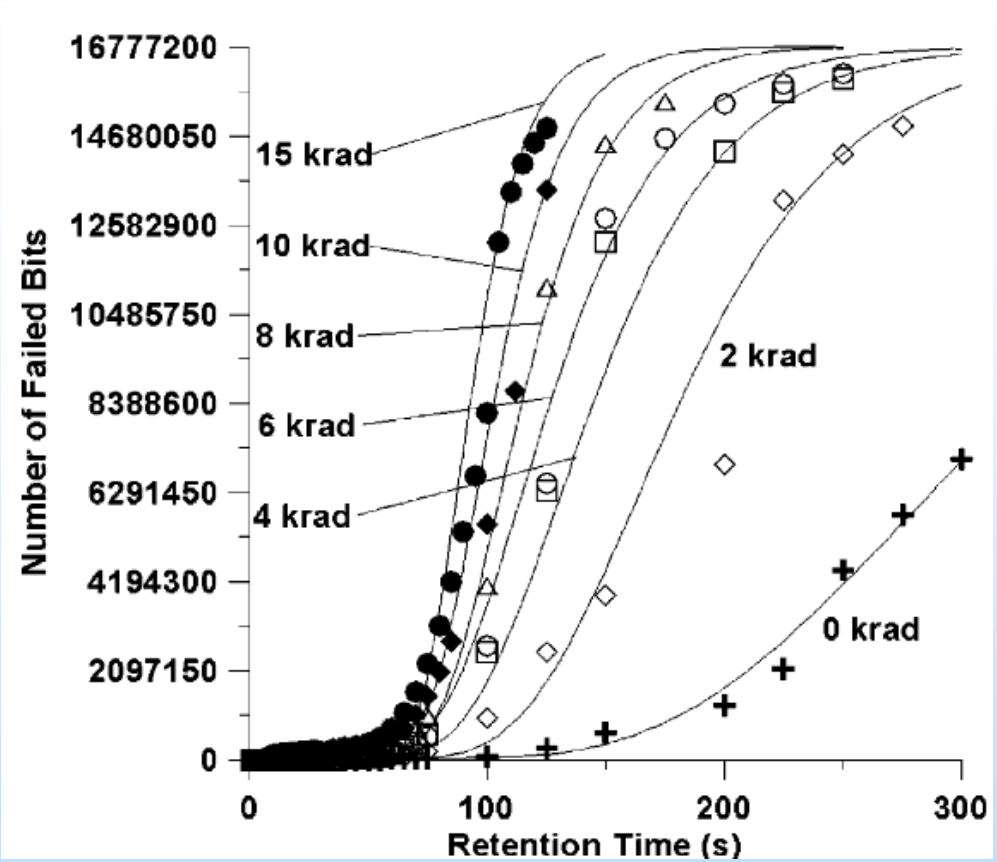


Time to Soft Error (1,000 hrs.) – Secs.

The main population at 90nm is tighter than at 130nm. Also the margin in weakest bits is improved at 90. This sort of trend is expected to continue to smaller feature sizes.

Total Ionizing Dose effects on DRAM

- TID from Cobalt-60 is used to simulate the proton TID contribution.
- Effect is shown on retention time (T_{ret}) at right.
  - Tret is the time between refreshes of a DRAM cell.
  - Entire distribution shifts to shorter retention time. (All cells become more leaky.)
- But proton effects are more localized.
  - Proton events lead directly to degradation of leakage current and premature data loss.

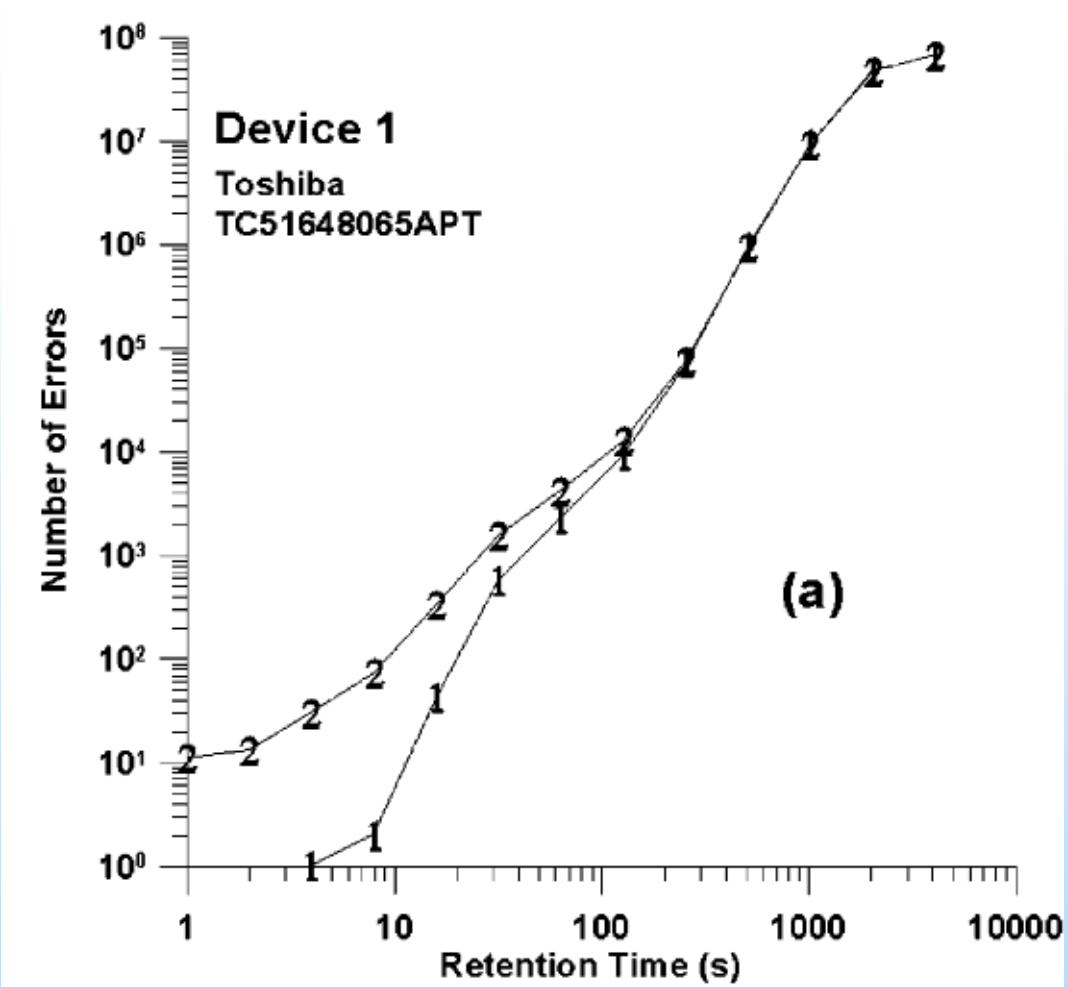


Scheick Et.Al, IEEE TNS 2000

TID from Co60 leads to reduction in retention time for all cells. Protons in space cause different effects.

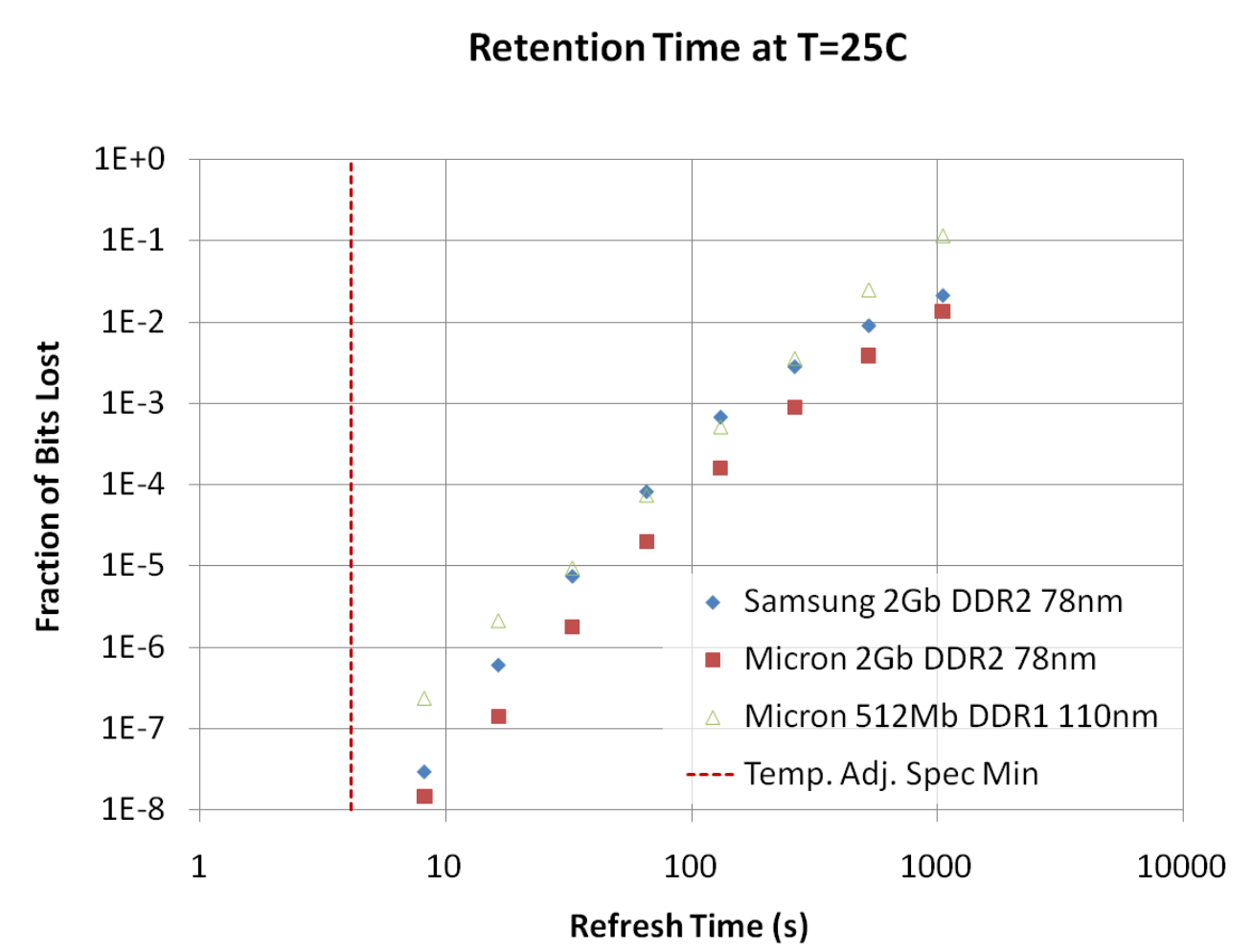
Proton Effects on DRAM Cells

- **Protons and heavier particles create a weak "tail" where the first failures are the ones that experienced the most catastrophic interactions.**



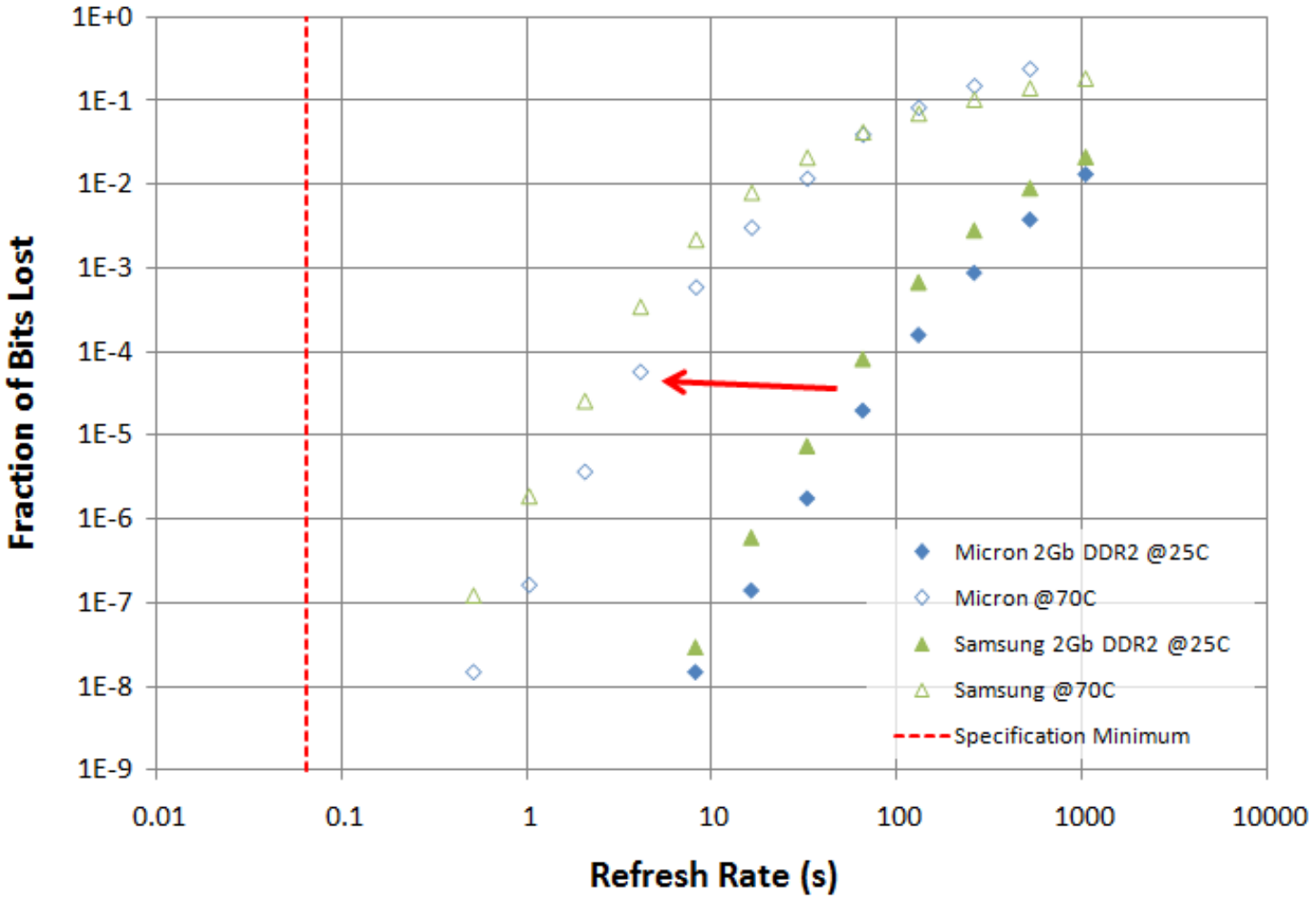
Protons are more appropriate for reliability testing because they are space-like and cause "weak" bits.

Preliminary Results at 25C



Validation of test system

Temperature Effect on Retention Time



Elevated temperature results in much faster data loss – this effect drives datasheet refresh requirement.

DDR Results Summary

- DDR1/DDR2/DDR3 are built of DRAM cells (cell has 1 T, 1 C, and leaks charge). The structure of these cells directly impacts the reliability concerns as a function of scaling.
- NEPP has investigated DRAM cells in the 90-130nm range, and is presently investigating 78nm. In the future this will be extended to 50nm (DDR3).
- Testing has shown very little impact of voltage stress.
- Temperature stress effects have shown significant impact on cell retention time, driving T_{ret}.
- Users of DRAM devices will gain significant margin by running with a faster refresh than 64ms, and by operating significantly below specification maximum temperature.
- Optionally, fault tolerance (such as EDAC) may be used to fix true random errors and failed bits.
- Additional reduction of DRAM reliability due to radiation effects is currently underway.

Plans (FY10/11) – 1 of 3

- Examine temperature stress impact on wear out
- Examine voltage stress (if regulation allows)
- Examine radiation effects
  - Planning to expose test devices to proton radiation – this will add a distribution of weakened bits to each device and is expected to drive first failure statistics.
- Full test matrix currently calls for, on one manufacturer
  - 3 devices for 25C stress, no protons
  - 3 devices for 25C stress, with protons
  - 3 devices for 85C stress, with protons
  - 3 devices from the other manufacturer for 25C stress
- If possible, this matrix may be expanded, or further testing may be delayed till 2011

Stress testing of DDR2 devices for rest of FY2010

Plans (FY10/11) – 2 of 3

- **Extend DDR2 Study**
  - **Expand test points to cover more combinations of temperature, voltage, and proton dose.**
  - **Expand manufacturer list.**
- **Start DDR3 study**
  - **Includes hardware development for modern devices**
  - **Gets the DDR study down below 50nm**
- **Other sub 65nm devices**
  - **Examine options for obtaining 45nm and lower devices (i.e. 32nm flash, 45nm SRAM or logic structures)**
  - **Determine failure rates for ring oscillators, SRAMS and other devices.**

For future years, DDR2 study will be extended to larger samples and more manufacturers. Will also test DDR3 (50nm). Study will also cover sub 65nm devices.

Plans (FY10/11) – 2 of 3

- **Improve Guideline**
  - **Extend to cover more technology types**
  - **Describe improving margin and fault tolerance methods**
- **Extension of Modeling efforts**
  - **Adding radiation failure to modeling effort (with proton radiation as initial goal for data source).**
  - **Expands model efforts to include more complete space environment. – Specifically targeting methods to predict FIT rate for different temperature, voltage and radiation environments.**
  - **Cells will be exposed to protons and then stressed for 1000 hours. By using multiple temperatures it will be possible to extract activation energy for bit populations with various soft error response curves.**