The NASA Electronic Parts and Packaging (NEPP) Program

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NASA/GSFC
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Unclassified

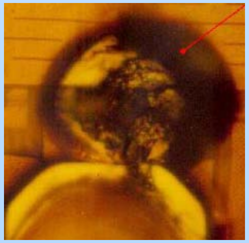
Outline

- Overview of NEPP
  - Who we are and what we do
  - Technology and NEPP
  - Knowledgeshare
  - Collaborations
  - Consortia/Universities
- FY12 Tasks
  - NEPP Technology Plans
- Recent Concerns
  - Class Y Advanced Package Qualification
  - Hermetic Seal Testing
  - X-ray Inspection and Radiation Degradation
  - Field Programmable Gate Array (FPGA) Radiation Update
- Summary

NEPP Introduction

- NEPP is the agency's only multi-disciplinary program dedicated to the safe utilization of integrated circuits and related technologies in the space environment.
- NEPP bridges the assurance and engineering needs of the agency and provides both focused research on electronics radiation and reliability in addition to acting as the agency voice in the development and implementation of government and industrial qualification and test standards.
- Three prime technical areas:
    - *Parts (die) Reliability, Device Packaging Reliability, and Radiation Effects on Electronics*
- NEPP has provided agency support for >20 years
    - 7 NASA Centers and JPL actively participate

Electrical overstress failure in a commercial electronic device



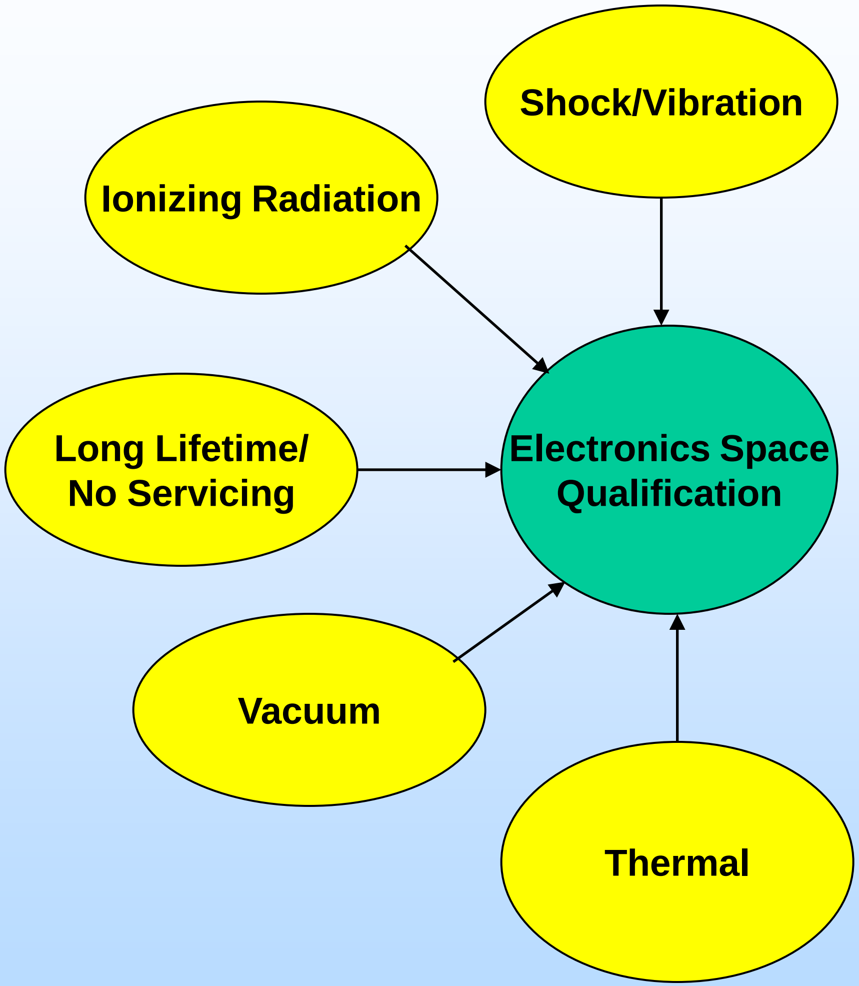
NEPP Works Two Sides of the Equation

- **Assurance**
  - *Issues applicable to space systems being designed and built (i.e., currently available technologies)*
  - Examples
    - Cracked capacitors
    - Power converter reliability
  - Communication infrastructure
    - NASA Electronic Parts Assurance Group (NEPAG)
  - Audit and review support

- **New electronics technology**
  - *Issues applicable to next generation space systems in conceptualization or preliminary design*
  - Examples
    - State-of-the-art commercial
    - High performance electronics
  - Collaboration with manufacturers and government programs for test, evaluation, and modeling
  - Development of new tools

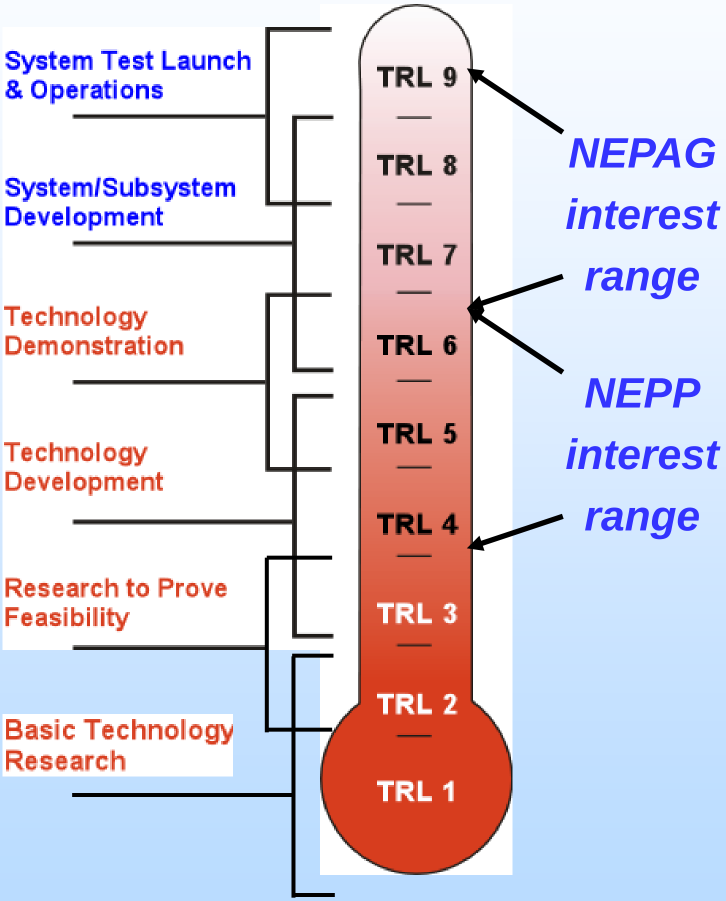
Qualifying Electronic Technologies
NEPP Perspective

- Electronics for space face hazards well beyond those of terrestrial/commercial
- Qualification requires repeatable and statistically significant testing over relevant environments to ensure mission success
- NEPP provides the basis for understanding the "how to's" for electronics qualification
- Why not strictly commercial?
  - Previous independent review/testing has repeatedly shown discrepancies that would impact reliable usage in space



Insertion of New Technologies – NEPP/NEPAG Focus

- NASA mission timeframes rarely allow for a technology development path
- For 2015 launch, technology freeze dates are likely 2012 or earlier
  - *May be time to qualify (test) a device, but may not be time to develop/validate a new technology solution!*
- Technology development and evaluation programs need to be in place prior to mission design
  - *Strategic planning for/by NEPP on technologies is critical*



NASA Technology Readiness Levels (TRLs)

Sample NEPP Technology Challenges

Can we "qualify" without breaking the bank?

Device Architectures
-system on a chip
-interconnects
-power distribution
-high frequencies
-application specific results

Silicon
-<65 nm CMOS
-new materials such as CNT

Packages
-Inspection
-Lead free
-How to test generically

Connectors
-higher-speed, lower noise
-serial/parallel
-ruggedized, electro-optic

Passives
-Embedded
-Higher performance
-Hybrids

Power Architectures
-distributed architecture
-thermal modeling
-stability

Board Material
-thermal coefficients
-material interfaces

Related areas (non-NEPP)

Design Flows/Tools
-programming algorithms, application
-design rules, tools, simulation, layout
-hard/soft IP instantiation

Workmanship
-inspection, lead free
-stacking, double-sided
-signal integrity

Knowledgeshare

- NEPP success is based on providing appropriate guidance to NASA flight projects
  - Interaction with the aerospace community, other government agencies, universities, and flight projects is critical.
- NEPP utilizes
  - NEPP Website: http://nepp.nasa.gov
  - NEPP 3rd Annual Electronics Technology Workshop (ETW): Week of June 11th 2012
    - HiREV (National High Reliability Electronics Virtual Center) Review Meeting to be held in conjunction
  - NEPP-hosted FPGAs for Space Workshop Aug 21-23, 2012
  - Standards working groups
  - Telecons
  - Documents such as Guidelines, Lessons Learned, Bodies of Knowledge (BOKs)

Collaboration

- **"Promote enhanced cooperation with international, industry, other U.S. government agency, and academic partners in the pursuit of our missions." –** ***Charles Bolden, NASA Administrator***
- **NEPP has a long history of collaboration. Examples include:**
  - **Direct funding from DoD**
    - **DTRA and NRO as well as in-kind efforts with AFRL, NRL, SNL, NAVSEA, etc…**
  - **Multiple universities**
    - **Vanderbilt, Georgia Tech, U of MD, Auburn University, …**
  - **Electronics manufacturers too numerous to mention!**
  - **International with ESA, JAXA, CNES, CSA, …**
- ***We work with the NASA flight programs, but do not perform mission specific tasks***

Consortia/Working Groups and Universities

- NEPP utilizes working groups for information exchange and product development
  - External examples:
    - JEDEC commercial electronics and GEIA G12 Government Users
  - Internal (NASA) examples:
    - DC-DC converters, point-of-load convertors, GaN/SiC, and connectors
- NEPP fosters university research in electronic parts
  - Examples
    - Radiation effects modeling at Vanderbilt University
    - Ultra-high speed electronics at Georgia Tech
- NEPP supports university-led electronics reliability research consortia

FY12 Sample Major Tasks/Challenges

- **Continued/new efforts in**
  - **State-of-the-art commercial device/technology evaluation**
    - **FPGAs (Virtex-5QV among others), Flash Memories, DDR2/3 Memories**
  - **Power conversion devices**
    - **Point-of-loads (POLs) – new market entries**
    - **Advanced/new power MOSFETs**
      - **SiC, GaN, new Si entries**
  - **Sub 65nm CMOS**
  - **Test guidelines: FPGAs, Flash, Solid State Recorders (SSRs)**
  - **Technology modeling, and so on**
- **Problem child continues**
  - **What to do with large area array package devices/packages?**
    - **Ex., Xilinx 1700+ pin CCGA or PBGA**
    - **Class Y dilemma**

FY12 NEPP Technology Efforts – Part 1

Radiation Hardness Assurance (RHA) and Guidelines

Low proton energy SEE test guide – Jonathan Pellish, NASA/GSFC

Ultra-ELDRS and ELDRS on Discretes – Dakai Chen, NASA/GSFC

IR Array Lessons Learned – Cheryl Marshall, NASA/GSFC

FPGA Standard SEE Test Guide – Melanie Berg, MEI Technologies – NASA/GSFC

Flash Memory Qualification Guide - Doug Sheldon, JPL

NVM Standard Radiation Test Guide – Tim Oldham, Dell – NASA/GSFC

NVM Combined Radiation and Reliability Effects – Tim Oldham, Dell – NASA/GSFC

DDR2 Combined Radiation and Reliability Effects - Ray Ladbury, NASA/GSFC

Updated Solid State Recorder Guidelines – Ray Ladbury, NASA/GSFC

Correlation of LASER to Heavy Ion Millibeam with FLASH Memories - Tim Oldham, Dell – NASA/GSFC

SEE Test Planning Guide – Ken LaBel, NASA/GSFC

Hydrogen and ELDRS – Philippe Adell, JPL

Devices

FPGA – Xilinx Virtex 5QV (SIRF) Independent SEE Testing - Melanie Berg, MEI Technologies – NASA/GSFC

FPGA – Commercial Virtex 5 SEE – Melanie Berg, MEI Technologies – NASA/GSFC

FPGA - Microsemi RTAX4000DSP SEE and ProASIC TID/SEE - Melanie Berg, MEI Technologies – NASA/GSFC

FPGA – Microsemi ProASIC Reliability – Doug Sheldon, JPL

Class Y (non-hermetic area array packaged device qualification) and related tests (Xilinx and Aeroflex packages/devices) – Doug Sheldon, JPL

FLASH Memory Radiation Effects – Tim Oldham, Dell – NASA/GSFC and Farohk Irom, JPL

Alternate NVM – MRAM/FRAM Reliability – Jason Heidecker, JPL

DDR2/3 Radiation Effects and Combined Effects – Ray Ladbury, NASA/GSFC

DDR2/3 Reliability – Steve Guertin, JPL

Newly Developed Si Power MOSFETs – Leif Scheick, JPL and Jean Marie Lauenstein, NASA/GSFC

System on a Chip (SOC) Radiation Testing – Steve Guertin, JPL

Newly Developed POLs Radiation and Reliability – Dakai Chen, NASA/GSFC and Philippe Adell, JPL

FY12 NEPP Technology Efforts – Part 2

CMOS Technology

IBM Technology and Radiation– Jonathan Pellish, NASA/GSFC w/ IBM, SNL, and NRL

INTEL Technology and Radiation (22nm FinFET processor – TID/Dose Rate) – Ken LaBel, NASA/GSFC w/INTEL, NAVSEA Crane

Tower Jazz Radiation Testing – Jonathan Pellish, NASA/GSFC and Melanie Berg, MEI – NASA/GSFC

Lyric Semiconductor Radiation – Jonathan Pellish, NASA/GSFC

Complex CMOS Device SEE Modeling – Vanderbilt University and Melanie Berg, NASA/GSFC

Physics-Based Modeling for SEE - Vanderbilt University

CMOS Radiation Testing TBD Others: TI, ON, Cypress, STM

III-V, Widebandgap, and RF

90nm SiGe Radiation Effects (IBM 9hp) – Georgia Tech and Paul Marshall, NASA/GSFC – Consultant

SiC and GaN Power Device Radiation Testing – Megan Casey, NASA/GSFC and Leif Scheick, JPL

RF Device Screening Practices (Reliability) – Mark White, JPL

SiC and GaN Power Device NASA Working Group – Leif Scheick

SiC and GaN Reliability Testing – Richard Patterson, NASA-GRC

Miscellaneous SiGe Device Radiation Testing – NASA/GSFC

TBD GaAs HEXFET Radiation – NASA/GSFC: We are tracking ESA research and determining applicability

FY12 NEPP Technology Efforts – Part 3

Qualification and Packaging

Class Y related packaging tests CCGA/PBGA, underfill, etc… – Doug Sheldon, JPL (w/many others)

Cryogenic Connector Failure Analysis – NASA/JPL

Body of Knowledge (BOK) documents on multiple packaging-related areas (TSV, 3D packages, X-ray and Workmanship, etc) – NASA/JPL

BME, Tantallum, and Polymer Capacitor Reliability/Screening – NASA/GSFC

DC-DC Converter NASA Working Group – John Pandolf, NASA/LaRC

NASA Connectors Working Group – Carlton Faller, NASA-JSC

Other

Infrared focal plane array lessons learned – Cheryl Marshall, NASA/GSFC

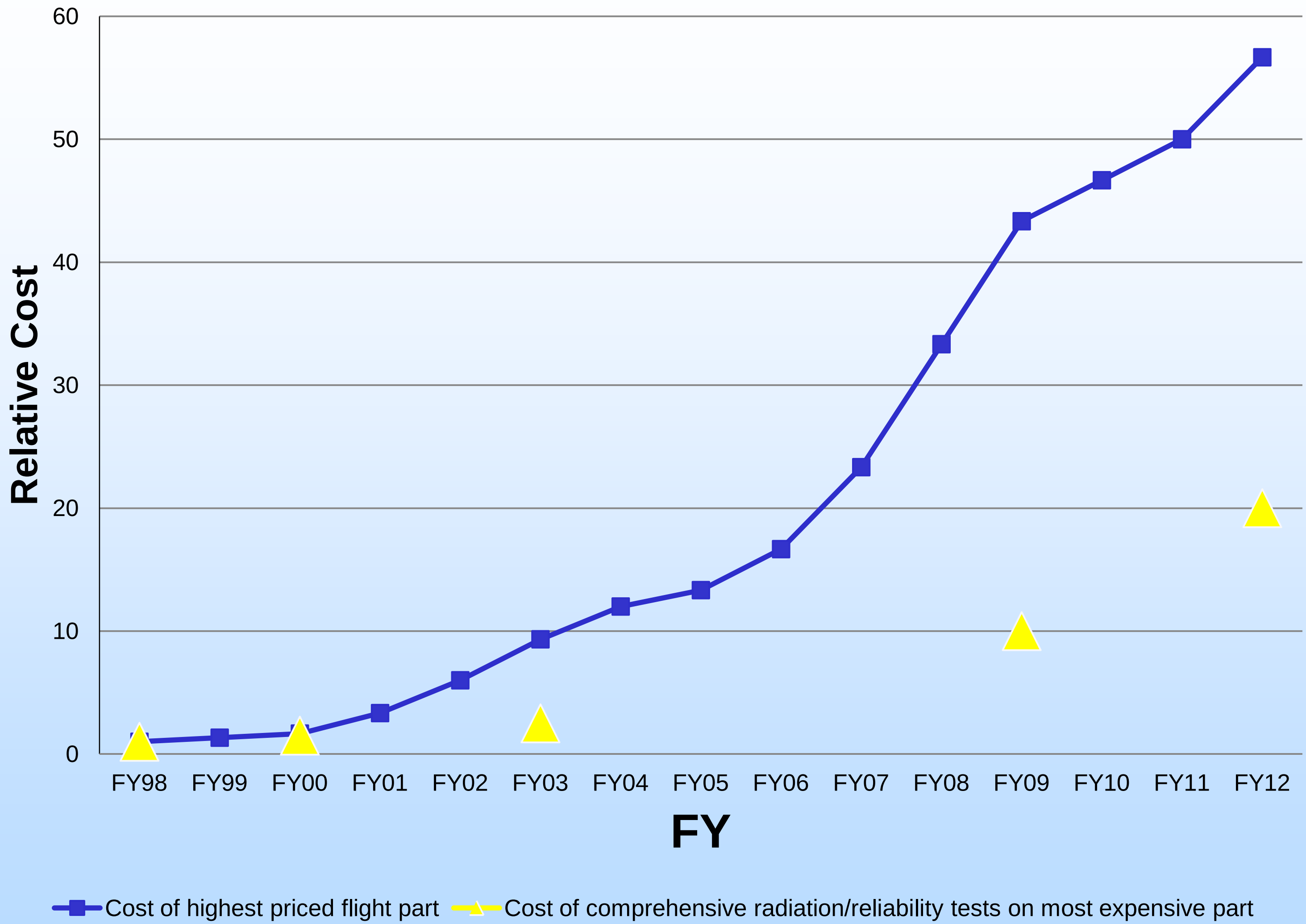
Development of SEGR Power MOSFET predictive technique – Jean Marie Lauenstein, NASA/GSFC

SEE Failures and Results Related to DC-DC Converter Design– Robert Gigliuto, MEI Technologies – NASA/GSFC

Point of Load NASA Working Group – Dakai Chen, NASA/GSFC

Optoelectronic Connectors and Transceivers – Melanie Ott, NASA/GSFC

Estimated Test/Parts Costs Normalized to FY98



Bottom line:

Costs have risen significantly, unfortunately NEPP budget hasn't!

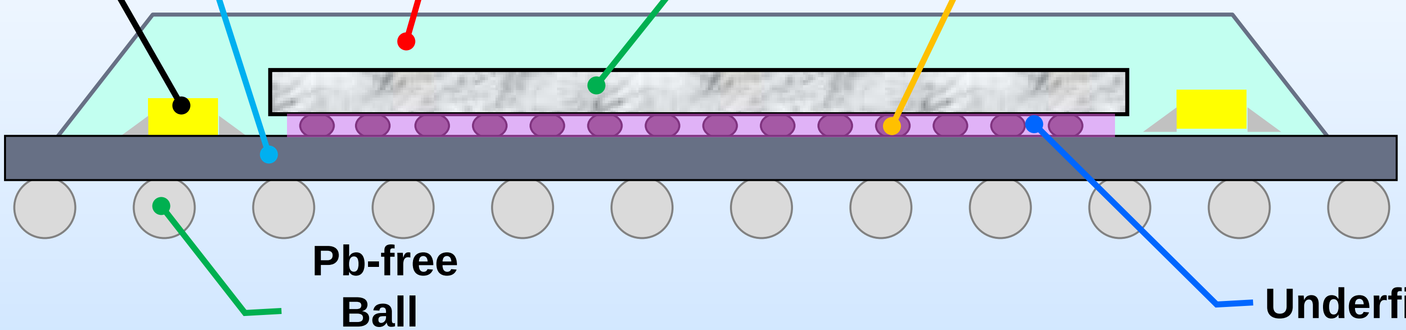
To be presented by Ken LaBel at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.

Packaging Challenges

- I/O s, increasing number, decreasing pitch
- Heat Dissipation, especially in space
- Manufacturability
- Materials
- Mechanical
- Installation
- Testability
- Inspectability
- Space Environment
- RoHS (Pb-free)
- Examples
  - Plastic Ball Grid Array (PBGA)
  - Ceramic Column Grid Array (CCGA)

Lunar Reconnaissance Orbiter (LRO), Launched with LCROSS, June 18,2009

Commercial, Non-hermetic Package (PBGA)



Design Drivers:
- High I/O count
- Large die
- Environmental protection
- Performance/Speed
- Ancillary parts

Commercial Drivers:
- Low cost
- High volume
- Limited life
- Automated installation
- Compact

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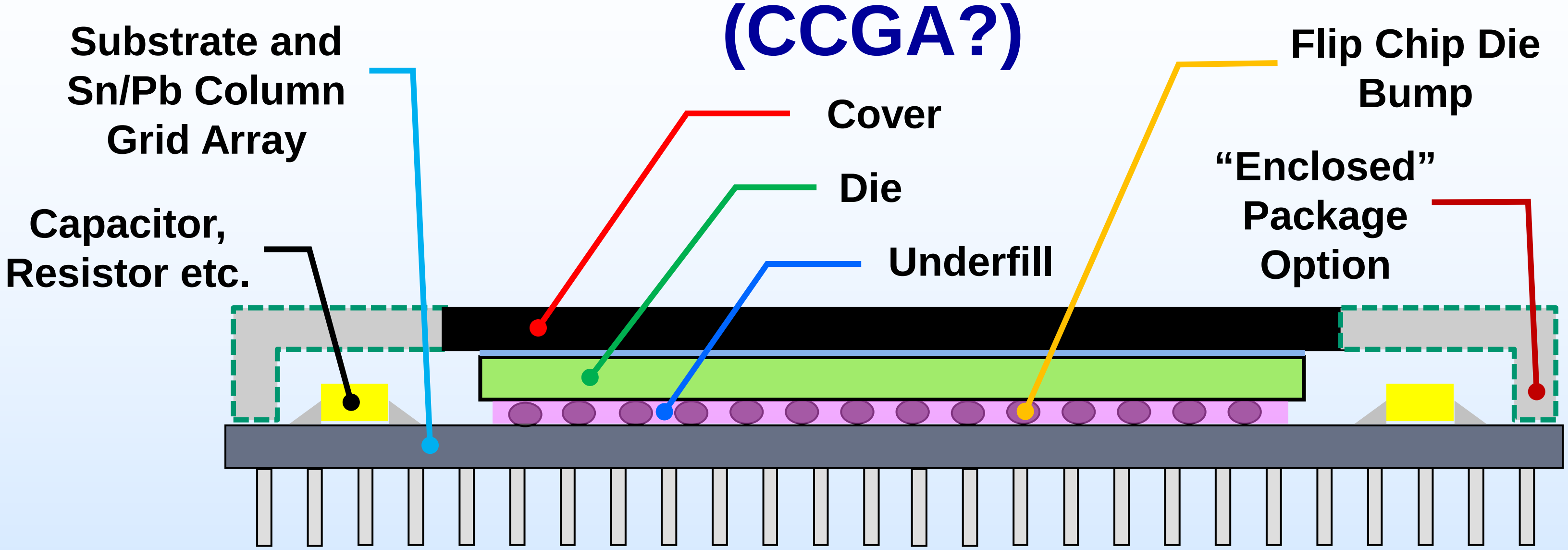
Non-hermetic Package, With "Space" Features (CCGA?)



Space Challenge	Some Defenses
Vacuum	Low out/off-gassing materials. Ceramics vs polymers.
Shock and vibration	Compliant / robust interconnects - wire bonds, solder balls, columns, conductive polymer
Thermal cycling	Compliant/robust interconnects, matched thermal expansion coefficients
Thermal management	Heat spreader in the lid and/or substrate, thermally conductive materials
Thousands of interconnects	Process control, planarity, solderability, substrate design
Low volume assembly	Remains a challenge
Long life	Good design, materials, parts and process control
Novel hardware	Test, test, test
Rigorous test and inspection	Testability and inspectability will always be challenges

Class Y - Current Status

- Class Y is a new addition to MIL-PRF-38535, microcircuits for space grade parts in non-hermetic packages
- Class Y is being added to the Appendix B, “Space Application”
- The Engineering Practices (EP) Study conducted by the Defense Logistics Agency, Land and Maritime, Document Standardization Unit (DLA-VA) has been completed. They have issued the final report.
- **DLA hosted a meeting April 12-13, 2012 to finalize the Class Y requirements.**

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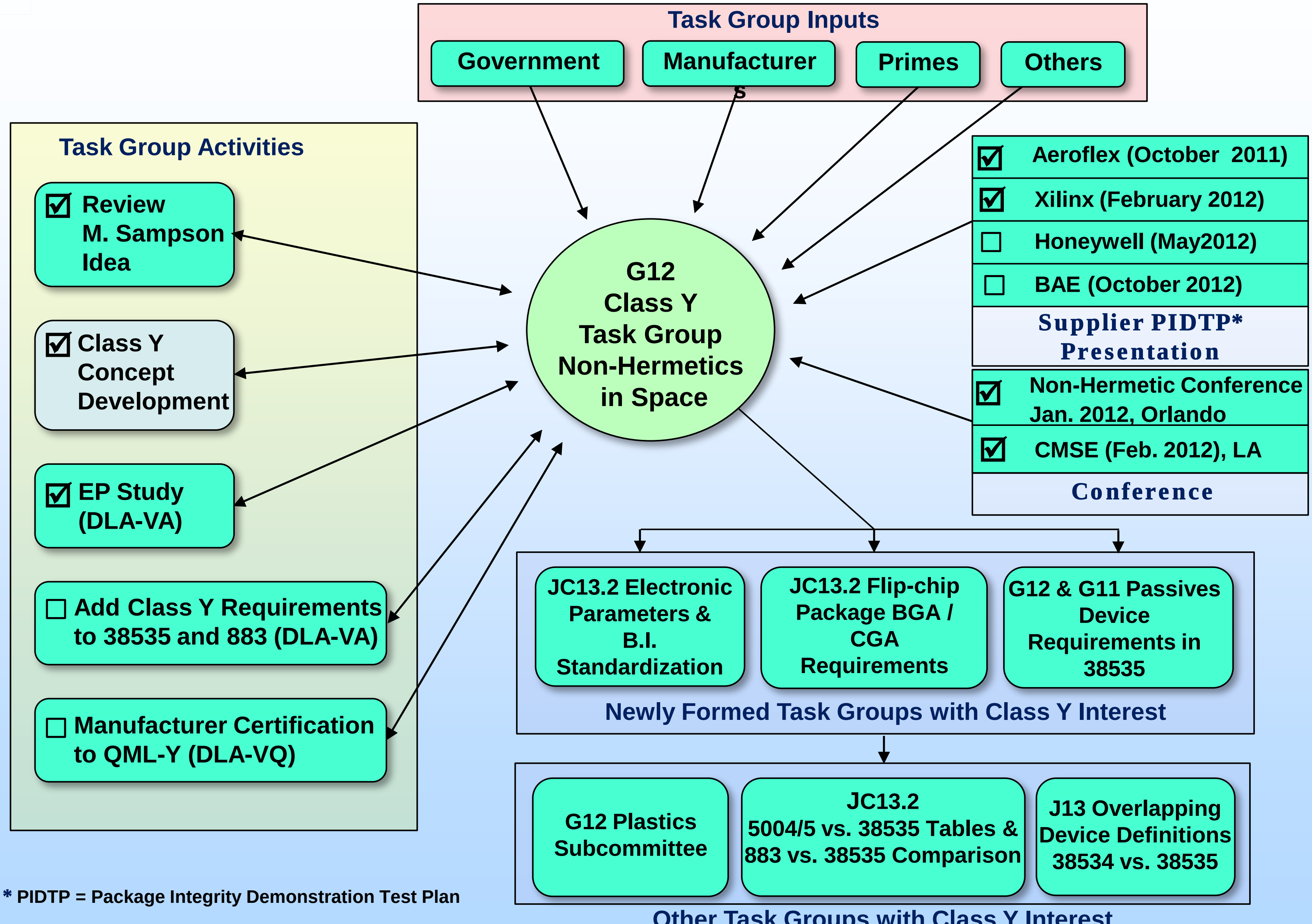
Infusion of New Technology into the QML system Road to QML-Y Flight Parts Procurement

- **Major Milestones:**
  - ☑ G12 approval of TG charter
  - ☑ G-12 Class Y Task Group to develop requirements
  - ☑ G12 approval for DLA-VA to commence EP study
  - ☑ DLA-VA to conduct EP study
  - ☑ DLA-VA to release "final" report
  - ☐ DLA-VA to update 38535 and 883 with Class Y requirements
  - ☐ DLA-VQ to begin audit of suppliers to Class Y requirements

  Users to procure QML-Y flight parts from certified/qualified suppliers

Infusion of New Technology into the QML system G12 Class Y Effort at a Glance



* PIDTP = Package Integrity Demonstration Test Plan

Closure of QML-Y (and related) Activities

Time T

(Goal: October 2012)

DLA-VA	DLA-VA Effort
Task Groups	JC13.2 Electronic Parameters & B.I. (Request priority for FPGAs, ASICs)
	JC13.2 Flip-chip Package BGA / CGA Requirements (CGA items)
	G12 & G11 Passives Device Requirements in 38535 (BMEs)
	G12 Plastics Subcommittee (CSAM)
	JC13.2 5004/5 vs. 38535 Tables & 883 vs. 38535 Comparison
	J13 Overlapping Device Definitions 38534 vs. 38535
Manufactures' PIDTP Class Y Data Presentations	Aeroflex (Completed October 2011)
	Xilinx (Completed February 2012)
	Honeywell (Scheduled for May 2012)
	BAE (Scheduled for October 2012)
Conferences	Non-Hermetic Packaging Technology Conference held Jan'12
	CMSE held Feb' 12

Hermetic Seal Testing Round-Robin Study (1 of 2)

- Both MIL-STD-750 TM 1071.9 and MIL-STD-883 TM 1014.13 call out He and radioisotope leak measurements as acceptable
- The purpose of the NEPP Round-Robin study is to compare repeatability of leak measurements between two He and a radioisotope testing instruments.
  - Comparing the actual leak rate values for parts with fine leaks.
  - Due to inherent characteristics of the He leak testers, gross leak will be compared as pass/fail

Participants and Equipment:

MSFC

- He leak detector (manufactured by Pernicka Corp).
- Kr85 radioisotope leak detector (manufactured by IsoVac Engineering Inc).

GSFC

- He leak detector (manufactured by Pernicka Corp).
- Possible incorporation of 3rd party verification

Hermetic Seal Testing Round-Robin Study (2 of 2)

Parts tested

- Three groups of parts. Each group contains:
  - 10 parts of same P/N that in the past have failed leak testing
  - 1 part of same P/N but delidded – used a control during bombing/testing to monitor He absorption/desorption
- Out of 10 parts in each group:
  - 5 parts are gross leakers
  - 5 parts are fine leakers

Procedure

- Parts tested with He leak detector at MSFC.
- Parts shipped to GSFC.
- Parts tested with He leak detector at GSFC.
- Parts shipped to MSFC.
- Parts tested with Kr85 radioisotope leak detector at MSFC*.

(*) Note: Kr85 radioisotope leak testing is done last due to shipment restrictions on parts with radiating above a specific limit. Parts therefore have to 'cool'.

TESTING CURRENTLY IN PROCESS

X-Ray Inspection and Radiation Degradation

- Studies performed 10 or more years ago focused on simple x-ray inspection and it's impact on radiation performance
  - Unless someone left the switch on, the accumulated additional total dose was trivial
- With more complex X-ray inspection techniques (think 3D and tomography) used on devices and printed wiring boards (PWBs), possibly at multiple stages of development cycle or counterfeit detection, the concern over radiation degradation has been reawakened.
- Caveats
  - Unlikely to be an issue for radiation hardened parts or parts that have sufficient radiation design margins (RDMs) for a mission.
  - Possibly an issue for more radiation sensitive devices with minimal RDMs.
    - Limited data has been taken measuring possible exposure doses
- Future?
  - Measure exposure levels for differing X-ray inspection machines
  - Develop a "rider" requirement for each part tracking accumulated dose?
  - Expose various types of electronics to X-rays and compare to gamma tolerance

FPGA Radiation Update

- FPGA Single Event Effects (SEE) Test Guideline
  - In internal release for review
- Radiation Tests Performed
  - SEE: Microsemi RTAX4000D
  - SEE: Microsemi ProASIC
  - TID: Microsemi ProASIC (to be presented at IEEE NSREC 2012)
  - SEE/Laser: BAE/Achronix Radrunner II (development vehicle)
- Upcoming Plans
  - Independent SEE Testing of Virtex 5QV (formerly called SIRF) and commercial Virtex 5
    - 1st Test Planned for early May
  - Combined TID/SEE on Microsemi ProASIC
  - FPGA TID Guideline (FY13 delivery)
  - FPGAs in Space Workshop

Summary

- **NEPP is an agency-wide program that endeavors to provide added-value to the greater aerospace community.**
  - **Always looking at the big picture (widest potential space use of evaluated technologies),**
  - **Never forgetting our partners, and,**
  - **Attempting to do “less with less” (static budget versus rising costs).**
- **We invite your feedback and collaboration and invite you to visit our website (http://nepp.nasa.gov) and join us at our annual meeting in June and FPGA Workshop in August at NASA/GSFC.**
- **Questions?**

Backups

NASA EEE Parts Assurance Group (NEPAG)

- Formed in 2000
- Weekly Telecons
  - International monthly
  - Typical participation ~ 35
  - Share knowledge and experience
  - Address failures, requirements, test methods
- Audit support
- Coordinate specification and standards changes

The NEPP Program in a Nutshell

Management

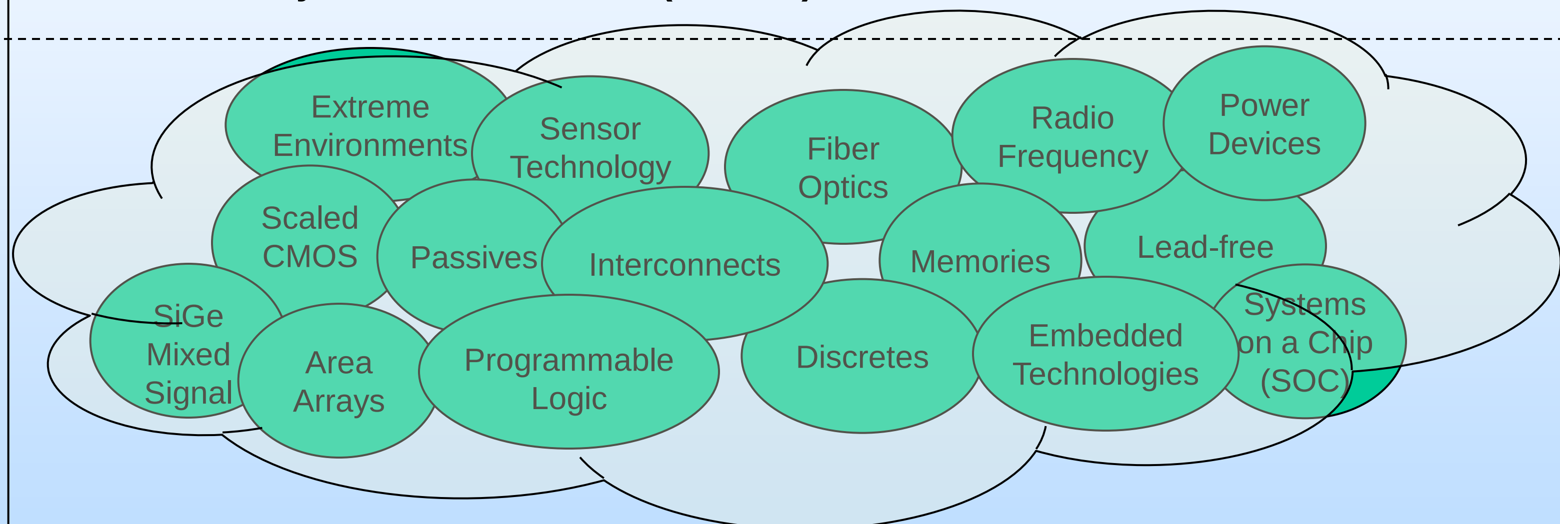
Ken LaBel - 561
Radiation Effects
Advanced Actives
NEPP Events

Mike Sampson - 300
NEPAG
Passives
Packaging

Core Elements

- Electronic Parts Reliability
- Radiation Effects
- Parts Assurance (NEPAG)
- Advanced Packaging
- Information Dissemination

Focus Technologies



Products/ Deliverables

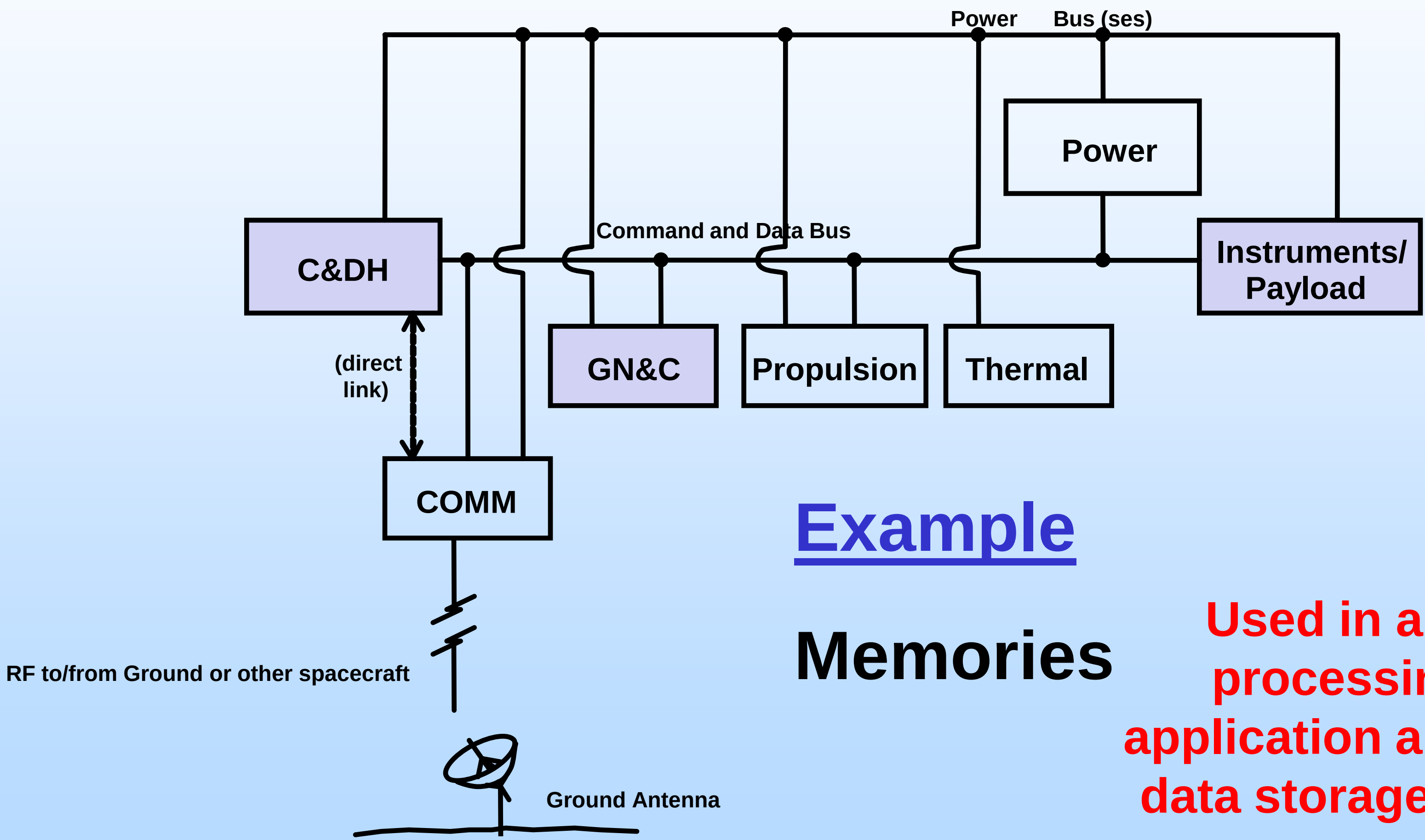
Guidelines
Specifications and Standards
Test Methods

Website Content
NASA Parts Selection List
Tools
Data

Technical Reports
Bodies of Knowledge
Conference Papers

Metric: 90% of NEPP Tasks should have NASA-wide Utility

Typical Spacecraft Electrical Architecture



Example

Memories

Used in any processing application and for data storage on a spacecraft.

GIDEP Safe Alert- A Part Issue

Distribution is not authorized outside of the GIDEP participant's organization.

GOVERNMENT - INDUSTRY DATA EXCHANGE PROGRAM

SAFE-ALERT

1. TITLE (Class, Function, Type, etc.)

Capacitor, Electrolytic Tantalum, Backward Installat
Hazardous Electrolyte Contaminant

4. MANUFACTURER AND ADDRESS

All Manufacturers
Wet Tantalum Electrolytic Capacitors

5. Va
7. Mi
9. Al

11. MANUFACTURER'S POINT OF CONTACT
Not Applicable

12. No

14. MFR. POC PHONE
Not Applicable

15. No

16. SUPPLIER
Not Applicable

17. No

19. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

During circuit card level testing at the NASA Goddar
failure (see Figure 1) of a wet electrolytic tantalum c
the failure, the capacitor case ruptured and the high
circuit card causing damage to the hardware which
persons were injured during this failure event nor du
contaminated flight hardware. The root cause of the
circuit card assembly. Wet electrolytic tantalum cap
sulfuric acid and are sensitive to reverse polarity ex
hardware were unaware of the acid burn hazard for

(See page 2 for continuation)

20. ACTION TAKEN/PLANNED

1. Ensure proper orientation (i.e., polarity) during i
through the implementation of robust quality assura
verification protocol with sign-offs to validate the co
marking on the circuit card, and the capacitor polari
powering up the circuit for the first time.
2. Wear appropriate personal protective gear whe
failure analyses (or other destructive physical analy
3. Adhere to the manufacturer and NASA-specific
properly limiting the reverse voltage, forward voltag

21. DATE MFR. NOTIFIED/ SUPPLIER NOTIFIED
Not Applicable

22. MFR./SUPPLIER RESPONSE
REPLY ATTACHED
Not Applicable
NO REPLY

(301) 286-2019 Jay.A.Brusse@nasa.gov

24. GIDEP REPRESENTATIVE
Mike Sampson

25. SIGNATURE

26. DATE
25 Jan. 2012

GIDEP Form 97-2 (September 2009)

Please refer to the complete distribution policy at the GIDEP member's website.

Expelled capacitor casing that was moved backwards. The capacitor negative end is still attached to the "+" board pad.

Capacitor positive end (internal elements) remaining on the board as it was installed backwards at the negative board pad.

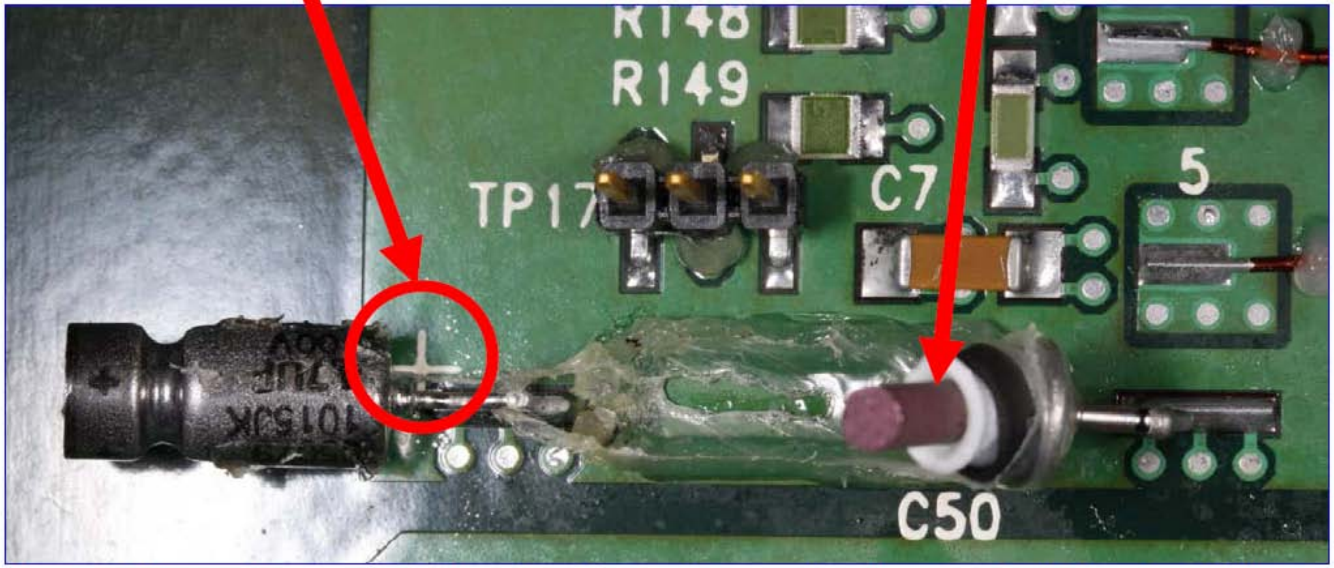


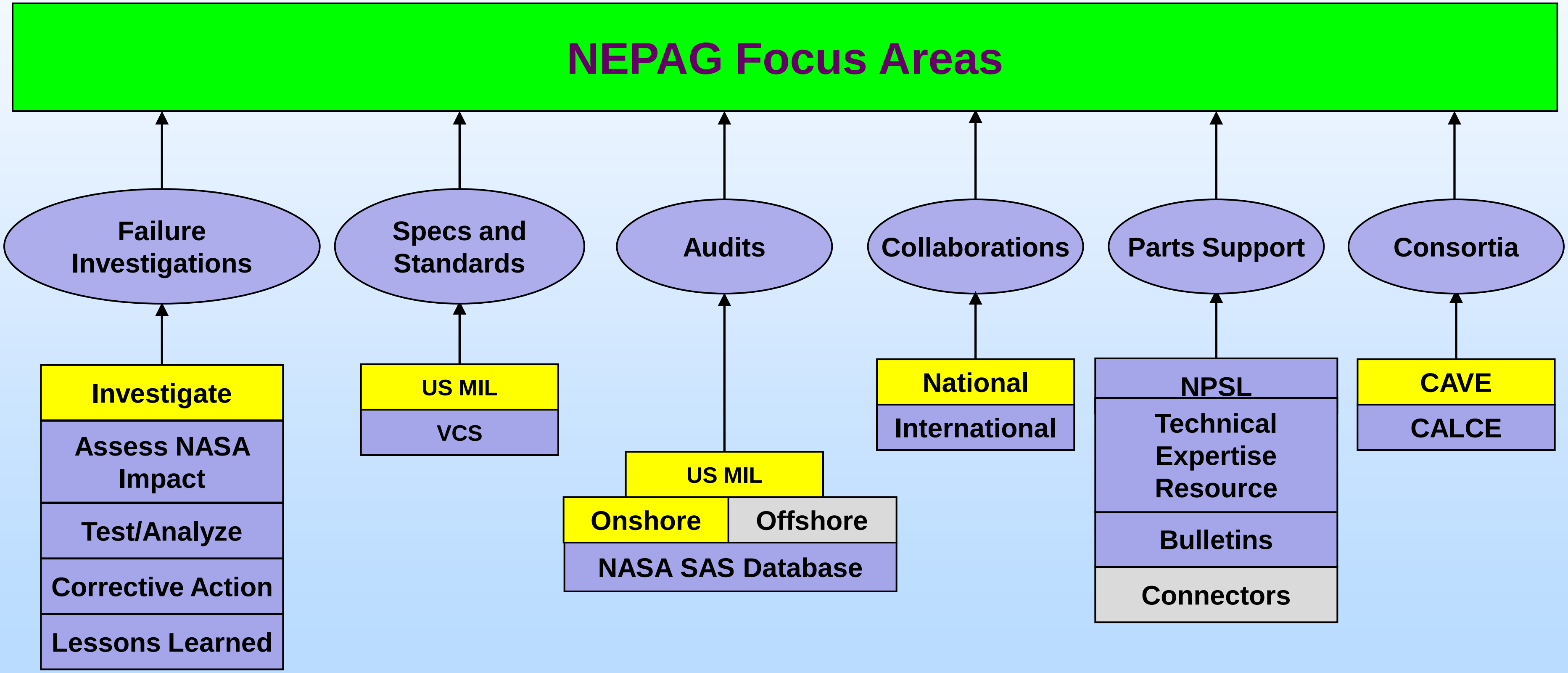
Figure 1. Failure residue of an exploded wet electrolytic tantalum capacitor at location "C50". Above the "C50" imprint are the remaining internal elements of the positive end of the capacitor which should have been installed at the board pad adjacent to the "+" indicator.

NASA Electronic Parts Assurance Group (NEPAG)

Core Areas are Bubbles; Boxes underneath are elements in each core

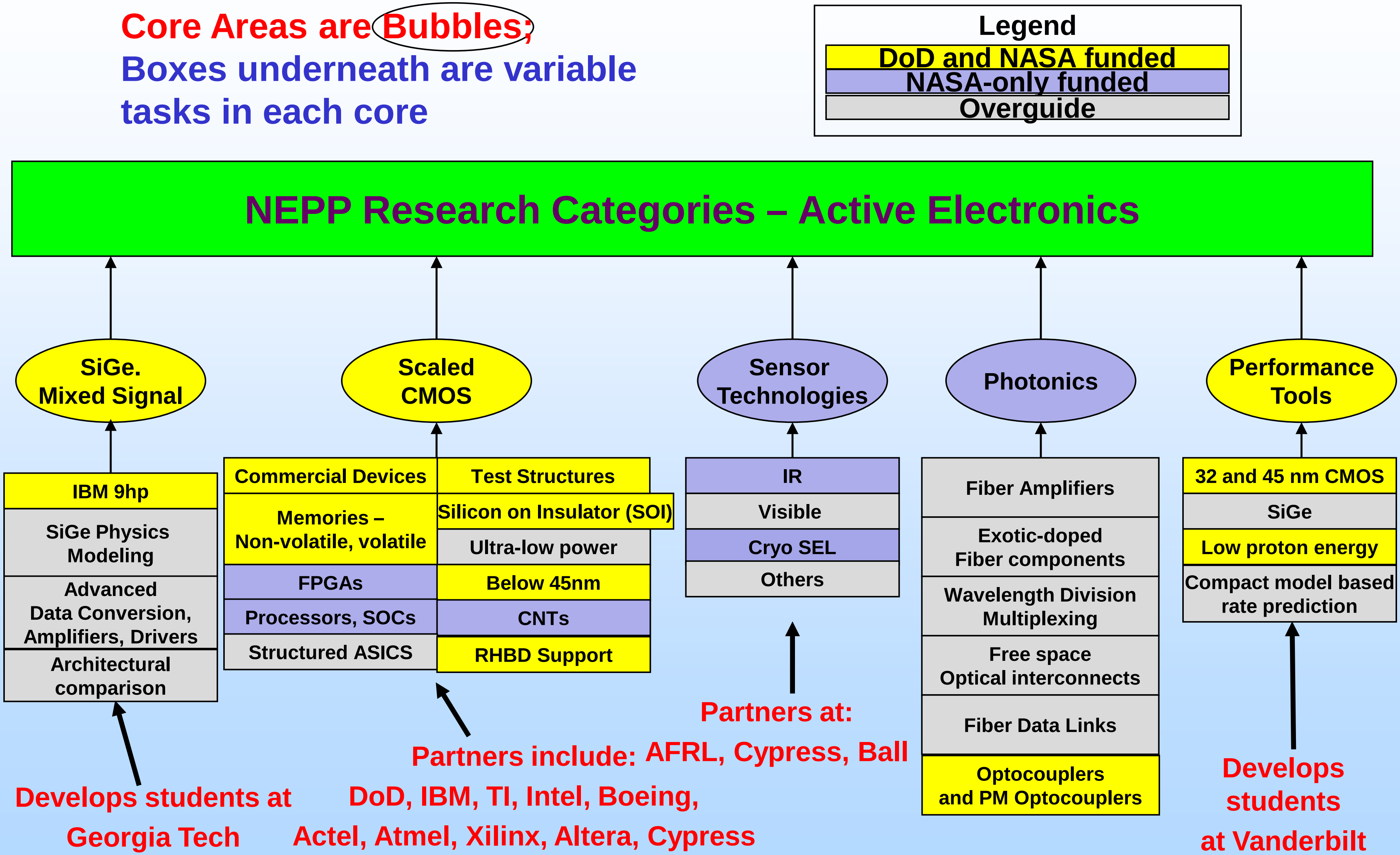
Legend

- DoD and NASA Funded
- NASA-only funded
- Overguide



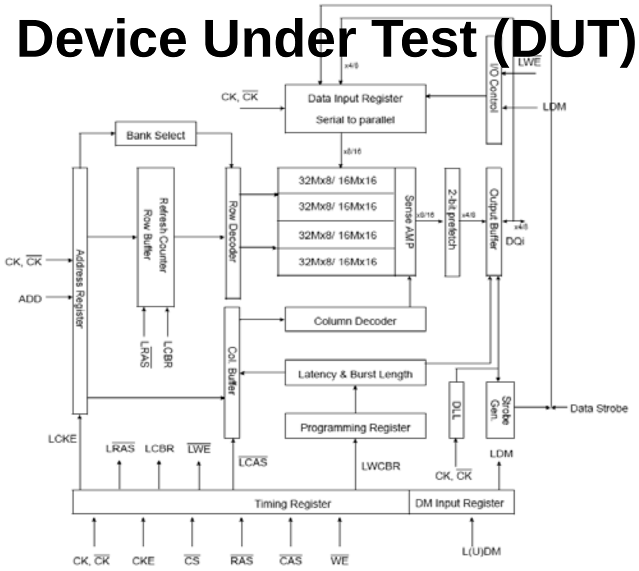
Sample FY12 Radiation Plans for NEPP Core (1)

Core Areas are Bubbles;
Boxes underneath are variable tasks in each core



Disclaimer:
Statistics and "Qualification"

Device Under Test (DUT)



Commercial 1 Gb SDRAM

-68 operating modes

-can operate to >500 MHz

-Vdd 2.5V external, 1.25V internal

Single Event Effect Test Matrix

full generic testing

Amount	*Item*
3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

66096 Hours

2754 Days

7.54 Years

Doesn't include temperature variations!!!

The more complex a device, the more application-specific the test results

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