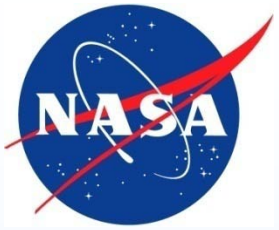
NEPP Electronic Technology Workshop
June 11-15, 2012

National Aeronautics
and Space Administration



Updated Solid State Recorder (SSR) Radiation Guidelines

Ray Ladbury

Radiation Effects and Analysis Group
NASA Goddard Space Flight Center
Greenbelt, MD 20771 USA

Introduction

- Solid-State Recorder (SSR) timeline
  - 1992—first use of solid state recorder
  - 2002—First radiation guidelines for SSR use (C. Poivey for NEPP)
  - 2012—Update of guidelines
- What's new in 2012?
  - Synchronous Dynamic Random Access Memories (SDRAMs) have dominated since late '90s; current generation uses 512 Mbit die
    - On-orbit data available for 64-Mbit, 256-Mbit and 512-Mbit generations
  - Next-generation will use 2nd generation Double-Data-Rate (DDR2) die
  - Memory organization has gone from x4 to x8
  - Word size increasing—32-bits is norm; some use of 64-bit
  - EDAC still dominant error correction technique
  - Decrease in # of SDRAM suppliers continues—lost Elpida this year
  - First commercial-FLASH SSR now available from Eads-Astrium

SDRAM Subtask

Description:

– *This is a continuation task for evaluating the effects of scaling (<100nm), new materials, etc. on state-of-the-art (SOTA) mass volatile memory (VM) technologies—mainly SDRAM. The intent is:*

– *To determine inherent radiation tolerance and sensitivities,*

– *Identify challenges for future radiation hardening efforts,*

– *Investigate new failure modes and effects, and*

– *Provide data to DTRA/NASA technology modeling programs.*

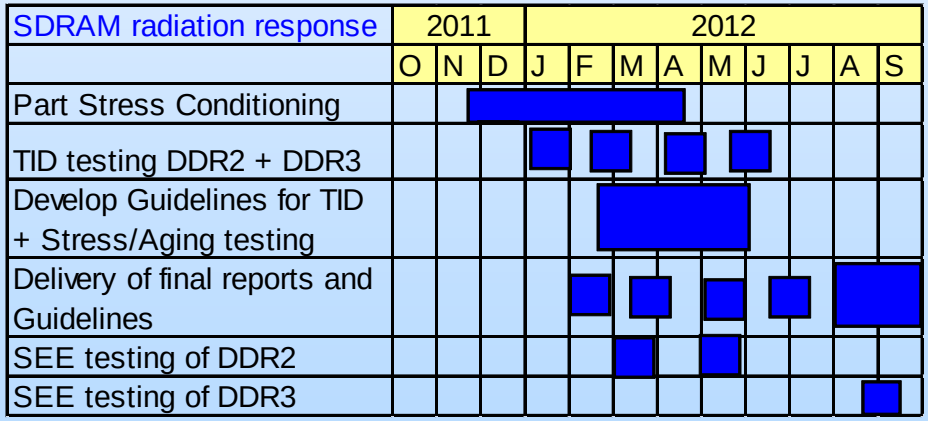
–*Testing includes total dose, single event (proton, laser, heavy ion), proton damage (where appropriate) and reliability. Test vehicles will include a variety of volatile memory devices as available, including DDR2 SDRAMs and commercial SRAMs… and DDR3 devices*

–*Emphasis for 2012 will be synergistic degradation resulting from aging and total ionizing dose (TID) response, but SEE testing also planned.*

FY12 Plans:

– *TID test structures*
  – *DDR2 and DDR3 SDRAM from Samsung and Micron*
  – *DDR2 SDRAMs from Elpida (courtesy of 3D Plus)*
  – *TID/reliability tests will use the new Triad Memory tester*
– *Test focuses*
– *Evaluate potential synergistic effects of TID and SDRAM aging*
  – *Use thermal and voltage acceleration methods*
  – *Evaluate degradation due to aging/stress*
  – *Compare TID response of stressed to unstressed parts*
– *SDRAM SEE response for current generation DDR2 and DDR3 SDRAMs if funding, tester capability and time allow.*

Schedule:



Deliverables:

-*Updated SSR Radiation Guidelines*

-*Updated guidelines for TID testing of SDRAMs taking into account wearout mechanisms*

- *Test reports*

-*Publications*

–*Effects of Bias, Electrical and Thermal Stress on DDR SDRAM Total Ionizing Dose Response*

–*NASA and Non-NASA Organizations/Procurements:*

–*Beam procurements: GSFC/REF, TAMU, LBNL*

–*Partners: 3D Plus, JPL, Micron, Samsung, BAE Systems*

Subtask lead: Ray Ladbury

Goals

- **Assess Current SEE Mitigation Techniques for SSRs**
  - **Current SSRs use SDRAM parts up to 512 Megabits (Mbits)**
- **Predict Whether Current Mitigation Techniques Adequate for Future SSR designs**
  - **Next Generation SSRs will use DDR2 SDRAMs**
- **Identify Trends and Challenges for Future SSRs**
  - **Candidate Parts and Vendors**
  - **Developments in Mitigation Techniques**
- **Assess Adequacy of Current Rate Estimation Techniques for State-Of-The-Art (SOTA) SDRAMs**
- **Update is about 90% completed**

Expected Impact to Community

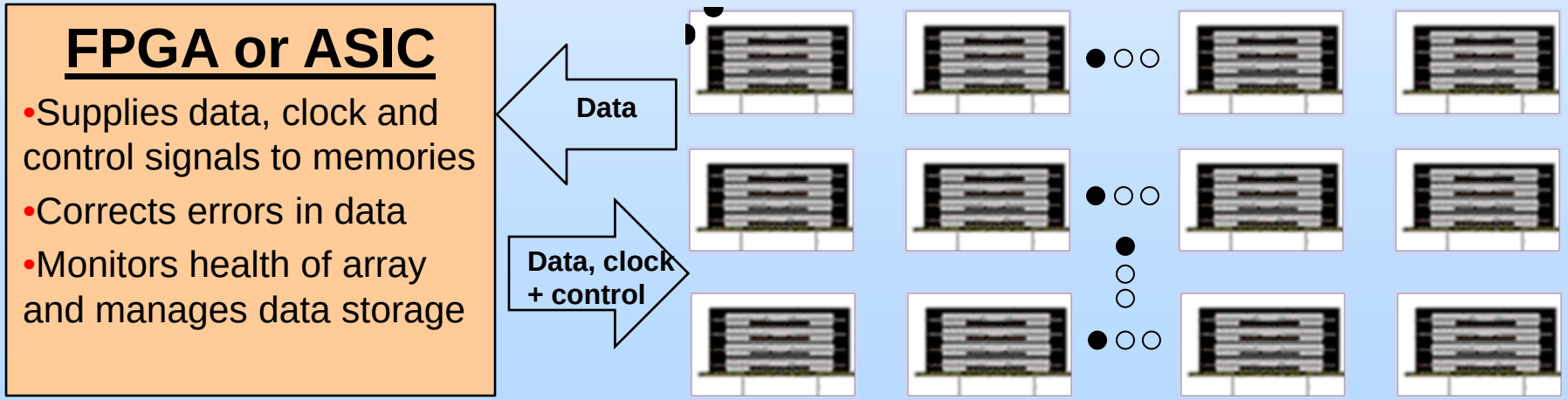
- **Increase confidence in SSRs**
  - **Validate test methods of SDRAMs for use in SSRs**
  - **Validate SEE mitigation Techniques in SSRs**
- **Identify Trends for SOTA SSRs**
  - **Anticipate new challenges**
- **Capture Lessons Learned**

Single-Event Effects by Consequence

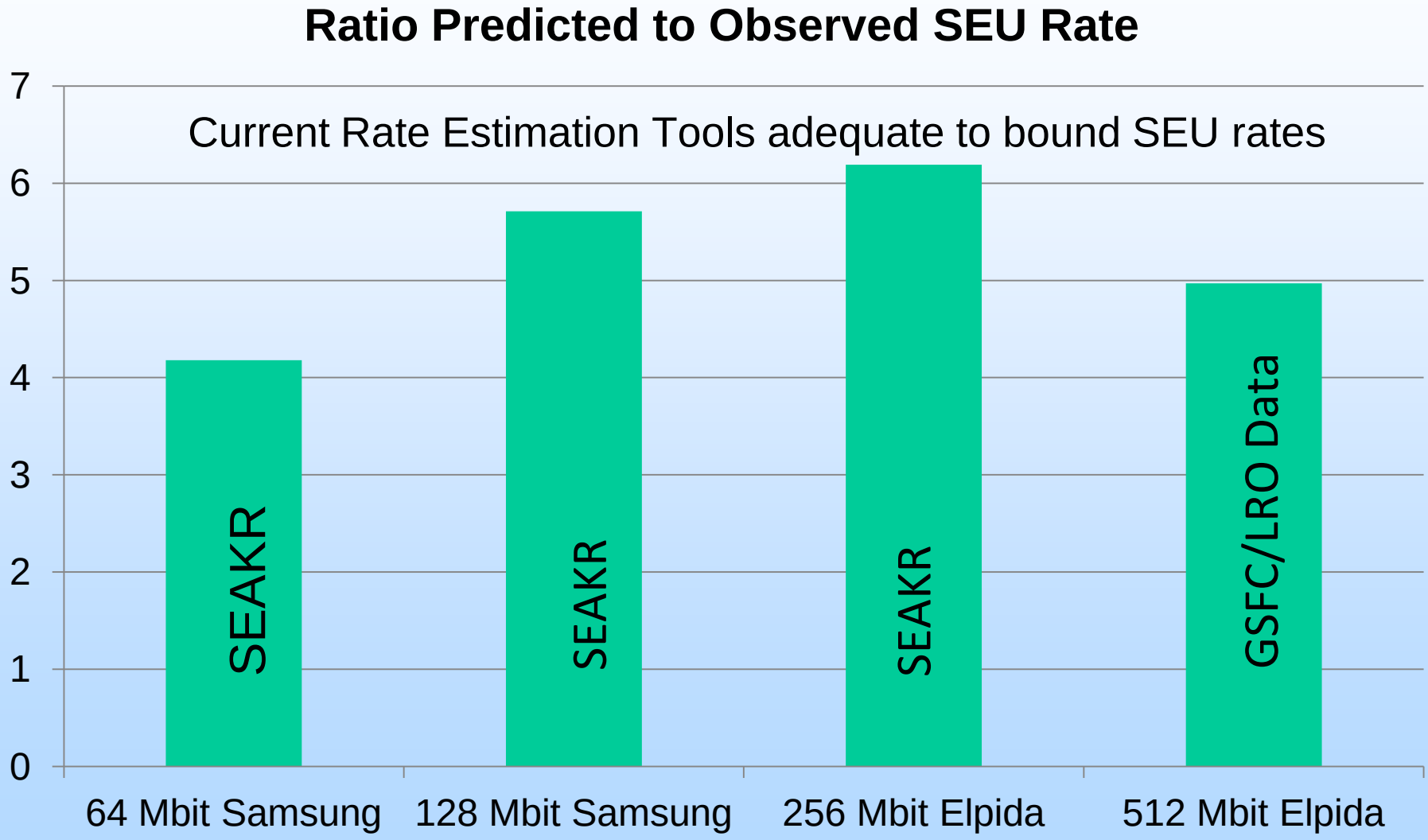
Radiation Risk	Consequence	Remediation	Impact to design
Destructive Single-Event Latchup (SEL)	Permanent loss of 1 die in memory array	Redundant die in array such that probability of meeting End-of-Life (EOL) requirements is high	Severe
Nondestructive SEL	Loss of all data on affected die/stack	Requires power cycle of affected die/stack for recovery	Moderate to severe
Single-Event Functional Interrupt (SEFI) requiring power cycle	Loss of functionality on affected die; Loss of most or all data on affected die/stacks	Requires power cycle of affected die/stack for recovery; EDAC may	Moderate to severe
Recoverable SEFI	Temporary loss of functionality; Loss of large amounts up to all data on affected die.	EDAC + Organzation of data words across independent die; FPGA programmed w/ ability to refresh mode registers/reset device	Moderate
Stuck Bits	Uncorrectable loss of data integrity in affected bits/symbols	EDAC can correct incorrect bit, but capability permanently degraded	Minor
Multi-Bit Single-Event Upset (SEU)	Correctable loss of data for multiple bits in same word	EDAC must have sufficient power to correct w/c MBU (usually no worse than w/c SEFI)	Moderate
Multi-Cell SEU	Multiple bits upset, but in different words	EDAC	Minor
SEU	single-bit upset	EDAC	Minor

Design Considerations

- Data stored in k-bit words, broken into n-bit symbols, 1 per part
- EDAC corrects m symbols
- If total symbol error rate = R, uncorrectable error rate~R^{m+1}
- Part with destructive SEL requires more die to meet EOL needs
- If SDRAM die are stacked, treat each stack as a "part"
  - Caveat—die in a stack have a common power supply, making it impossible to monitor overcurrent or cycle power to a single die.

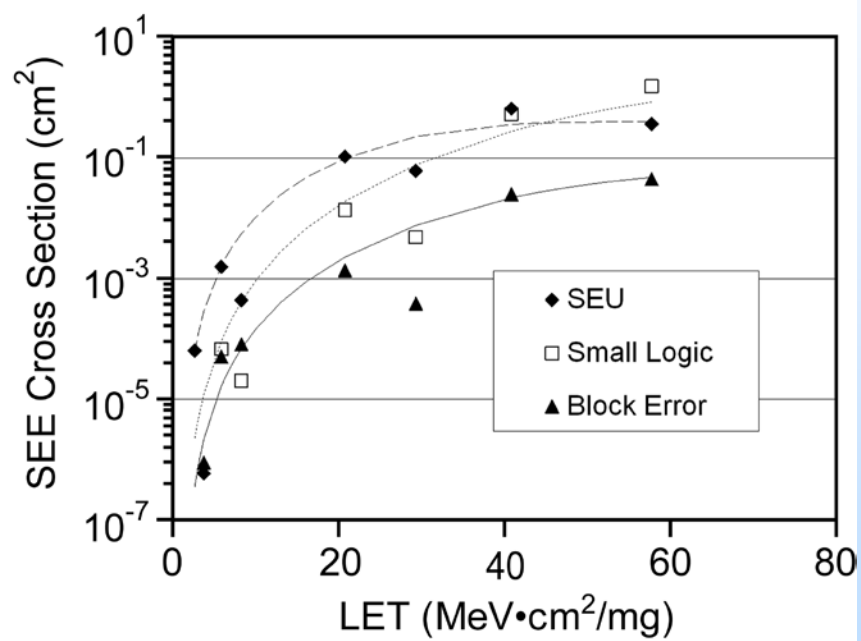


SSRs: The Current Generation



On-Orbit Data For LRO SSR

- SSR for Lunar Reconnaissance Orbiter (LRO) provides a check on predicted rates
  - >730000 device-days

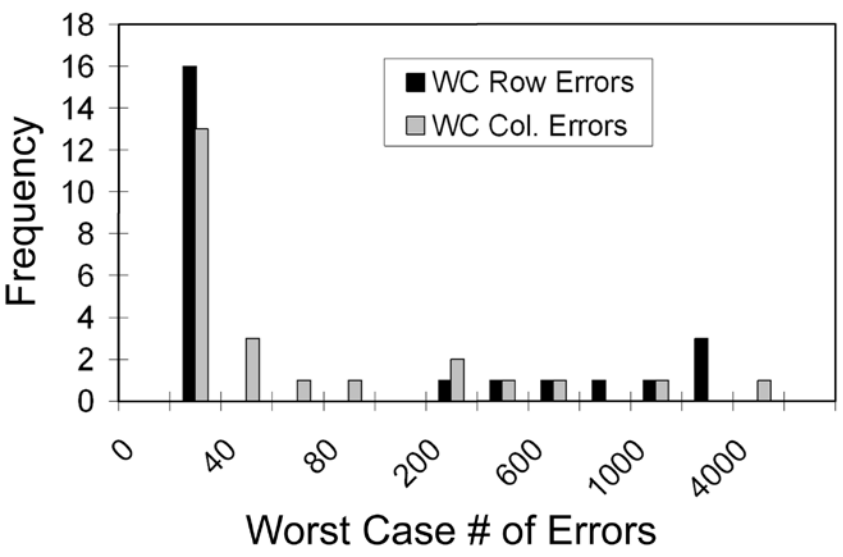


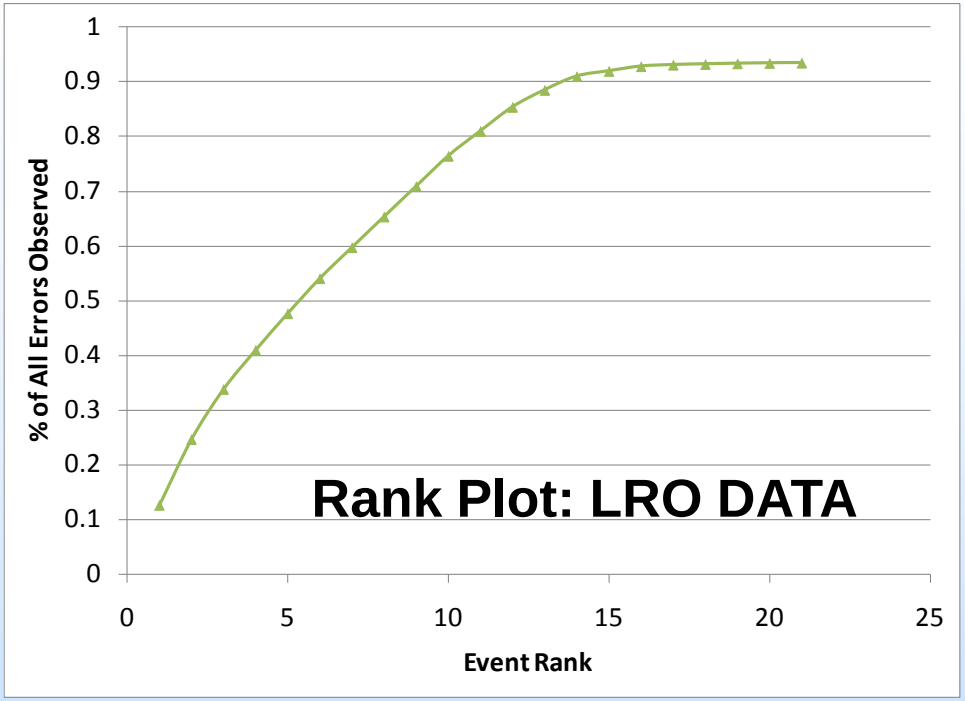
Error Mode	Predicted	Observed	Ratio: Obs/Pred.
SEU	0.0154	0.0031	0.2012987
Logic Errors	0.01	0.00017	0.017
Block Errors	0.00035	0.000033	0.0942857
SEFI	<8E-6	<6.5E-6	XXXXXXX
Stuck Bit		<1E-5	XXXXXXX

- Where statistics are good, observed SEE rate agrees with prediction
  - The more disruptive or rare the event, the worse the statistics are for error prediction
- On-orbit data limits now more stringent on SEFI and stuck bits than those from accelerator data

More LRO Data Analysis

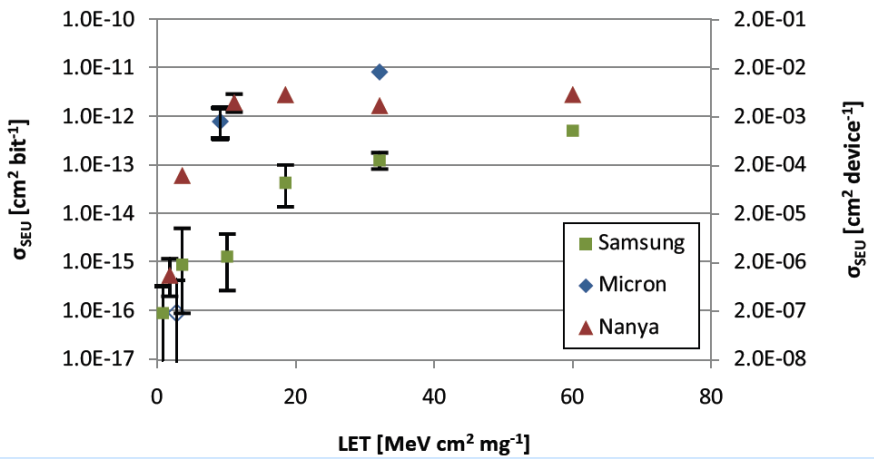
TAMU Data for Elpida SDRAM



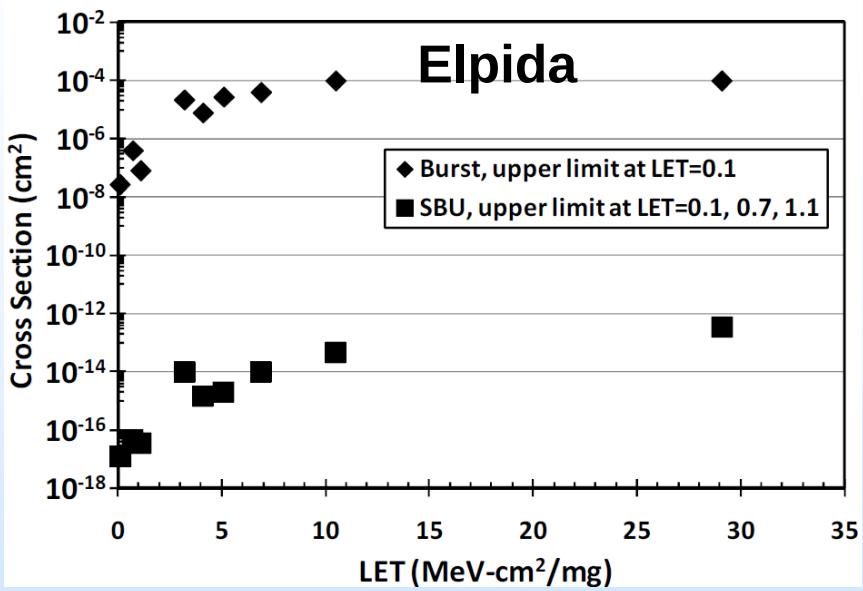


- As in heavy-ion test, majority of errors come in burst/block errors
  - 14 events account for >90% of errors
- No data lost to date using Reed-Solomon 2-nibble correction (x4 configuration)
  - No SEFIs requiring power cycle

SSR Components: Next Generation



M. Hermann et al., "Heavy Ion Testing of 2 Gbit DDR3 SDRAM," 2011 RADECS Data Workshop Proceedings.



R. Koga et al., "Sensitivity of 2 Gb DDR2 SDRAMs to Protons and Heavy Ions," IEEE Radiation Effects Data Workshop proceedings, p. 6, 2010.

- **Next-Generation SSRs will use DDR2 and DDR3 components**
  - **Test data for these parts are sparse**
    - **800-1600 GHz speeds make parts a challenge to test as well as to use.**
  - **Hits to Phase-Lock Loop (PLL) likely cause of Burst Errors seen at low LET**
    - **Some SRR designs will have PLL disabled**
  - **Using full speed of DDR2/3 parts will require very fast controllers**

New Challenges for SSRs

- **Most challenges arise due to increased density and Integration**
  - **Increased density of SDRAM die**
    - **Progression from 512 Mbit to 4 Gbit means increased correction load for EDAC—increased correction cycles or increased vulnerability**
  - **×4 die are now uncommon; ×8, ×16 more readily available**
    - **Larger data words easier to implement on wider die**
    - **Common EDACs can correct ~2 nibbles in error—that's 2 WC SEFIs on ×4, but only 1 on a ×8**
    - **EDAC that can correct 4 nibbles tends to be complicated**
  - **Stacked Die**
    - **Makes it difficult to SEL by overcurrent; SEL protection not possible**
    - **If SEFI requires power cycle, all data on stack is lost**
    - **Data not lost if memory is nonvolatile**
- **Rising rates for Block/Burst Errors means more worst-case errors**
  - **Increased correction burden**
- **Fewer vendors means fewer chances of hardness by serendipity**

Conclusions

- Current error mitigation approaches yield robust data integrity for SSR designs used to date.
- SEE rate estimation tools are adequate at least to 512 Mbit generation of SDRAMs
  - Poor statistics due to disruptive nature or rarity account for conservative nature of predictions for block data and SEFI modes
- Challenges upcoming
  - DDR2/3 SDRAMs exhibit a broad range of SEFI/block error behavior
  - SEFIs and block errors account for increasing share of bit flips
  - Data words and memory organization increasing in complexity
    - Makes implementing EDAC a challenge
  - Stacking of parts increased data loss during recovery from “unrecoverable SEFI”
- In Passing
  - EADS Astrium has developed a Flash based SSR
    - Nonvolatile nature of storage cells has advantages for error recovery, but FLASH has its own challenges
- Current mitigation strategies likely to persist for foreseeable future