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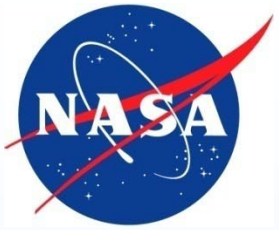
June 11-15, 2012

National Aeronautics
and Space Administration



Combined Effects on DDR* Class Memories

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***Double-Data-Rate**

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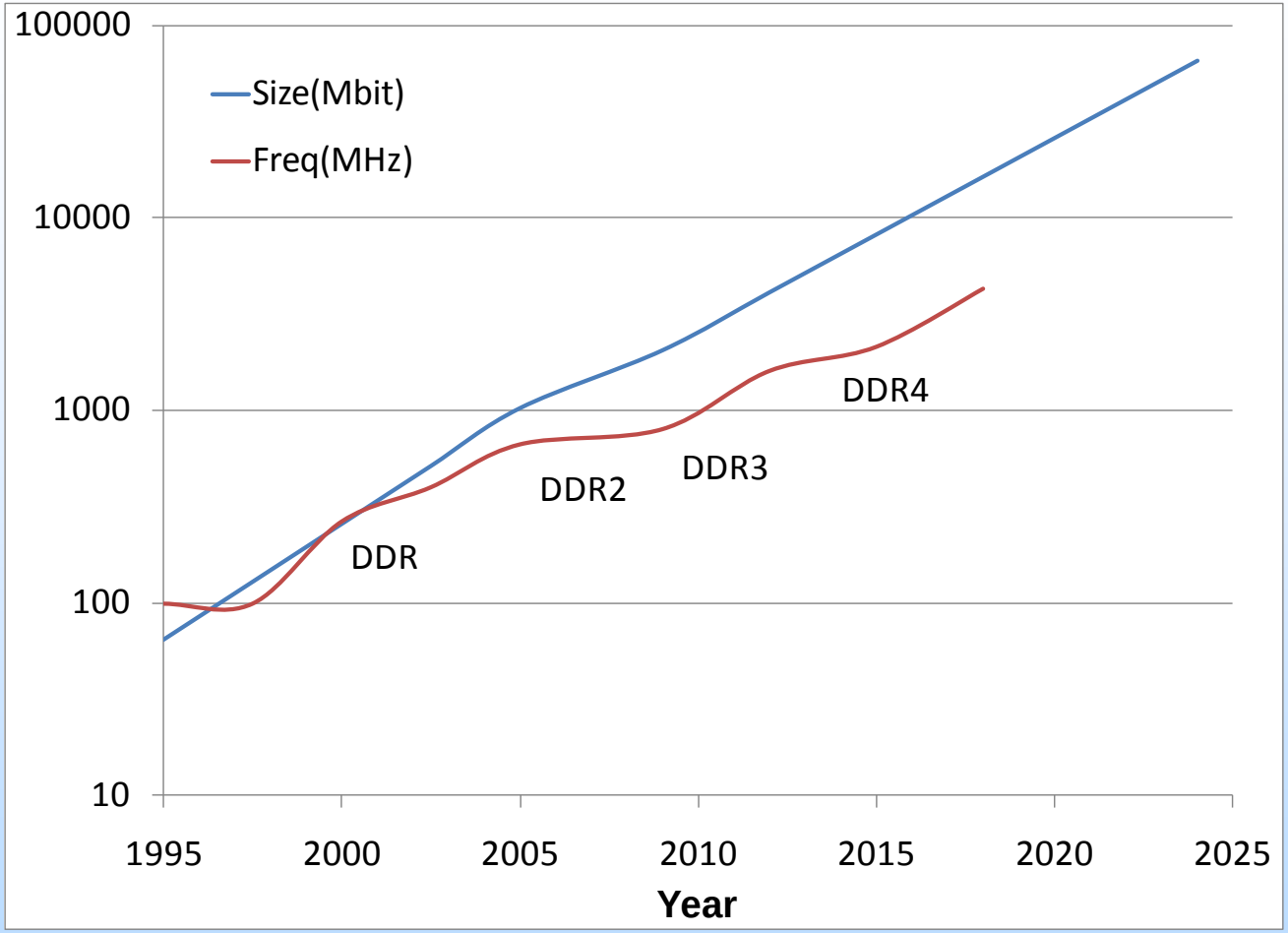
- Triad Spectrum
  - Ray Chao, Gary Ng, Mike Mikula

DDR SDRAM vs. FLASH



- **DDR SDRAM—Double-Data Rate Synchronous Dynamic Random Access Memory**
  - **Higher speed and endurance/retention make DRAM a better option in some applications than FLASH despite volatility and smaller size.**

Introduction

- 2011 testing: DDR2 SDRAMs hard to total ionizing dose (TID)
  - Parametric failures between 150 and 300 krad(Si)—only for biased parts
  - Functional Failure ~1 Mrad biased, 900 krad(Si) unbiased (little difference)
- Goal for 2012: Investigate synergistics between TID and Aging
  - Use overvoltage + elevated temperature 1000 hour "burn-in" to accelerate:
    - Electromigration (EM) and Stress migration (SM)
    - Hot Carrier Effects (HCE)
    - Time-Dependent Dielectric Breakdown (TDDB)
    - Negative Bias Temperature Instability (NBTI), etc.
- Do degradation mechanisms (aging) affect TID response?
  - Functional?
  - Parametric
- Is the strong bias dependence observed for virgin parts affected?
- Approach—Start with Industry standard life testing procedures and adapt as required to simulate ~10 years aging.
  - Test parts are 1-Gbit Dual Inline Memory Modules (DIMMs) from Samsung and Micron
    - Micron DDR2—MT47H128M8HQ
    - Samsung DDR2—M379T2863FB3-CF7

SDRAM Subtask

Description:

– *This is a continuation task for evaluating the effects of scaling (<100nm), new materials, etc. on state-of-the-art (SOTA) mass volatile memory (VM) technologies—mainly SDRAM. The intent is:*

– *To determine inherent radiation tolerance and sensitivities,*

– *Identify challenges for future radiation hardening efforts,*

– *Investigate new failure modes and effects, and*

– *Provide data to DTRA/NASA technology modeling programs.*

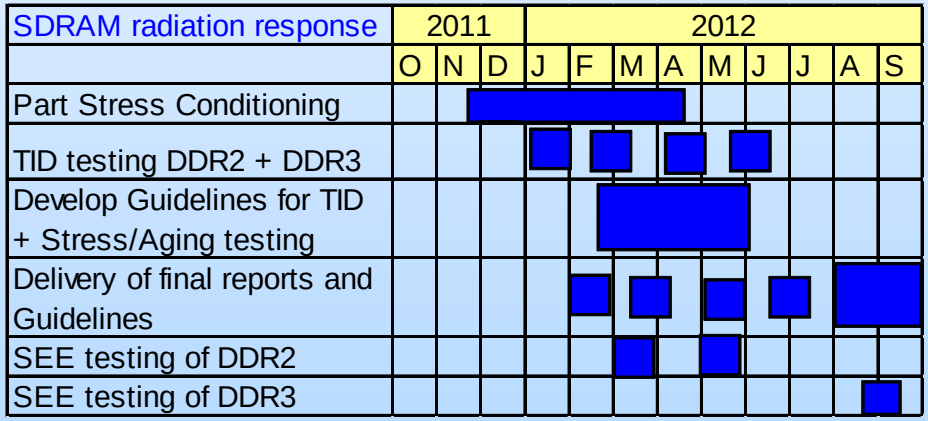
–*Testing includes total dose, single event (proton, laser, heavy ion), proton damage (where appropriate) and reliability. Test vehicles will include a variety of volatile memory devices as available, including DDR2 SDRAMs and commercial SRAMs… and DDR3 devices*

–*Emphasis for 2012 will be synergistic degradation resulting from aging and total ionizing dose (TID) response, but SEE testing also planned.*

FY12 Plans:

– *TID test structures*
  – *DDR2 and DDR3 SDRAM from Samsung and Micron*
  – *DDR2 SDRAMs from Elpida (courtesy of 3D Plus)*
  – *TID/reliability tests will use the new Triad Memory tester*
– *Test focuses*
– *Evaluate potential synergistic effects of TID and SDRAM aging*
  – *Use thermal and voltage acceleration methods*
  – *Evaluate degradation due to aging/stress*
  – *Compare TID response of stressed to unstressed parts*
– *SDRAM SEE response for current generation DDR2 and DDR3 SDRAMs if funding, tester capability and time allow.*

Schedule:



Deliverables:

-*Updated SSR Radiation Guidelines*

-*Updated guidelines for TID testing of SDRAMs taking into account wearout mechanisms*

- *Test reports*

-*Publications*

–*Effects of Bias, Electrical and Thermal Stress on DDR SDRAM Total Ionizing Dose Response*

–*NASA and Non-NASA Organizations/Procurements:*

–*Beam procurements: GSFC/REF, TAMU, LBNL*

–*Partners: 3D Plus, JPL, Micron, Samsung, BAE Systems*

Subtask lead: Ray Ladbury

Goals

- **Assess TID capability of SOTA DDR2**
  - **Current generation parts ~30 nm min. feature size**
  - **Previous tests (~90 nm) failure occurred ~150-250 krad(Si)**
- **Independently assess reliability/life testing**
  - **Work with vendor to reproduce standard test regime**
  - **Assess degradation in performance and functionality**
- **Look for Evidence of Synergy**
  - **Rationale—TID, TDDB and HCE, NBTI, etc. all depend on and modify oxide properties**
  - **Also, all these stresses erode margins, affect timing—critical for operation of DDR devices**
- **Extend study to DDR3 devices for both Samsung and Micron**

Expected Impact to Community

- **Increase confidence for use of DDR devices in space environments**
  - **Validate life testing for conditions of use in space**
  - **Validate reliability test methods**
- **Identify new failure mechanisms**
  - **Reduce risk**
  - **Refine test methodologies and standards**
- **Determine whether TID and reliability can be assessed independently**
  - **Do synergies exist, and are they important for assessing reliability or for qualification strategies?**

Status/Schedule

- **DDR2 DIMMs—Samsung and Micron**
  - **Initial TID testing of Samsung DDR2 completed 2011**
  - **Aging study completed on Samsung DDR2 1/2012**
    - **85 °C + 50% overvoltage for 1000 hours ~10 yrs for operating temperatures up to 40 °C**
    - **Overvoltage effect questionable due to internal regulation**
    - **Triad tester used for both aging study and parametric/functional testing**
  - **TID testing of aged Samsung DDR2s completed 1/2013**
  - **Initial TID testing of Micron DDR2 completed 4/2012**
  - **Aging Study for Micron DDR2s completed 6/2012**
  - **TID testing of Micron DDR2—6/2012**
  - **Full results to be reported @ NSREC 2012 in Miami**
- **DDR3 DIMMs to be tested once DDR2s completed**
  - **Triad is unavailable for testing while parts are undergoing aging**
  - **Same CMOS generation for DDR2/DDR3-expect similar behavior**

DDR Parametrics

Parametric measurements limited to current drawn, timing

Symbol	Test Conditions
IDD0	**Operating one bank active-precharge current**; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC =tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD2P	**Precharge power-down current**; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD2Q	**Precharge quiet standby current**:; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD2N	**Precharge standby current**; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD3P	**Active power-down current**; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD3N	**Active standby current**; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD5B	**Burst auto refresh current**; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD6	**Self refresh current**; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R

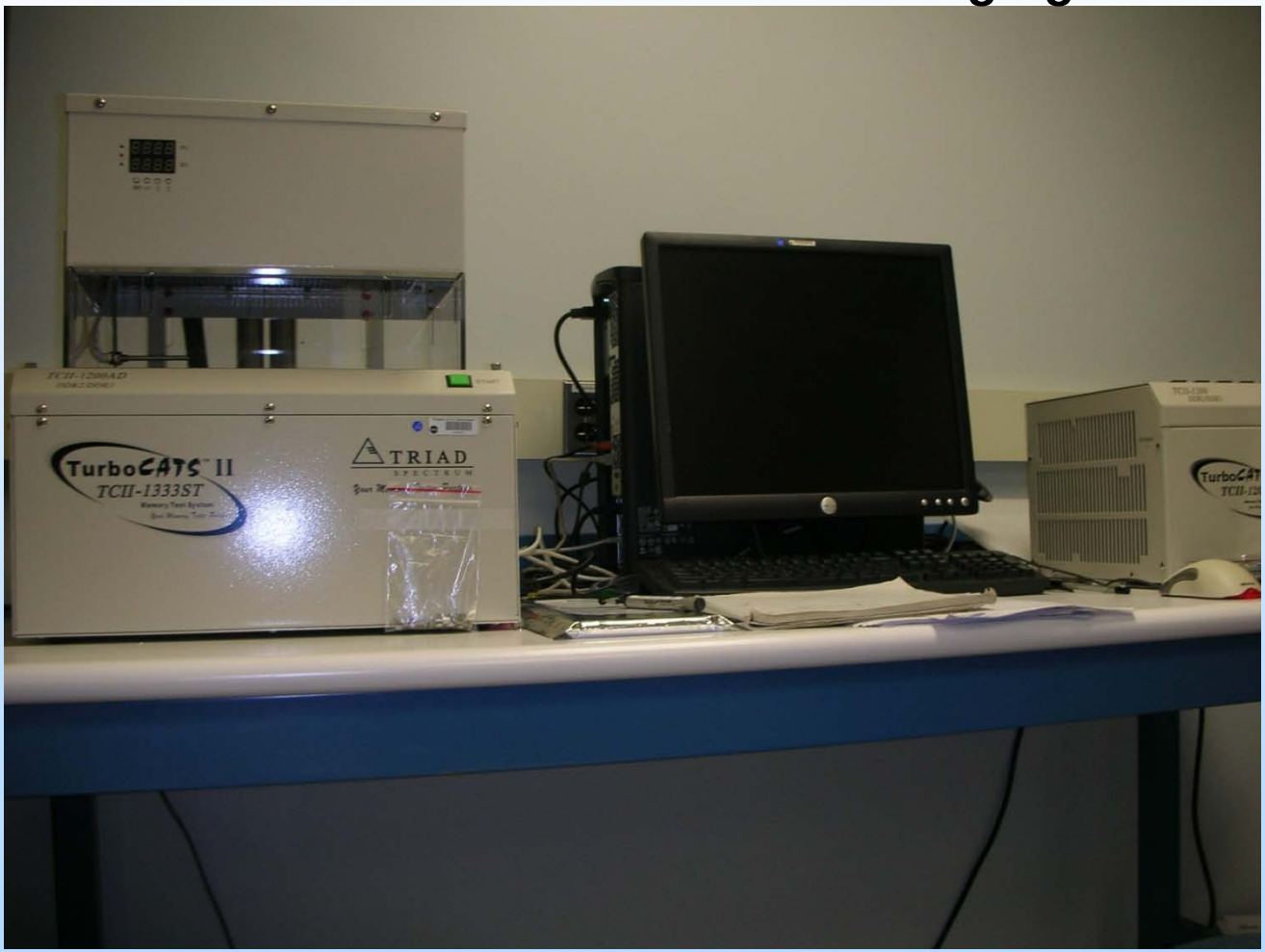
Sensitive Parameters for Micron

Sensitive Parameters for Samsung

Sensitive for Micron

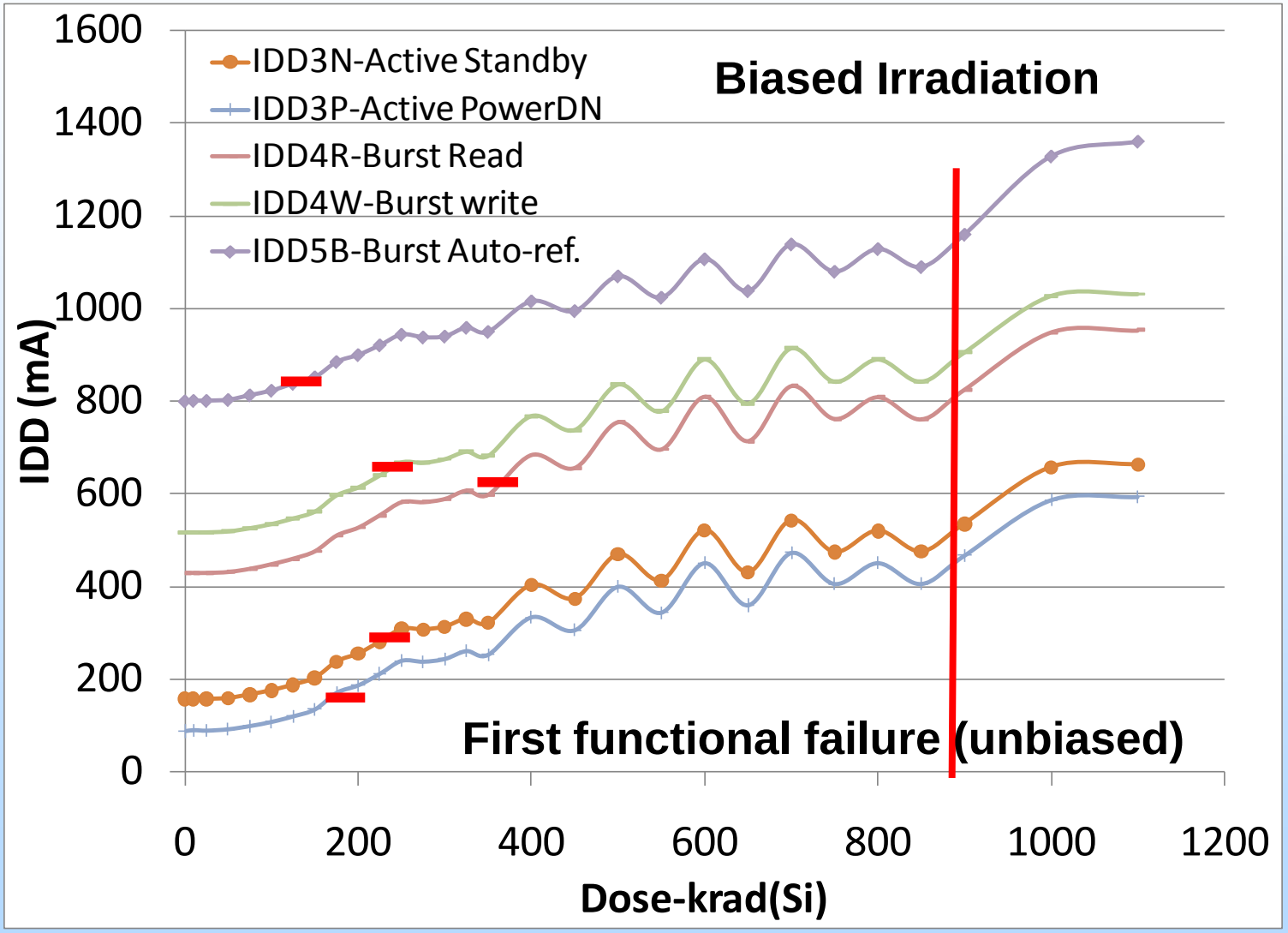
Technical Highlights

- Triad tester automatically measures timing, current while providing clock and control of DIMMs
  - Used for both measurement and aging



Technical Highlights

Review of Unstressed Samsung DDR2 SDRAM



Technical Highlights

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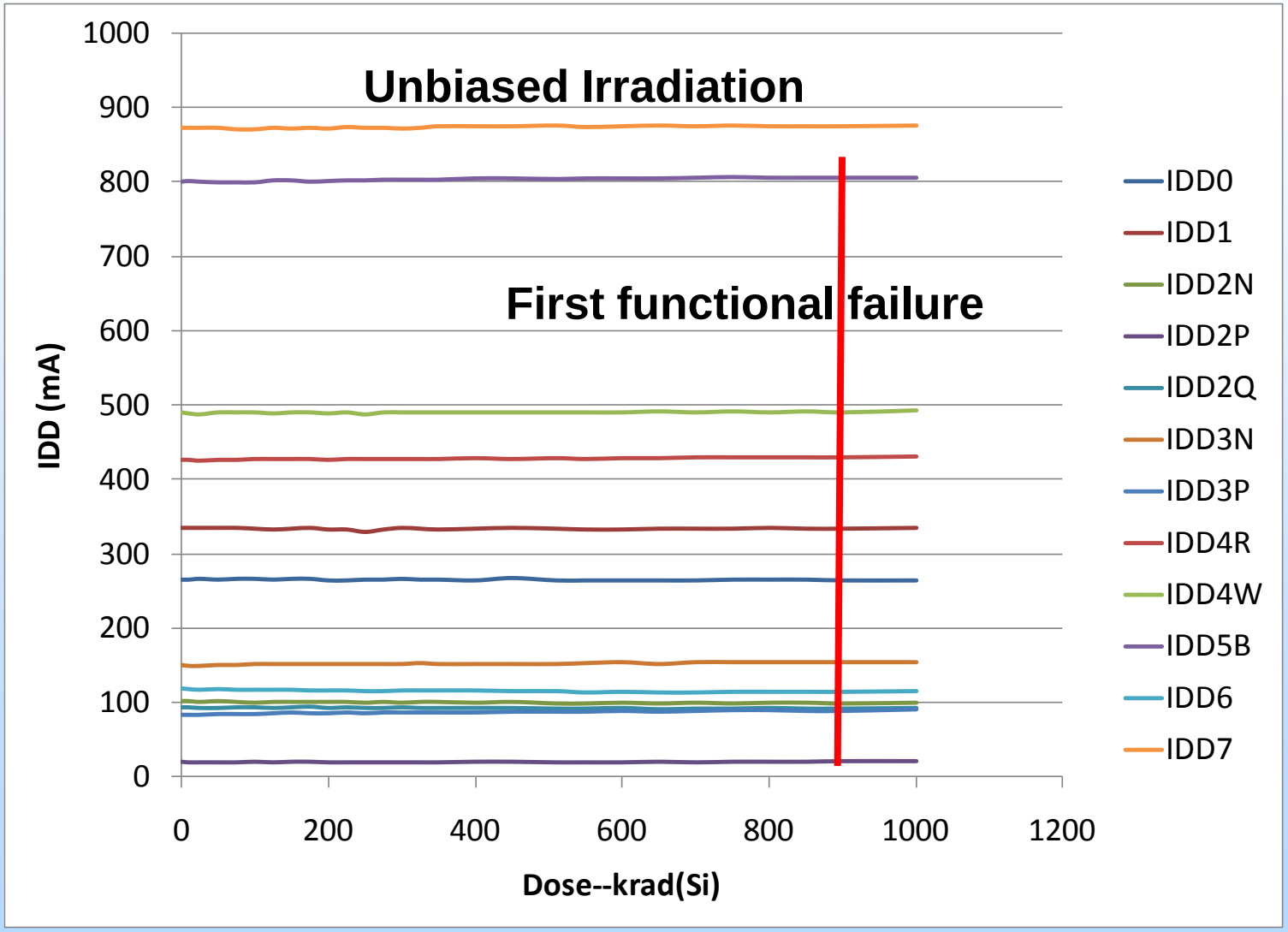
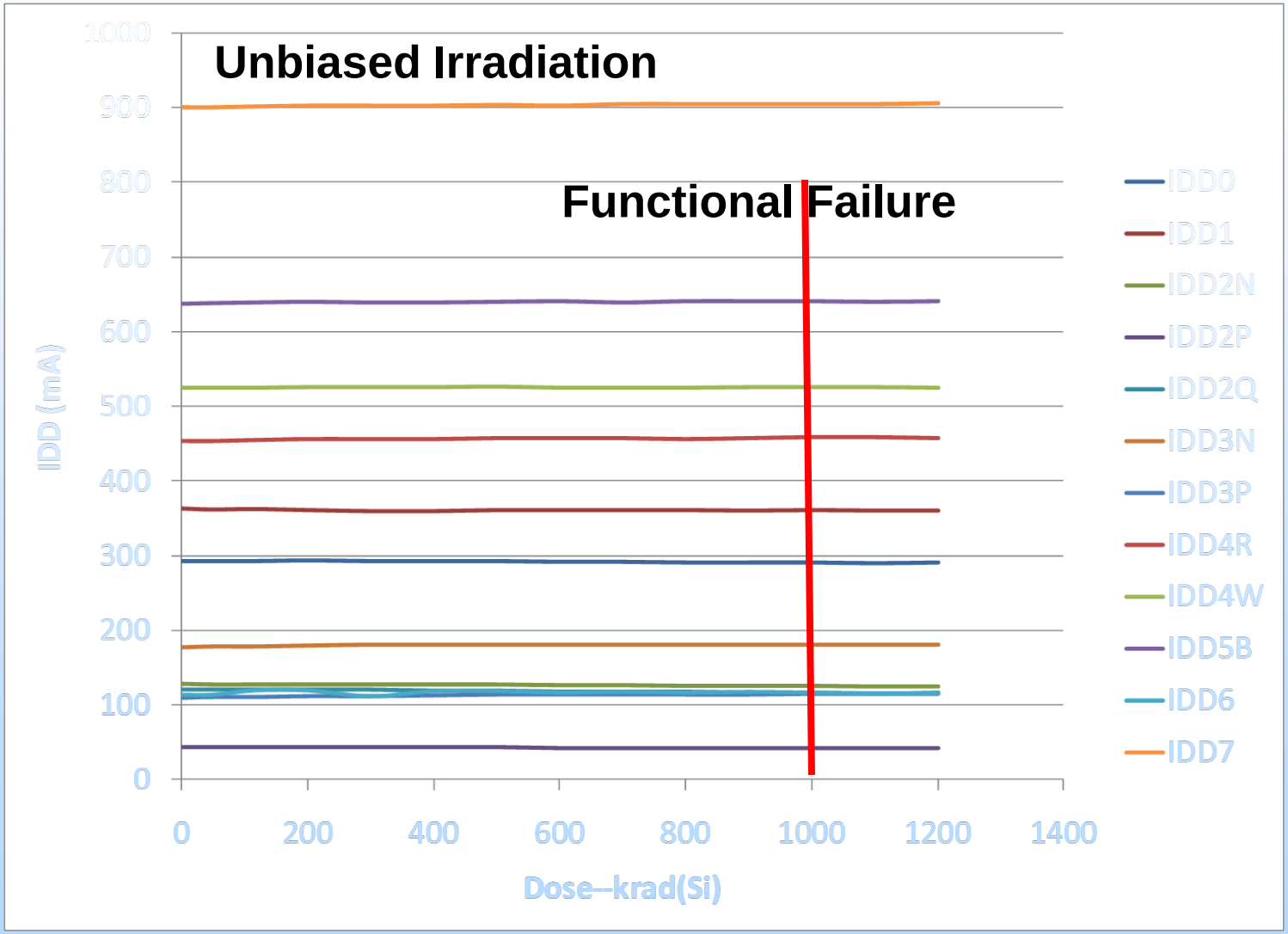


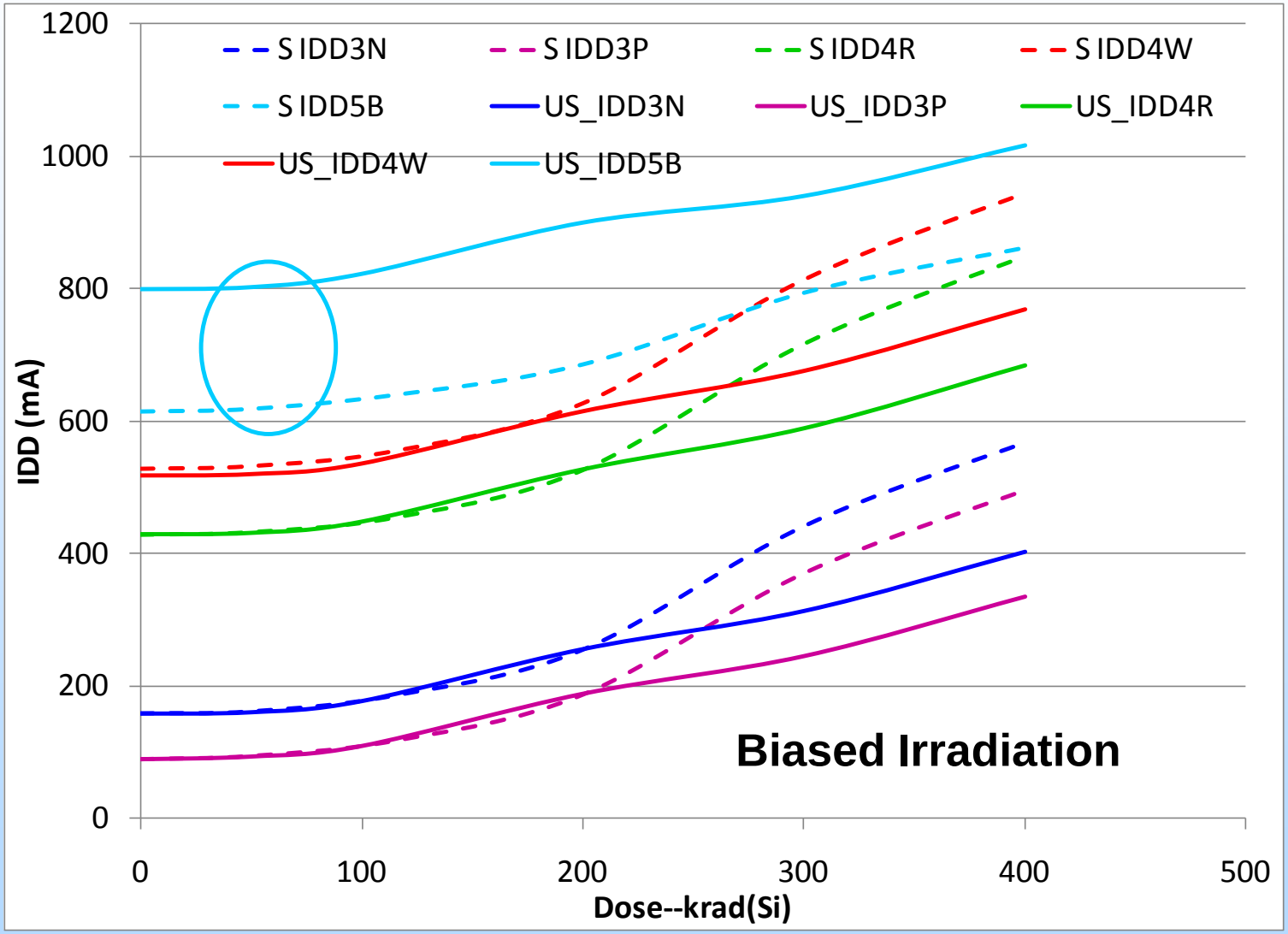
Technical Highlights

New: Stressed Samsung DDR2 SDRAM--Unbiased



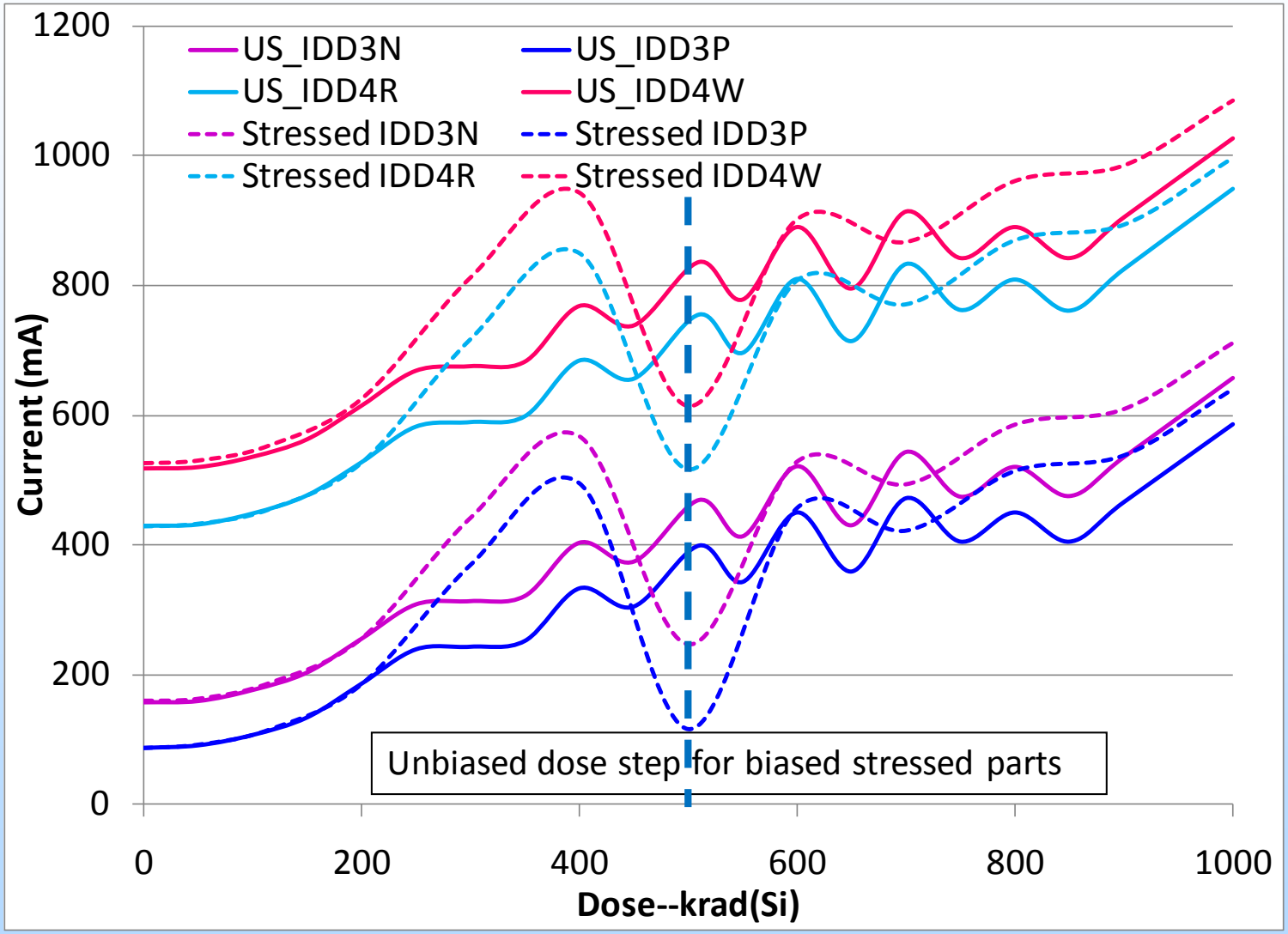
Technical Highlights

Comparison Samsung DDR2 SDRAM—Biased



Technical Highlights

Comparison Samsung DDR2 SDRAM—Biased



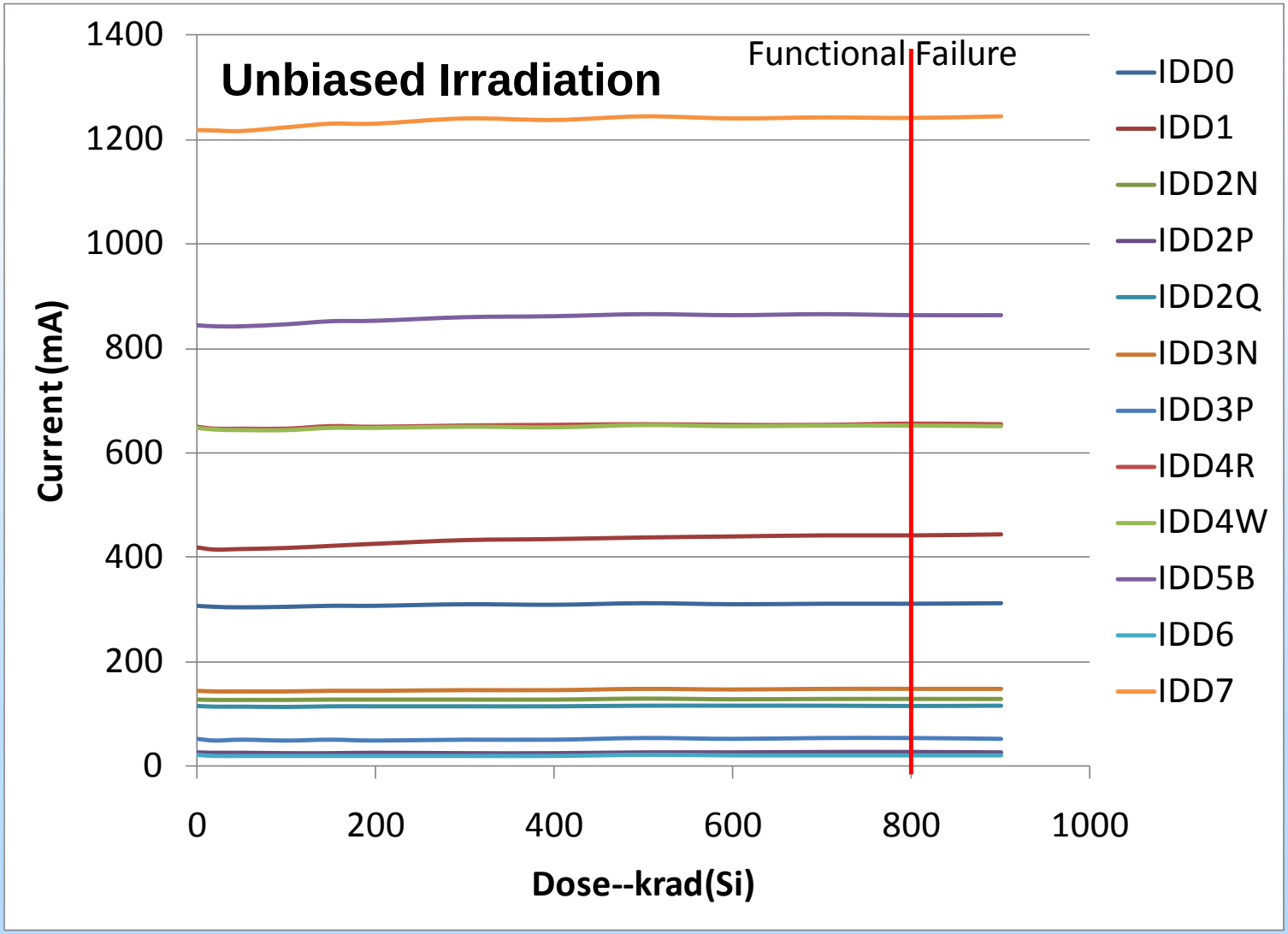
Technical Highlights

Summary: Samsung DDR2 TID and Aging

- **Unbiased irradiation—Almost no change in operating currents, but functional failure at same level as biased parts**
- **Biased irradiation—monotonic increase in operating currents—especially**
  - **IDD3P—Active Power-Down Current**
  - **IDD3N—Active Stand-By Current**
  - **IDD4R—Operating Burst Read Current**
  - **IDD4W—Operating Burst Write Current**
  - **IDD5B—Burst Auto-Refresh Current**
  - **All other currents remain within specification up to and beyond failure.**
- **Functional Failure occurs @1 Mrad(Si) ±100 krad(Si)**
  - **Most vulnerable for most dynamic tests (e.g. hammer and Marching patterns)**
- **Effect of Aging**
  - **TID in Biased DIMMs similar for stressed and unstressed up to ~200-300 krad(Si)**
    - **Failures doses unaffected**
    - **Above ~200 krad(Si), stressed parts degrade slightly more rapidly than unstressed**
  - **Unbiased DIMM TID response is unaffected by prior applied aging stress**
  - **Functional failure doses and modes unaffected by stress**

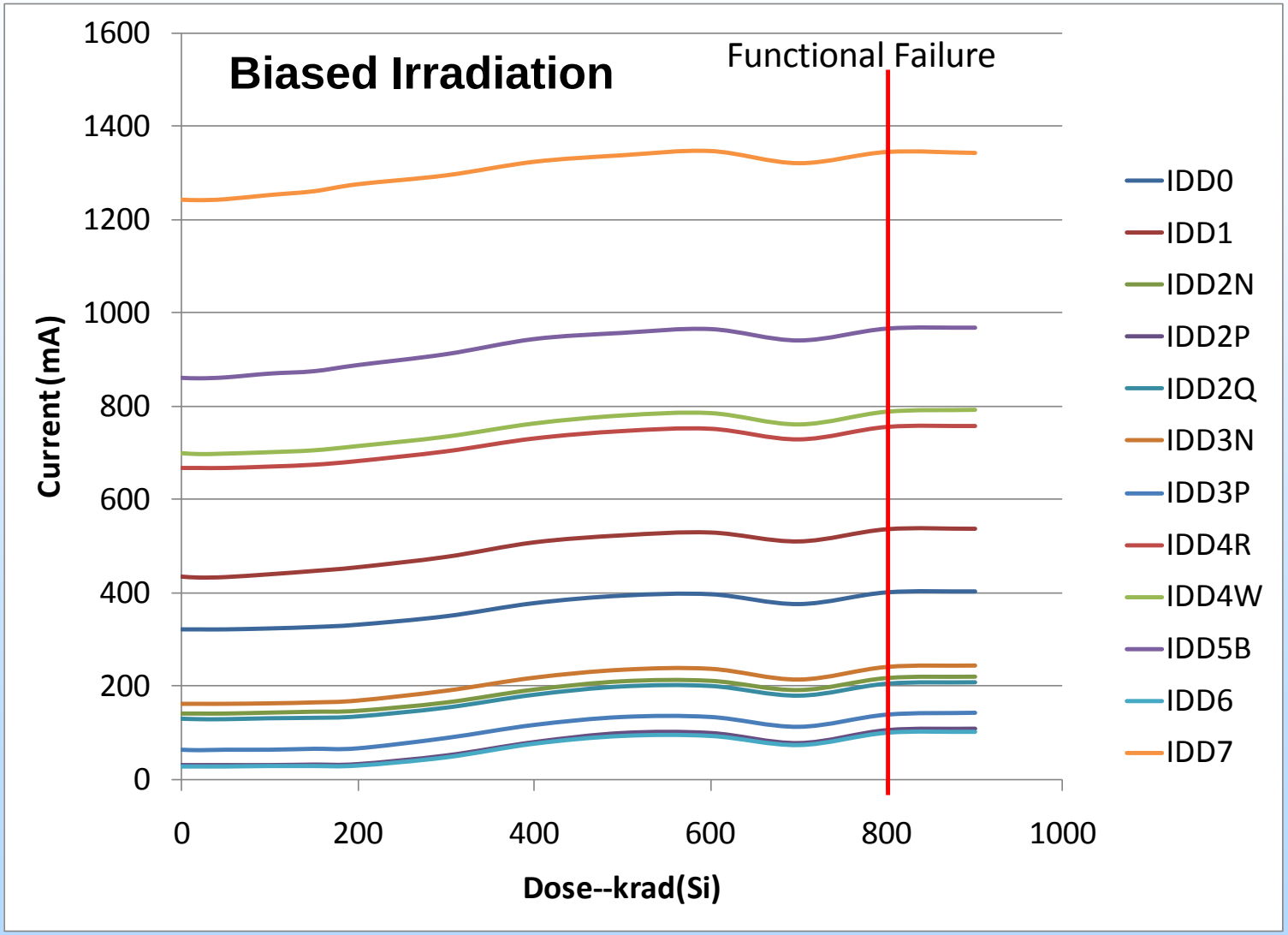
Technical Highlights

Unstressed Micron DDR2 SDRAM



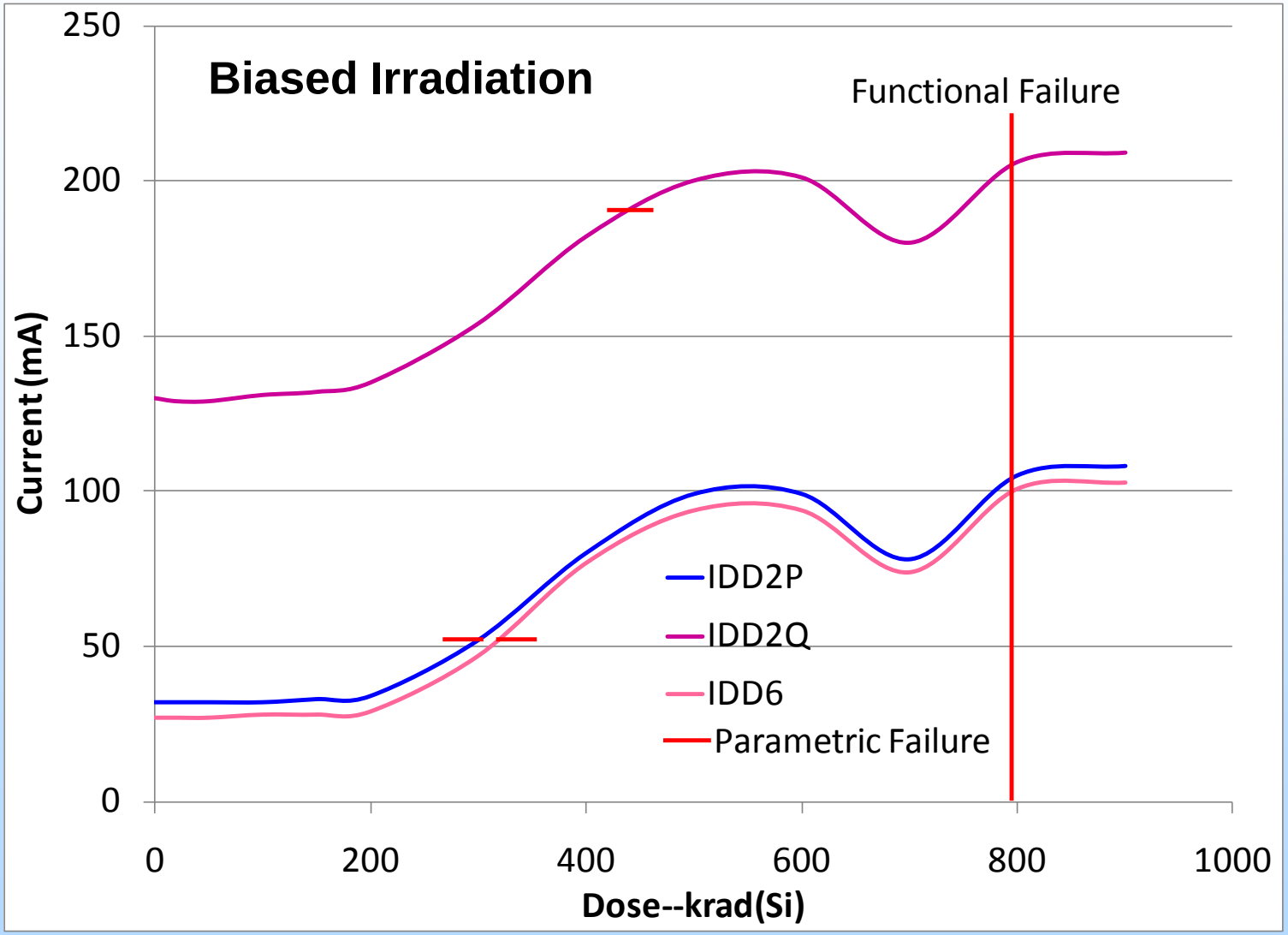
Technical Highlights

Unstressed Micron DDR2 SDRAM



Technical Highlights

Unstressed Micron DDR2 SDRAM—Parametric Failures



What Does It Mean?

- Current Generation DDR2 SDRAMs are TID hard
  - Samsung DDR2s fail parametrically (DC) between 150-400 krad(Si) (biased only) and functional failure ~1 Mrad(Si) (biased and unbiased)
  - Micron DDR2s fail parametrically (DC) from 250-500 krad(Si) (biased only) and functionally ~800 krad(Si) (biased and unbiased)
    - Sensitive parameters are IDD2P, IDD2Q and IDD6
- Manufacturer life-testing can be simulated with commercial testers
  - Moderate overvoltage (~50%) and elevated temperature (85 °C) @ 1000 hrs yields ~10 yrs. of aging.
    - Internal voltage regulation limits efficacy of overvoltage for memory core
    - Different degradation mechanisms have different overvoltage and temperature dependence—difficult to define a single acceleration factor
- Samsung DDR2s show minor enhancement of TID damage w/ aging
  - Does not significantly affect parametric or functional failure doses
- Results for Stressed Micron DDR2s this month—see you @ NSREC
- For now, results indicate TID and aging effects can be assessed independently, despite minor synergistic interaction