Non Volatile Flash Memory Radiation Tests

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Introduction

- Commercial flash memory industry has experienced a fast growth in the recent years, because of their wide spread usage in cell phones, mp3 players and digital cameras

- On the other hand, there has been increased interest in the use of high density commercial nonvolatile flash memories in space because of ever increasing data requirements and strict power requirements

- Because of the complex structure of flash memories; they cannot be treated as just simple memories in regards to testing and analysis. It becomes quite challenging to determine how they will respond in radiation environments

DEVICES UNDER STUDY

- Samsung 1,2,4 and 8Gb
- Micron Technology 1,2,4,8,16, 32 and 64Gb
- Feature sizes from 120-25 nm

Experimental Procedure

Test Facilities

- SEU Measurements
  - BNL
  - RADEF
  - TAMU
- TID Measurements
  - JPL Co-60

Experimental Procedure

Test Methods

- Data were taken using a commercial memory tester from JDI
- Prior to irradiation, the DUTs were programmed with all ‘0’ pattern
- The sample size for all measurements was three

Experimental Procedure

SEU MEASUREMENTS

- The DUTs were etched to remove the plastic packaging and expose the die to the ion beam

- During high LET SEU measurements the beam flux was set to ~ $2x10^2$ ions/cm^2/sec and the DUT was irradiated for 10-12 seconds in order to reduce the likelihood of occurrence of SEFIs in a given run

Experimental Procedure

SEU Measurements

– During irradiation, the DUT was dynamically operated in READ mode. After irradiation and the completion of the final READ cycle that was started during irradiation, the device's power was cycled, the DUT was read again, checked for errors, and logged. This method insured that the errors are from bit upsets in the FGs.

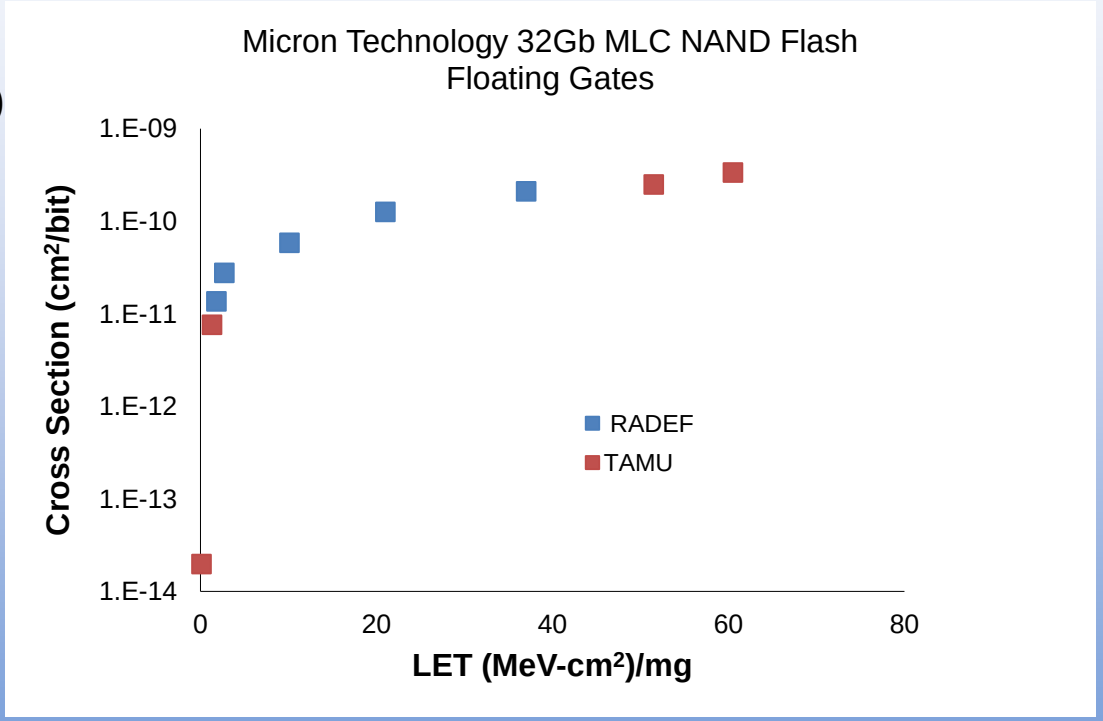
Experimental Procedure

TID Measurements

- Dose rate of 50 rad (Si) per second at room temperature
- In all measurements the DUTs were under static bias (3.6V) during irradiation, but not actively exercised
- Measurements were made in No Refresh Mode (READ only) & Refresh Mode (Erase/Program/Read)

Single Event Upset Results

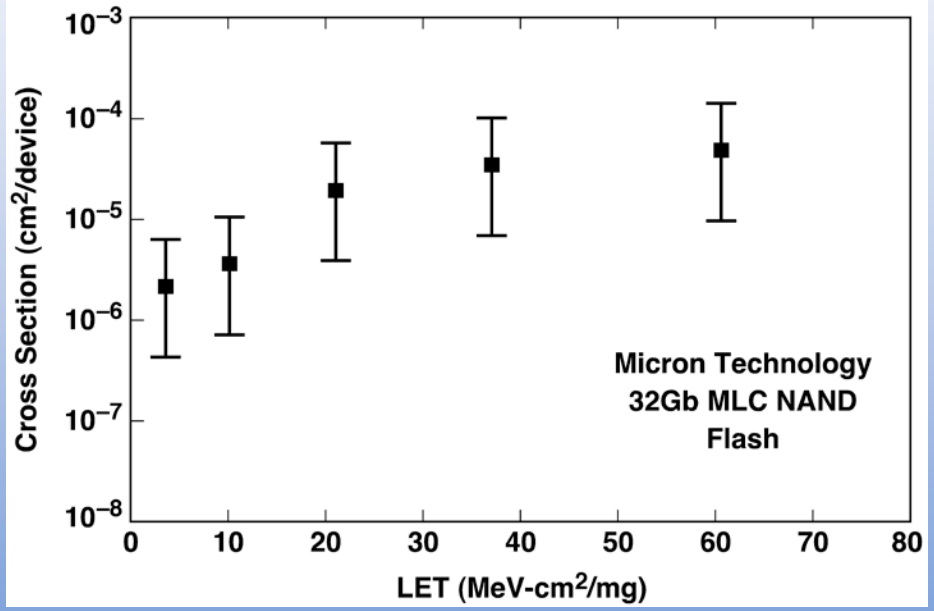
- SEU events were measured at RADEF and TAMU on MLC 32Gb (LET 0.1- 62 MeV-cm^2/mg)
- The FG SEU cross-section per bit is on the order of 3×10^{-10} cm^2/bit
- The FG SEU rate is 5.1×10^{-9} per bit per day for the background GCR environment



SEU cross-section for Micron 32Gb MLC NAND flash memory. Error bars are smaller than the plotting symbols

Single Event Upset Results

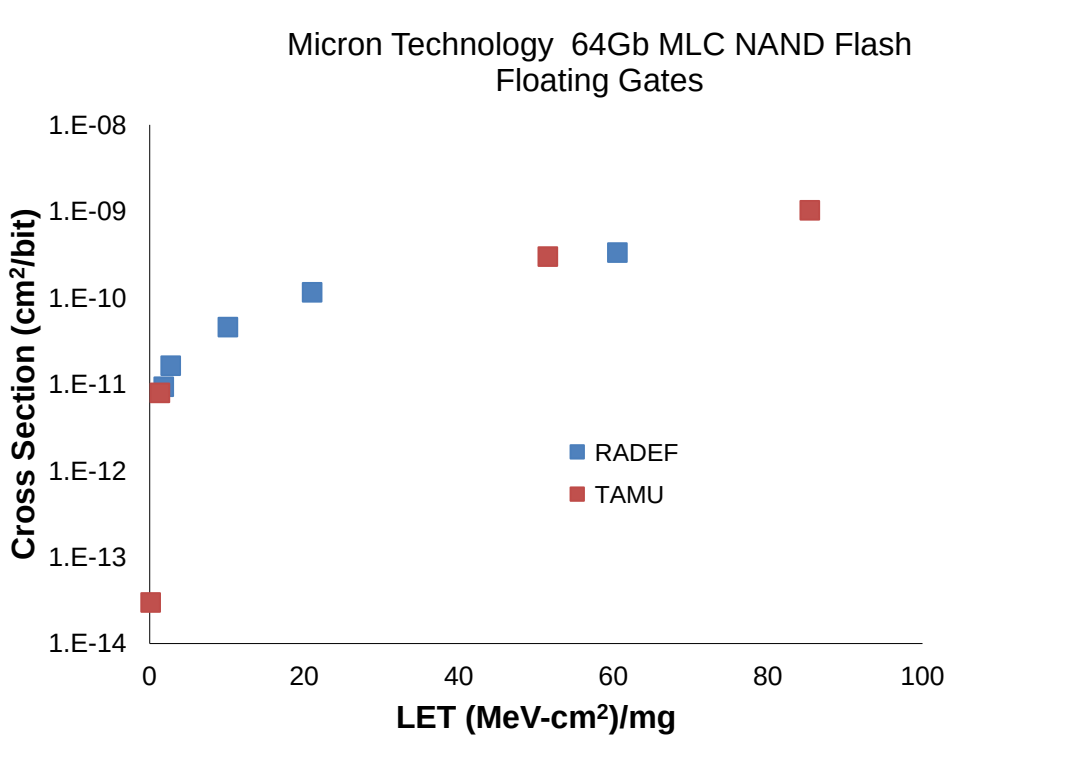
- SEFI events were measured at RADEF on MLC 32Gb (LET 3.6- 62 MeV-cm^2/mg)
- The SEFI cross-section per bit is on the order of 5×10^{-5} cm^2/bit
- The SEFI rate is $2.1\text{x}10^{-4}$ per device per day for the background GCRs environment



SEFI cross-section for Micron Technology 32Gb MLC NAND flash memory

Single Event Upset Results

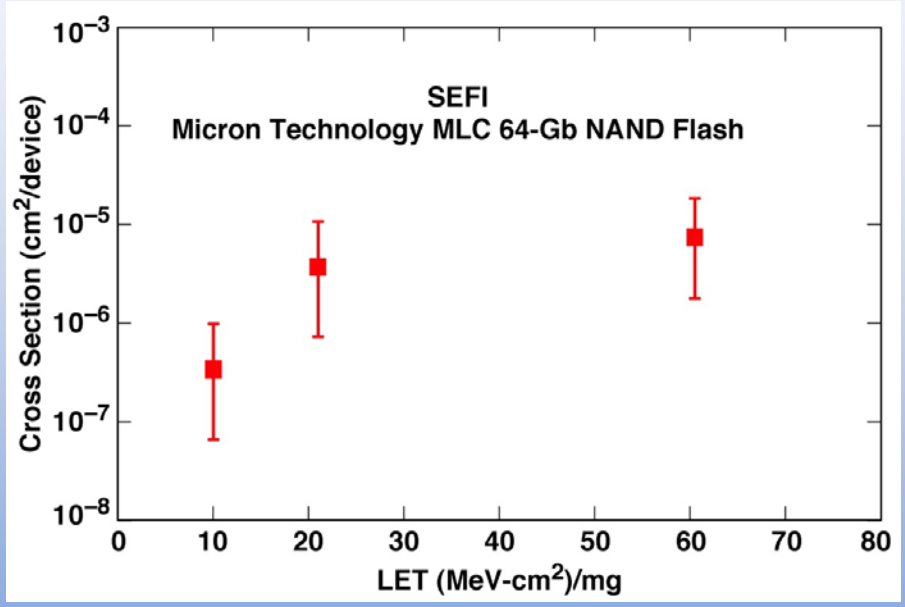
- SEU events were measured at RADEF and TAMU on MLC 64Gb (LET 0.1- 85 MeV-cm^2/mg)
- The FG SEU cross-section per bit is on the order of 1×10^{-9} cm^2/bit



SEU cross-section for Micron Technology 64Gb MLC NAND flash memory. Error bars are smaller than the plotting symbols

Single Event Upset Results

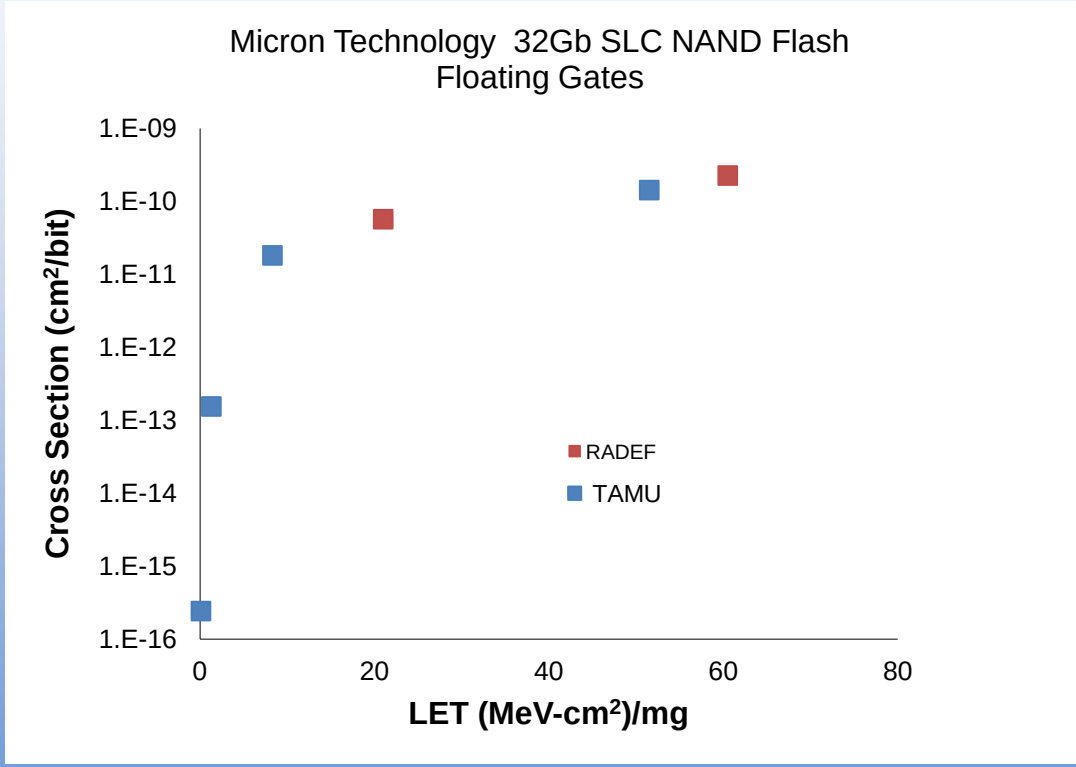
- SEFI events were measured at RADEF on MLC 64Gb (LET 10.1- 62.5 MeV-cm^2/mg)
- The SEFI cross-section is on the order of 7×10^{-6} cm^2/device



SEFI cross-section for Micron Technology 64Gb MLC NAND flash memory.

Single Event Upset Results

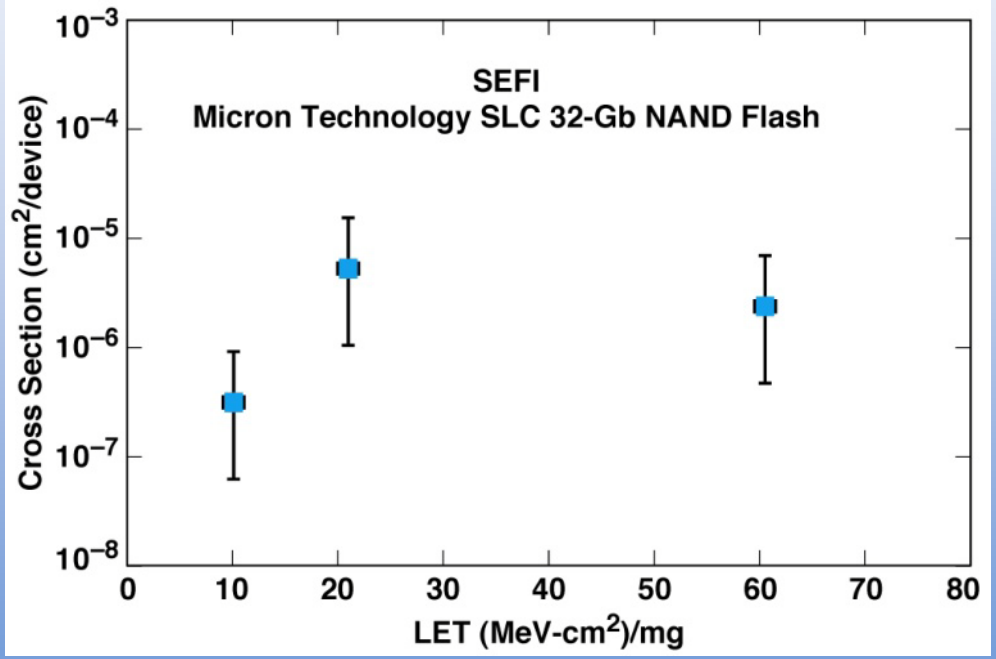
- SEU events were measured at RADEF and TAMU on SLC 32Gb (LET 0.1- 62 MeV-cm^2/mg)
- The FG SEU cross-section per bit is on the order of 2×10^{-10} cm^2/bit



SEU cross-section for Micron 32Gb SLC NAND. Error bars are smaller than the plotting symbols

Single Event Upset Results

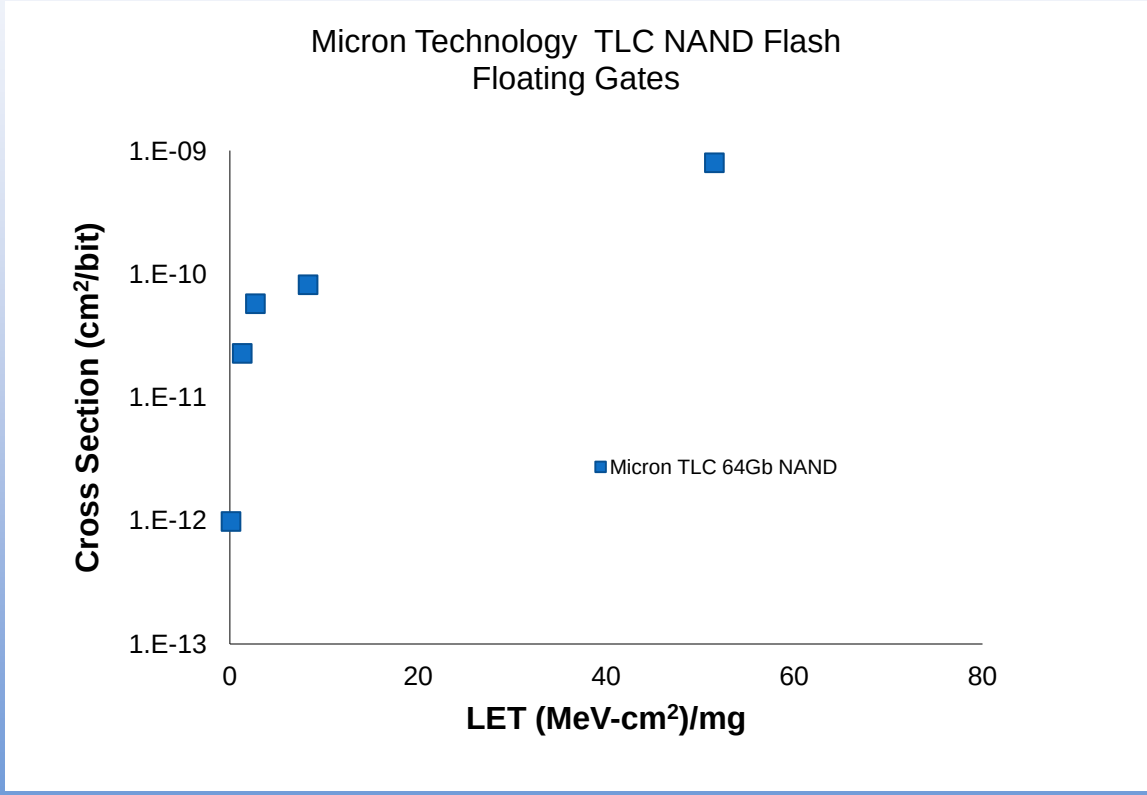
- SEFI events were measured at RADEF and TAMU on SLC 32Gb (LET 10.1- 62 MeV-cm^2/mg)
- The SEFI cross-section per bit is on the order of 2×10^{-6} cm^2/device



SEFI cross-section for Micron 32Gb SLC NAND flash memory.

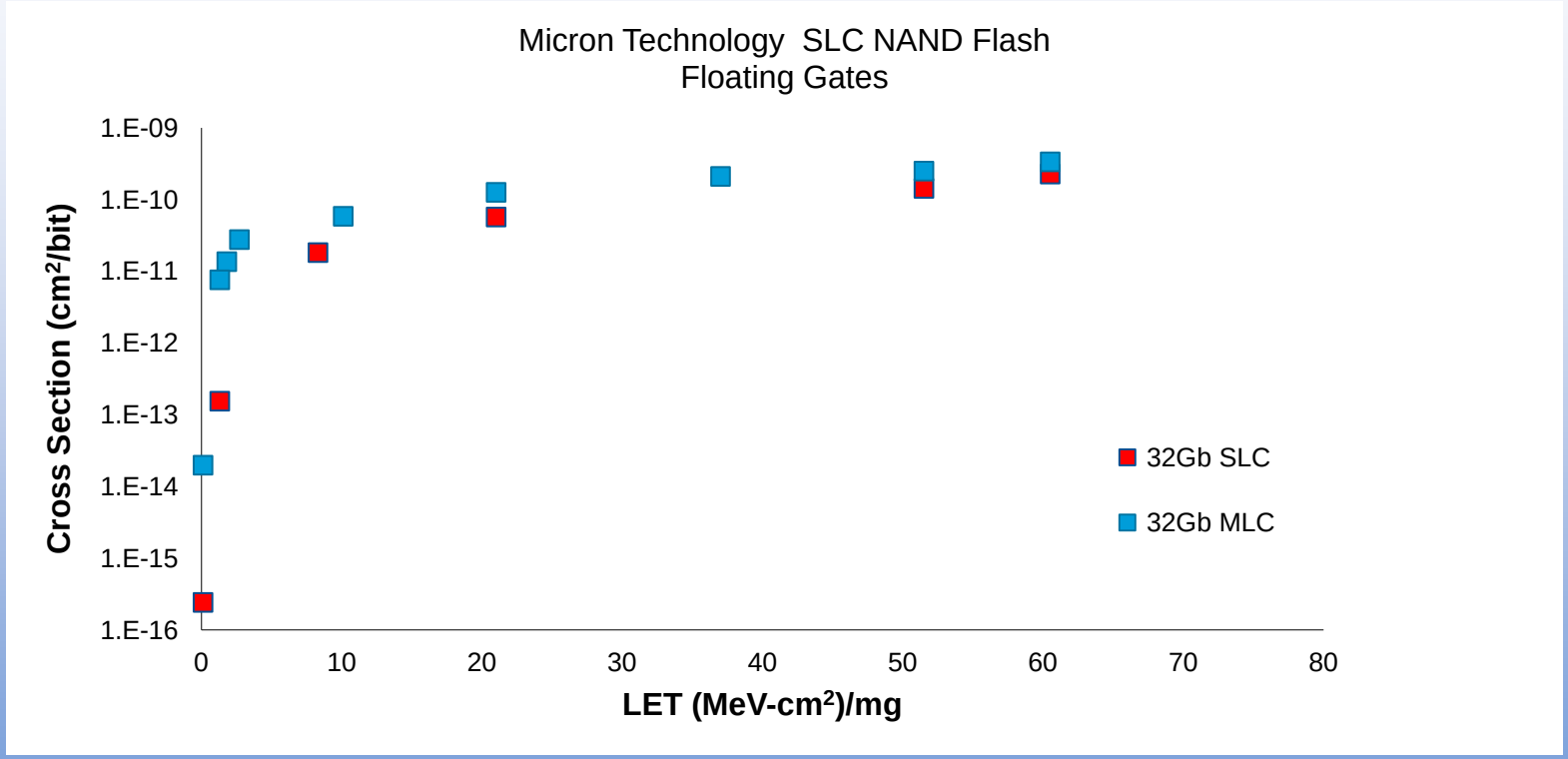
Single Event Upset Results

- SEU events were measured at TAMU on TLC 64Gb (LET 0.1- 51 MeV-cm^2/mg)
- The SEU cross-section per bit is on the order of 8×10^{-10} cm^2/bit



FG SEU cross-section for Micron 64Gb TLC NAND flash memory. Error bars are smaller than the plotting symbols.

Single Event Upset Results



Comparison of SEU cross-section for Micron 32Gb SLC and MLC NAND flash memories. Error bars are smaller than the plotting symbols.

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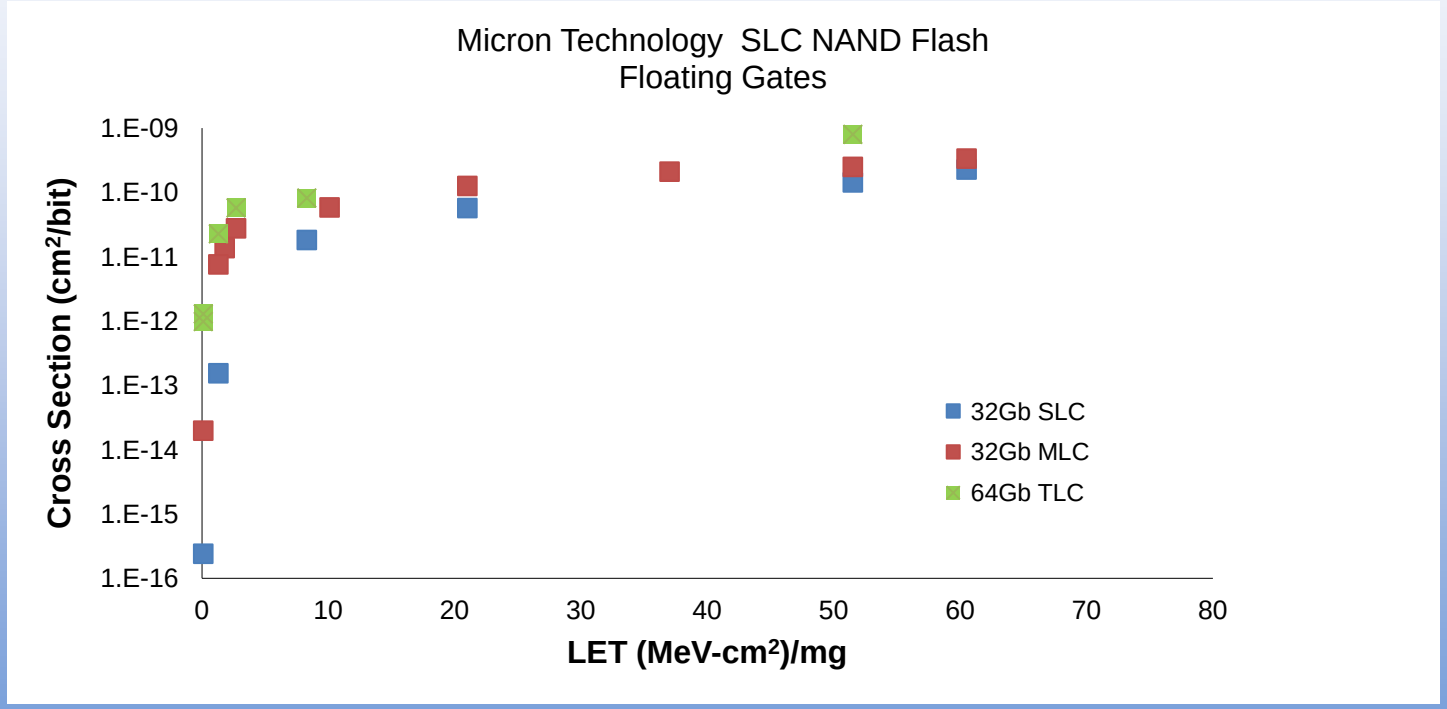
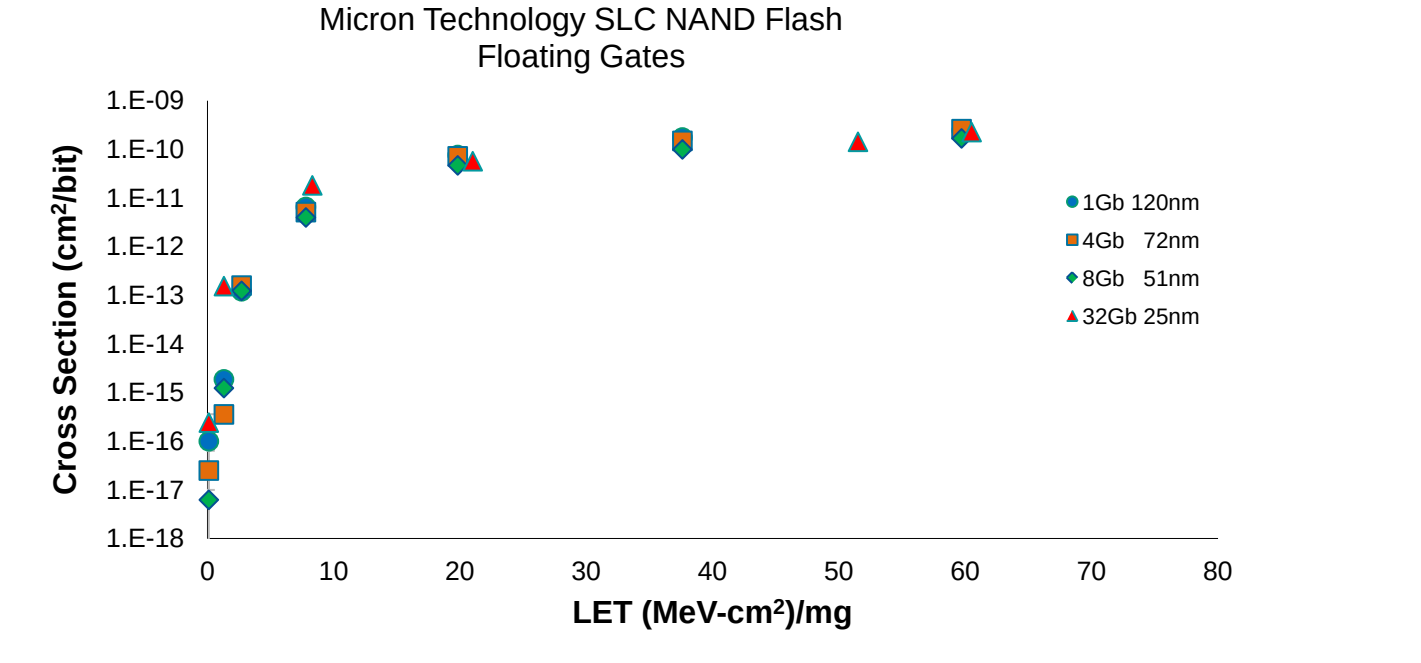
Single Event Upset Results



Comparison of SEU cross-section for Micron SLC, MLC and TLC NAND flash memories. Error bars are smaller than the plotting symbols.

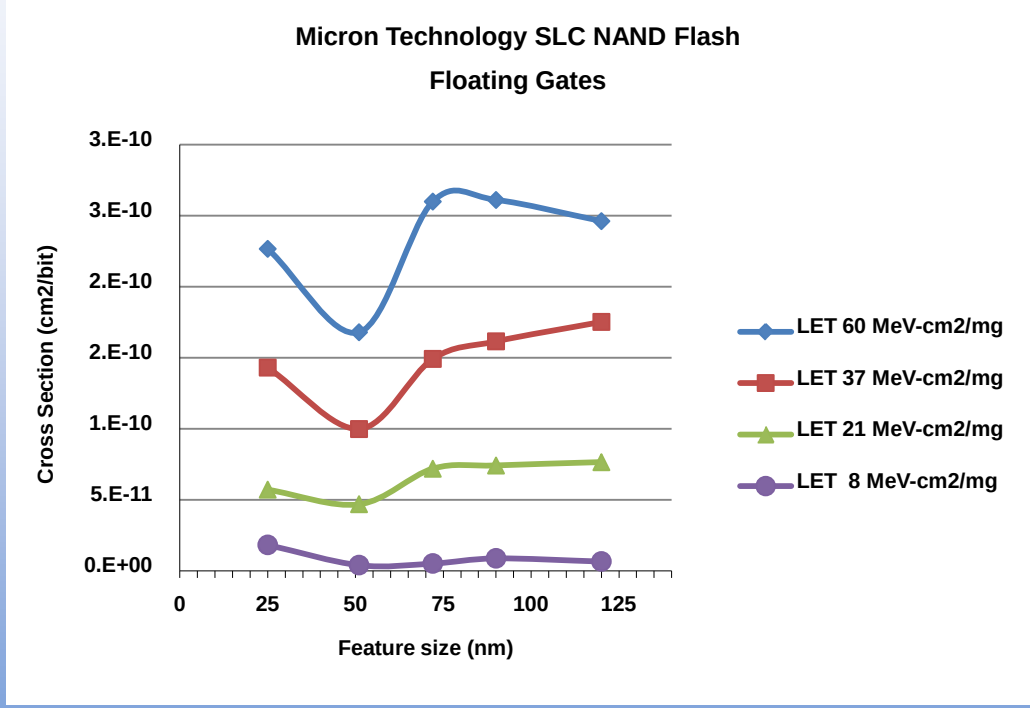
Single Event Upset Results Scaling



Scaling effect of FG SEU cross-sections for Micron SLC NAND flash memories. Error bars are smaller than the plotting symbols

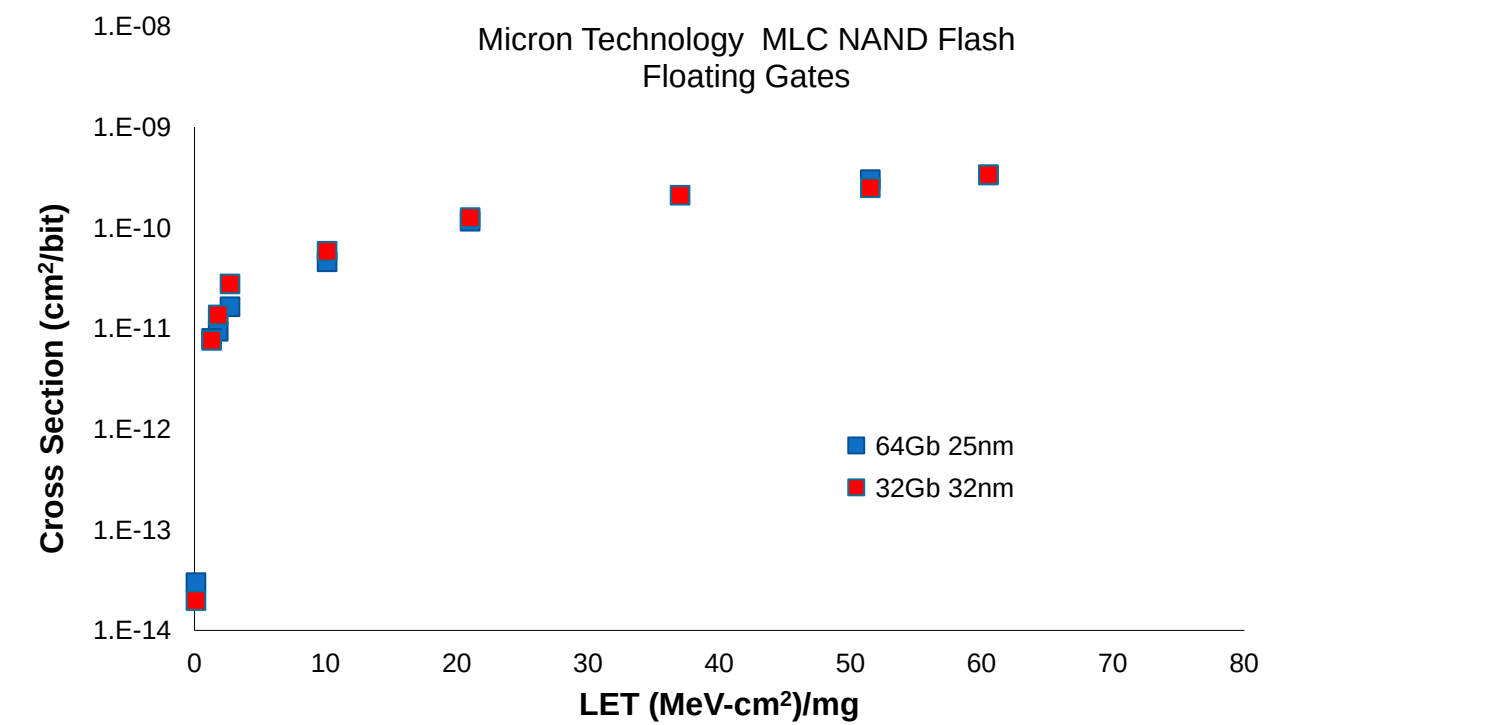
Single Event Upset Results Scaling

- No noticeable scaling effect for the 120 to 72nm feature sizes
- There is a reduction in the SEU cross section at high LETs for 50nm feature size and increase cross section at 25nm



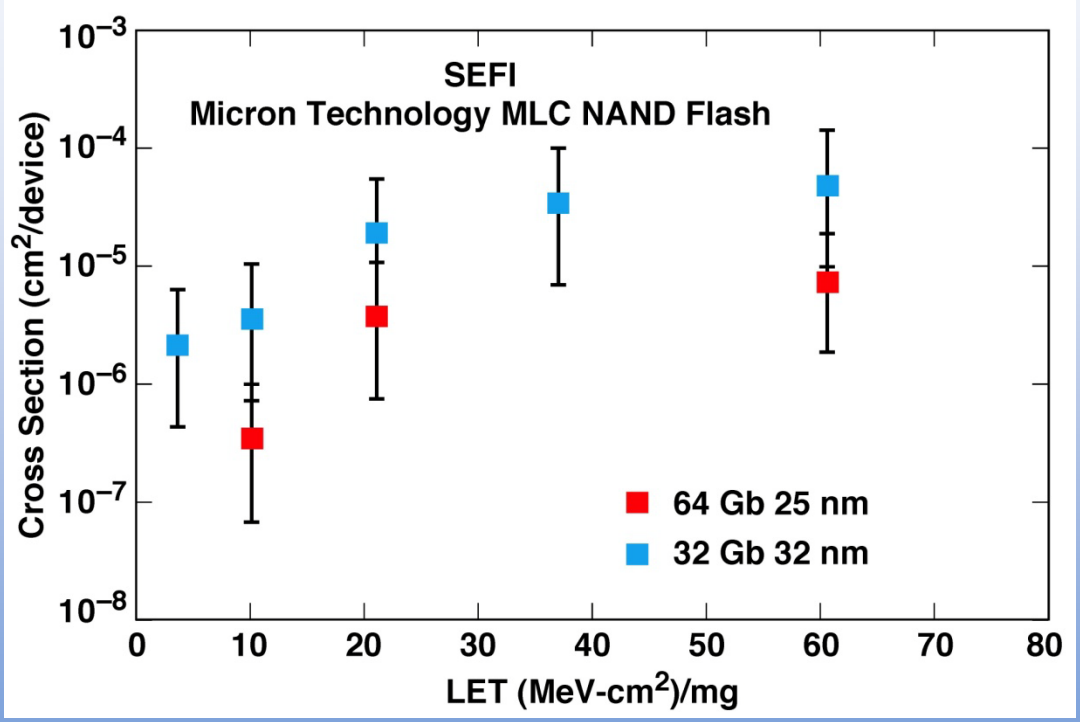
SEU cross-sections for Micron SLC NAND flash memories. Error bars are smaller than the plotting symbols

Single Event Upset Results Scaling



Scaling effect of FG SEU cross-section for Micron MLC NAND flash memories. Error bars are smaller than the plotting symbols

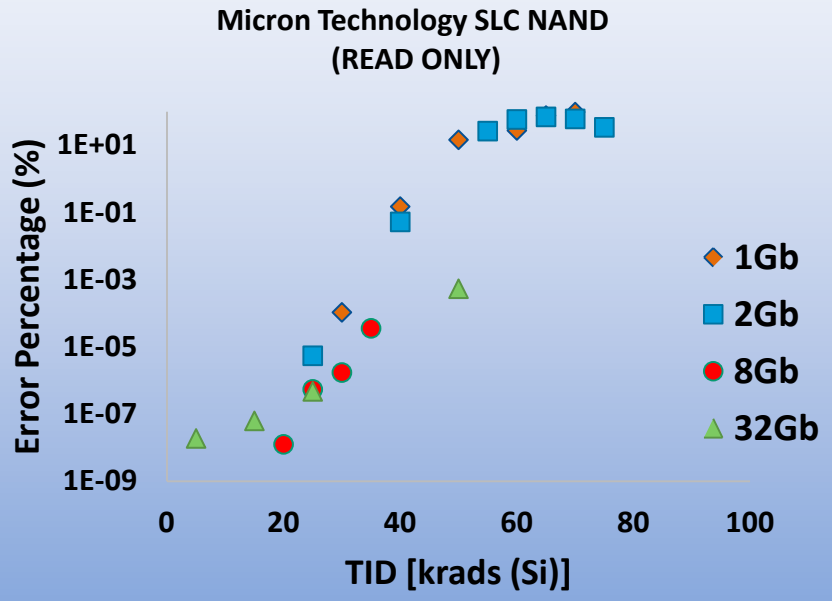
Single Event Upset Results Scaling



Scaling effect of SEFI cross-section for Micron MLC NAND flash memories

TID Results Scaling

- The SLC parts (1, 2, 4, 8 and 32Gb) were irradiated up to 80 krad
- For a particular TID level, the number of errors scales with feature size



Percentage of data errors versus dose for Micron Technology 1, 2, 8 & 32Gb SLC NAND flash memory

Conclusion

- The FG SEU cross section doesn't scale with feature size, except for SLC 8-32Gb devices which are built with 51-25 nm feature size. The FG SEU per bit cross section for SLC 1Gb device which is built with 120 nm feature size is 60% higher than SLC 32Gb device which is build with 25nm at high LETs

- No change in threshold LET was noticed in the range of 120-25 nm feature size

- In general the TID response improves with scaling