NEPP Electronic Technology Workshop
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National Aeronautics
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Single-Event Effects in Silicon Carbide Power Devices

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List of Acronyms

- BJT – Bipolar Junction Transistor
- BVdss – Drain-to-Source Breakdown Voltage
- ETW – Electronic Technology Workshop
- GaN – Gallium Nitride
- GRC – Glenn Research Center
- GSFC – Goddard Space Flight Center
- JFET – Junction Field-Effect Transistor
- JPL – Jet Propulsion Laboratory
- JSC – Johnson Space Center
- LBNL – Lawrence Berkeley National Laboratory Facility's 88-Inch Cyclotron
- LET – Linear Energy Transfer
- MOSFET – Metal Oxide Semiconductor Field Effect Transistor
- NEPP – NASA Electronic Parts and Packaging program
- NSREC – Nuclear and Space Radiation Effects Conference
- PIGS – Post-Irradiation Gate Stress
- SiC – Silicon Carbide
- SEE – Single-Event Effect
- TAMU – Texas A&M University's Radiation Effects Facility
- TID – Total Ionizing Dose
- V_{GS} – Gate-source voltage
- V_{DS} – Drain-source voltage

Wide Band Gap Working Group: Collaborators and Areas of Focus

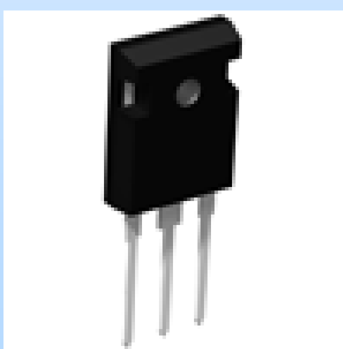
- JPL: GaN radiation performance and overall reliability
  - Leif Scheick (Working Group Chair)
  - Rick Harris
  - Steve McClure
  - Doug Sheldon
- GSFC: SiC radiation performance
  - Megan Casey
  - Jean-Marie Lauenstein (GSFC Task Lead)
  - Ken LaBel
  - Mike Sampson
- GRC: Thermal ruggedness
  - Dick Patterson
  - Ahmad Hammoud
- JSC
  - Chuck Bailey

Working Group Purpose

- Explore opportunities for collaboration to leverage strengths of different Centers
- Share test data between Centers and avoid duplicative efforts
- Assist in test planning and analyzing test data
- Identify devices of interest and assist with vendor contacts
- Increase Technology Readiness Level of devices to foster use by flight projects

GSFC Goals and Expected Impact

- **Evaluation of SiC power devices for space applications**
  - Research new and emerging manufacturers
  - Develop relationships with SiC device suppliers
  - Investigate SEE and TID susceptibility of currently available commercial products
- **Identify possible radiation tolerant power MOSFET alternatives for the space environment**
- **Strengthen existing and foster new relationships with industry**



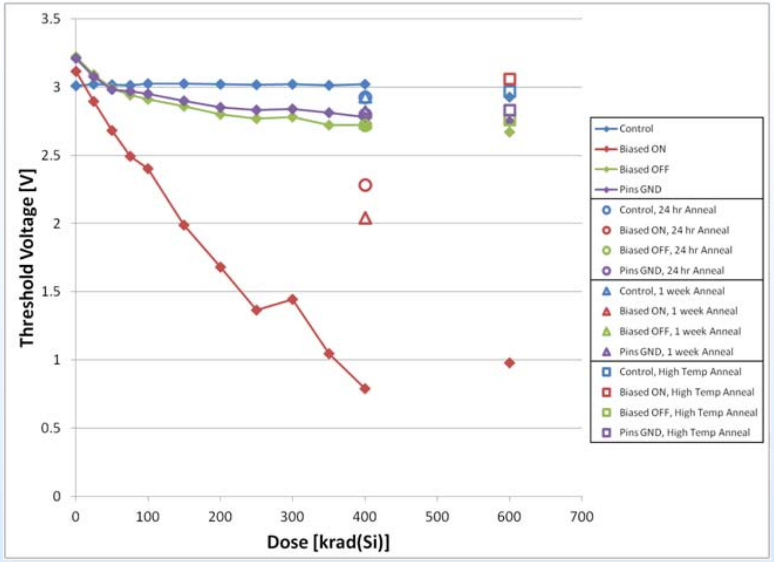
Rohm

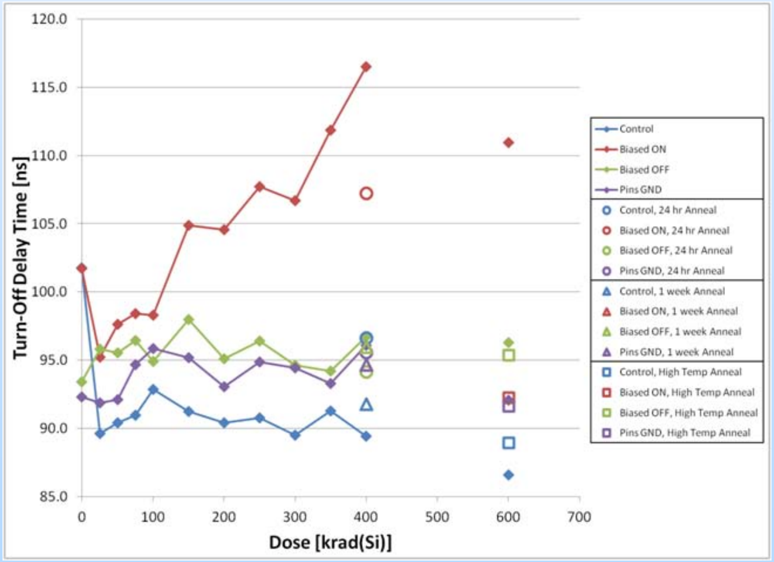
Micross

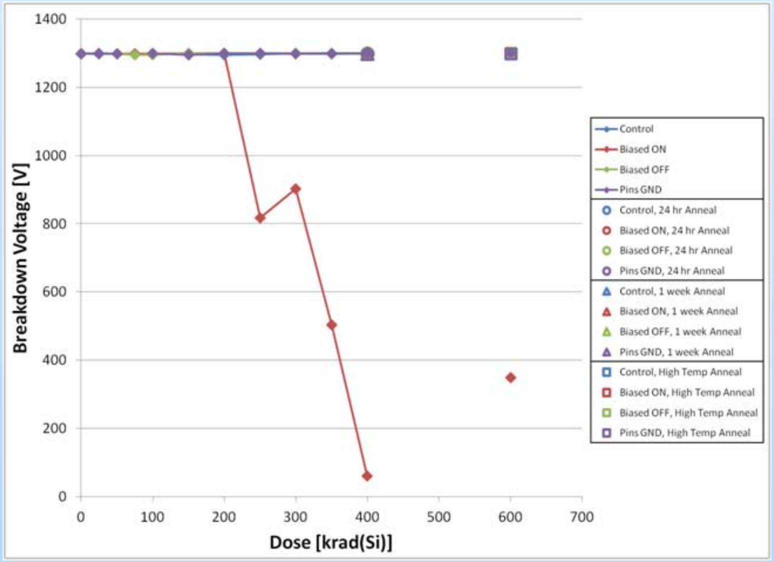
Cree

Recap: Cree CMF20120D SiC Power MOSFET TID Test Results

- **TID test completed during FY12**
- **Small sample size and large part-to-part variability**
- **All parameters, except breakdown voltage, stayed within "specification" to 600 krad(Si)**
  - Most parameters list a typical value and do not have a minimum or maximum



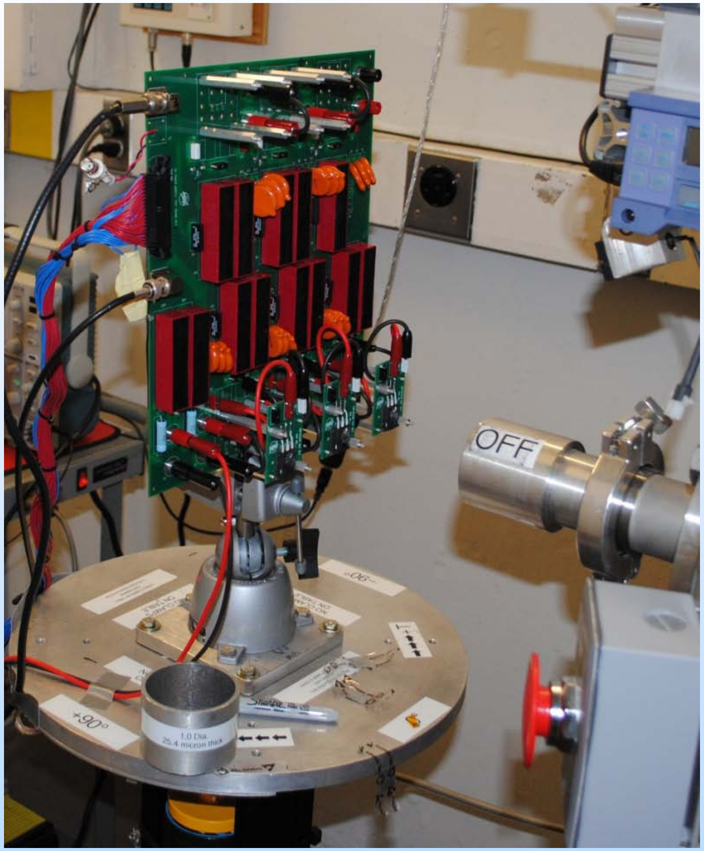




All charts from M. C. Casey, *NEPP ETW*, 2012.

Status

- **Accomplishments**
  - Heavy ion tested a variety of SiC power devices
    - Cree CMF10120D 1200 V Power MOSFET
    - Cree CMF20120D 1200 V Power MOSFET
    - SemiSouth SJEP120R100 1200 V JFET
    - SemiSouth SJEP170R550 1700 V JFET
    - TranSiC BT1206 1200 V BJT
  - SEE data will be presented at the 2013 NSREC in San Francisco, CA



Test Facilities

Facility	Ion	Energy (MeV)	LET at Normal Incidence (MeV-cm^2/mg)	Range in Si (µm)
TAMU	Ar	944	5.6	193
	Kr	1914	20.3	136
LBNL	Ar	400	9.7	130
	Kr	886	30.9	113
	Xe	1232	58.8	90

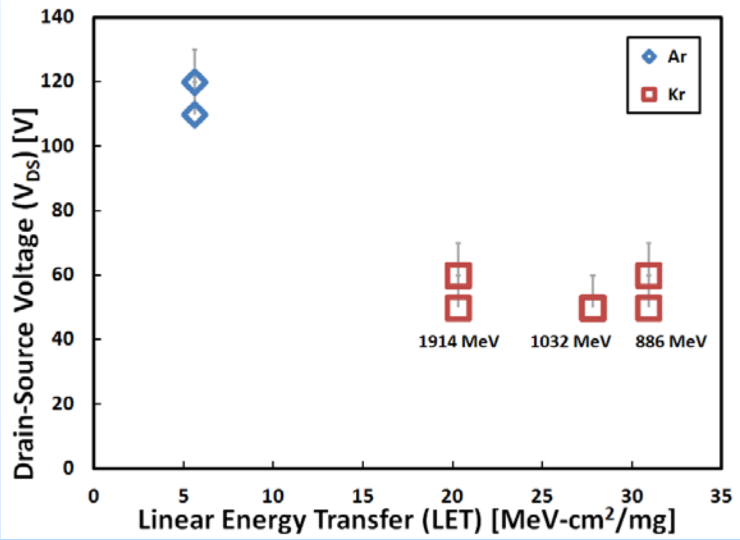
– The fluxes used ranged from 5×10^3 to 1×10^4 particles/cm^2-s.
– Fluences were the lesser of 3×10^5 particles/cm^2 or when a failure was observed.
– Additional LET values were obtained by changing the angle of incidence of the ion beam.

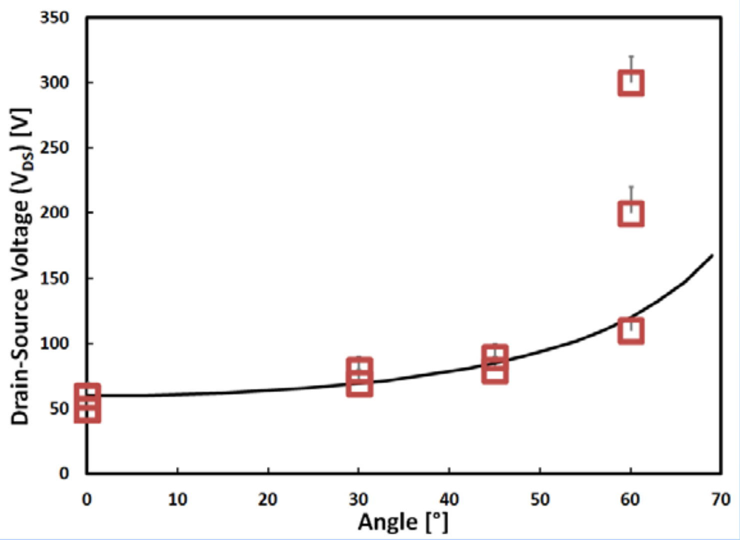
Test Procedure

- Parts are irradiated with heavy ions in the OFF state
  - V_{GS} is held at 0 V and V_{DS} is held constant during the irradiation, and then increased stepwise until a failure is observed
  - V_{DS} is held at 0 V and V_{GS} is constant during the irradiation, and then stepped in the negative direction until a failure is observed
- After each irradiation, a PIGS test was completed for the MOSFETs and the BVdss was measured
  - There are no gate oxides in JFETs or gates in BJTs, so PIGS testing was not conducted on these devices

Cree CMF20120D – 1200 V, 42 A, 80 mΩ n-channel MOSFET

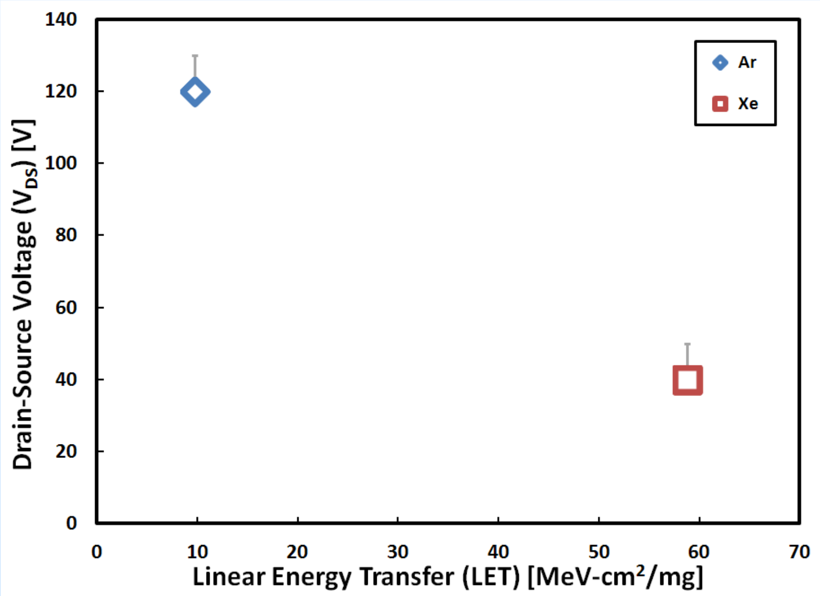
- Irradiated at LBNL and TAMU
- Last passing V_{DS} was 110 V at 944 MeV Ar and 50 V at various energies of Kr (V_{GS} = 0 V)
- No appearance of failure during irradiation
  - During PIGS test was gate found to be broken
  - Large decrease in BVdss was also observed
- Parts follow the cosine law when irradiated at angle
  - Shadowing of die observed at high angles – accounts for large part-to-part variability

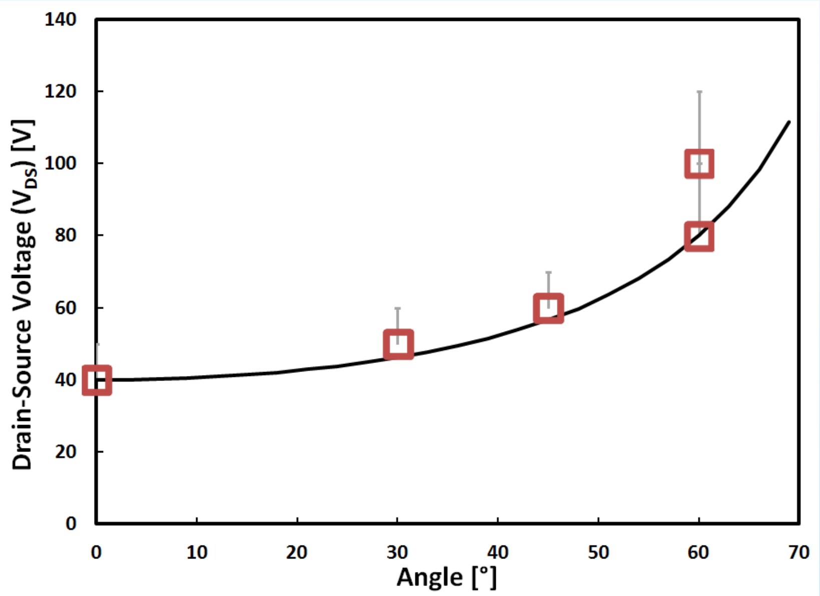




Cree CMF10120D – 1200 V, 24 A, 160 mΩ n-channel MOSFET

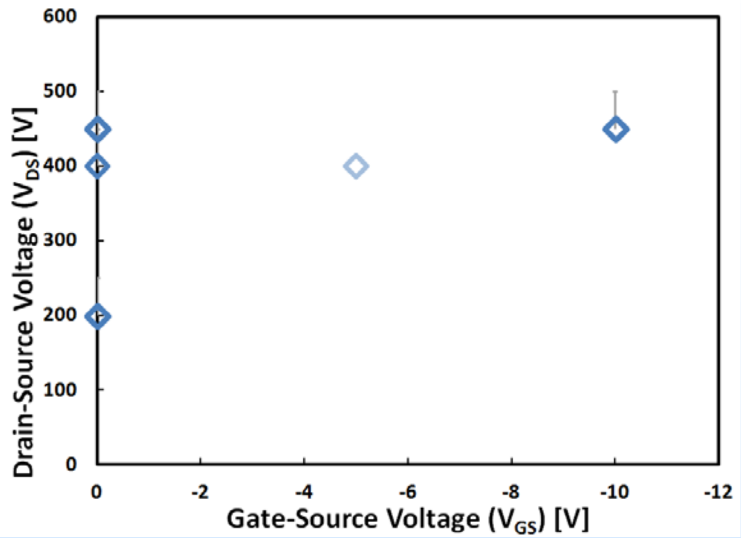
- Irradiated at LBNL
- Last passing V_{DS} was 120 V at 400 MeV Ar and 40 V at Xe (V_{GS} = 0 V)
  - Similar performance to the CMF20120D

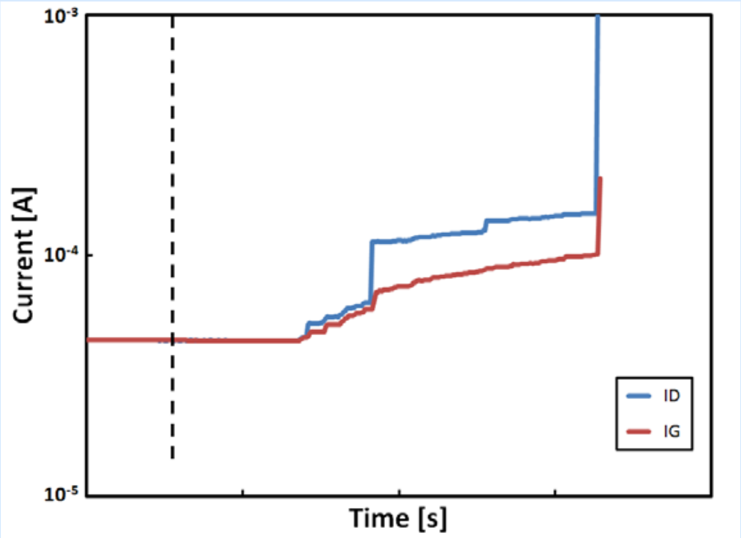




SemiSouth SJEP120R100 – 1200 V, 100 mΩ Normally-Off Trench JFET

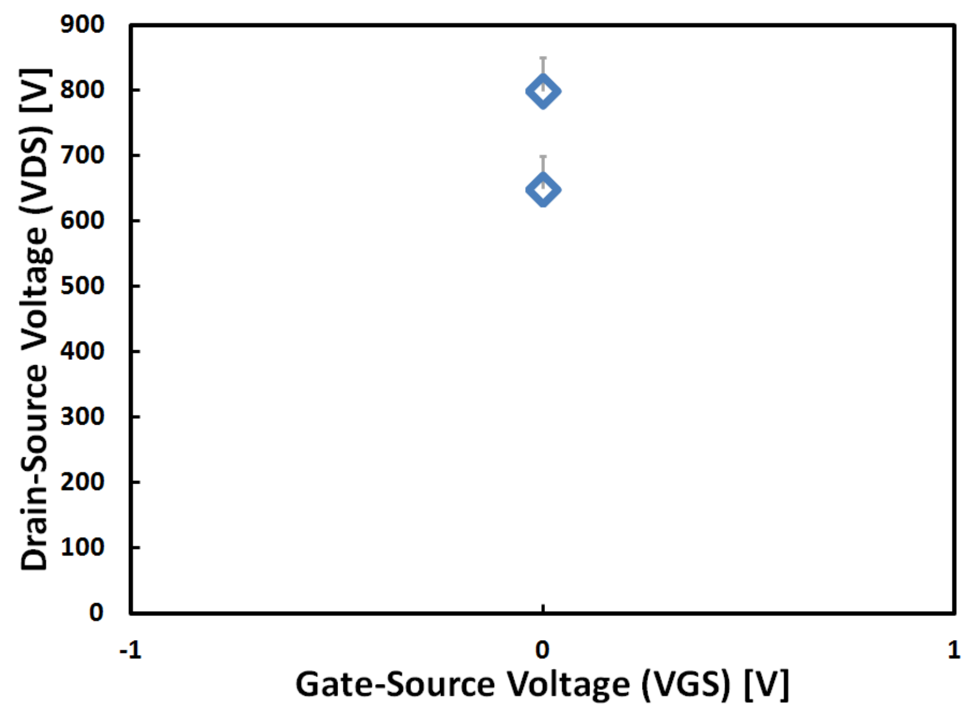
- Irradiated at TAMU
- Last passing V_{DS} (V_{GS} = 0V) was 400 V at 944 MeV Ar and 450 V when V_{GS} = -10 V
- Failure was observed during irradiation
- Large decrease in BVdss was observed





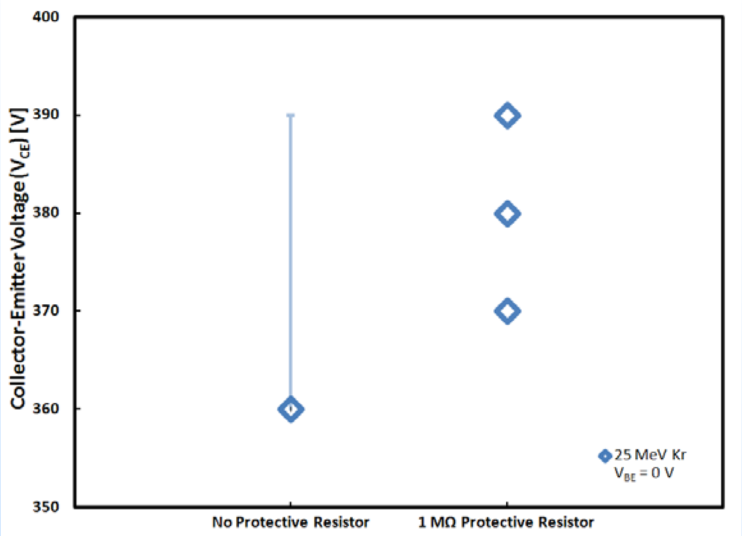
SemiSouth SJEP120R100 – 1700 V, 550 mΩ Normally-Off Trench JFET

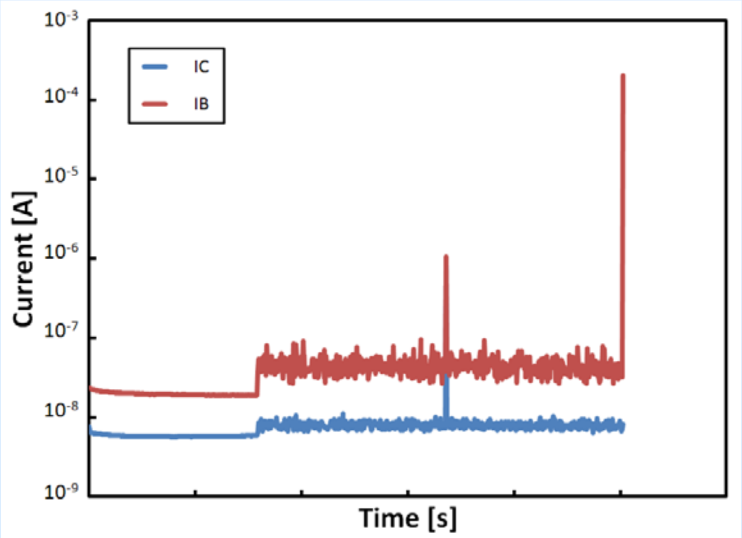
- Irradiated at TAMU
- Last passing V_{DS} (V_{GS} = 0V) was 650 V at 400 MeV Ar
- Failure was observed during irradiation
- Large decrease in BVdss was observed



TranSiC BT1206 – 1200 V, 6 A NPN BJT

- Irradiated at TAMU
- Last passing V_{DS} with a 1 MΩ protective resistor was 370 V at 1914 MeV Kr, and 360 V when no protective resistor was present
- Failure was observed during irradiation
  - Large current spikes were also observed that indicated possible failures absent the protective resistor





Conclusions and Path Forward

- SiC devices show high TID tolerance, but low SEE tolerance
  - Similar problems were initially observed in Si MOSFETs
  - Hardening requires a trade-off in electrical performance
- Plan to test SJEP170R550 JFETs for TID performance
  - Anticipate good results due to SiC and lack of gate oxide inherent to JFETs
- Collaborating with Solar Electric Propulsion technology demonstration mission to identify candidate electronics for testing
  - Investigating additional commercial SiC MOSFETs and Schottky diodes