National Aeronautics and Space Administration

NASA Evaluation of Automotive Grade Microcircuits

NASA Electronic Parts & Packaging Program (NEPP) Electronics Technology Workshop (ETW)

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The outer zones of the solar system, which Voyager 1 has traversed to enter interstellar space.
Courtesy NASA/IBEX/Adler Planetarium

Evaluation of Automotive Grade Microcircuits

- **This talk will give status of the work being performed at**
  - Navy Crane, Indianapolis, Indiana
  - DPA Components International in Simi Valley, California
  - All parts are in plastic packages

Automotive Grade Parts Evaluation at Navy Crane

- **Navy Crane**
  - Joint NASA/Navy Crane Effort
  - Coordinated by Josh Gray of Navy Crane
  - Limited funds
  - Three commodities being evaluated.
    - Passives
      - ❖ Led by Jay Brusse (NASA/GSFC)
    - Discrete Semiconductors
      - ❖ Led by Benny Damron (NASA/MSFC)
    - Microcircuits
      - ❖ Led by Shri Agarwal (NASA/JPL)
  - Periodic telecons are held
    - Participants: J. Gray, J. Brusse, B. Damron, S. Agarwal, M. Sampson, C. Barnes

Automotive Grade Microcircuits Evaluation at DPACI

- **DPA Components International (DPACI)**
  - NASA/JPL contract at DPACI to
    - Evaluate a digital IC from a high volume auto parts supplier
  - Status
    - Parts on order
    - Developing electrical test program

Microcircuits
Planned Evaluation

- **The microcircuits evaluation is divided into four phases**
  - Phase I.
    - Assess quality (of parts as received)
      - 100% Electrical testing
      - Sample DPA
  - Phase II.
    - Assess infant mortality
      - 100% screening
  - Phase III.
    - Assess reliability
      - Sample life test
  - Phase IV.
    - Additional Quality Conformance Inspection (QCI) tests
      - TBD

Automotive Grade Microcircuits Evaluation
Parts Selection

- **Vendor / Part Type Selection**
  - Texas Instruments (TI).
    - Linear function
    - Digital function
  - Analog Devices, Inc. (ADI)
    - Linear
  - ON Semiconductor (ON)
    - Digital function
  - MSI complexity
    - Minimum time for test program development

NEPAG

From Discussion on Automotive Parts

- **Existing automotive parts market**
  - Plastic packages
  - No screening is done
  - Much testing is done at the wafer level
  - Limited qualification
  - The customer must enforce any desired requirements
  - Manufacturers self certify—no DLA-type regulators
  - The system works because of **high-volume production**—That is the customer's power to enforce upgrades
- **Microcircuit Evaluation is in progress (2014)**
  - In progress
  - Screening and qualification are planned
    - ❖ Qualification will be limited to life test

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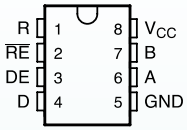
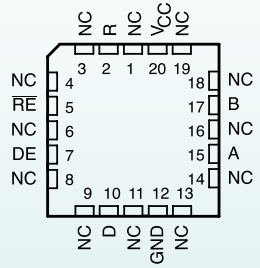
- **Bidirectional Transceiver**
- **Meets or Exceeds the Requirements of ANSI Standard TIA/EIA–485–A and ISO 8482:1987(E)**
- **High-Speed Low-Power LinBiCMOS™ Circuitry**
- **Designed for High-Speed Operation in Both Serial and Parallel Applications**
- **Low Skew**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Very Low Disabled Supply Current . . . 200 μA Maximum**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Thermal-Shutdown Protection**
- **Driver Positive-and Negative-Current Limiting**
- **Open-Circuit Failsafe Receiver Design**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC176, SN65LBC176, SN65LBC176Q, and SN75LBC176 differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet ANSI Standard TIA/EIA–485–A (RS-485) and ISO 8482:1987(E).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{IA} - V_{IB}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

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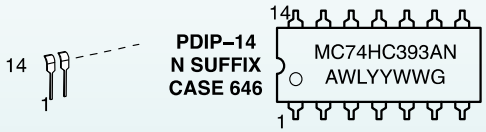
meters.



(Note: Microdot may be in either location)

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ANALOG DEVICES

Data Sheet

Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifier

w SOIC and
14-lead TSSOP plastic packages. See the Ordering Guide for
automotive grades.

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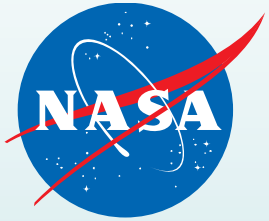
ers.

http://nepp.nasa.gov



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