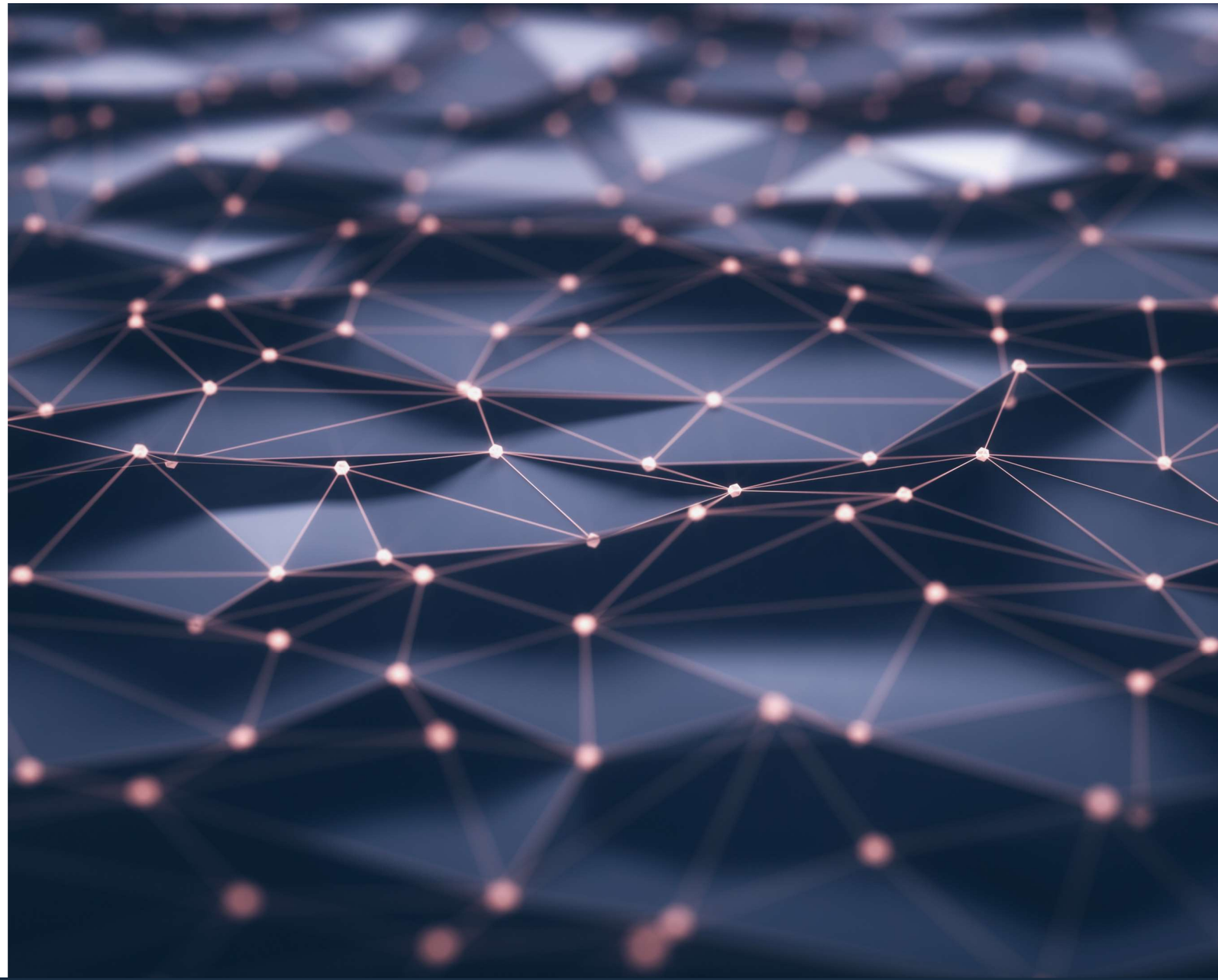
POLARIS
ALPHA
a PARSONS Company

NASA Electronic Parts and Packaging (NEPP) Program - 2018 Electronics Technology Workshop

Printed Hybrid Electronics (PHE)

June 19, 2018



AGENDA

- Corporate Overview
- Technology Comparison: PHE vs. PCB
- QRC PHE Initiative
  - Capability Development Cycle
  - Phase 1 Goals
  - Printed MCM Demonstrator: HERCULES
  - PCB Repair
  - Ink Characterization
  - Phase 2 Plans
- Questions

POLARIS ALPHA: CORPORATE OVERVIEW

200+ HIGHLY CLEARED CYBER PROFESSIONALS

SOPHISTICATED C5ISR, EW & SENSOR PROTOTYPING/INTEGRATION FACILITIES

30+ AMAZON WEB SERVICES (AWS) CERTIFIED ARCHITECTS AND DEVELOPERS

300 TECHNICAL PROFESSIONALS SUPPORTING SPACE AND CYBER PROGRAMS

19,000 SQUARE FOOT ACCREDITED SCIF SPACE

QUICK REACTION CAPABILITY (QRC) SERVICES

- Founded in 2016 when 4 successful companies, EOIR, ISS, INTELESYS and PROTEUS Technologies came together to form an agile, high-tech solutions provider
- Expanded in 2017-2018 with SOLIDYN SOLUTIONS and FOURTH DIMENSION ENGINEERING to establish one cohesive mid-tier leader
- Acquired in 2018 by PARSONS
- Critical mass in emerging warfighter domains (cyber, space, and the electromagnetic spectrum)
- Broad experience in research and development as well as operationally-fielded systems
- Employs over 1,300 technical experts with deep subject matter expertise worldwide
- Broad portfolio of IP including software and hardware products
- ~$340 million of 2018 forecasted pro forma revenue

CYBER & SIGINT: BRIDGING SOLUTIONS

- Rapid-Turn Hardware Development & Manufacturing
  - Custom Microelectronics (ASIC, Multi-Chip Modules)
  - Low Volume, High Mix (200+ unique PCB designs/year)
  - High Reliability, Long Life (15+ years)
  - Information & IP Sensitive Customers – Government & Commercial (Trusted, Domestic Vendor Base)
  - Perform in space between Capability Development & Mission Implementation
- Reverse Engineering & Vulnerability Analysis
- Test Design & Execution (Functional Verification, Environmental, RF)

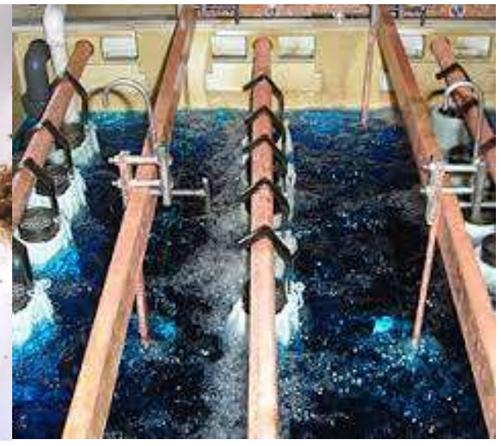
Quick Reaction Capability (QRC) Mission

- Project durations ranging from 24 hours to 6 months
- 300+ QRC responses, 1000+ fielded systems since 2009

WHY PRINTED ELECTRONICS? PCB VS. PHE

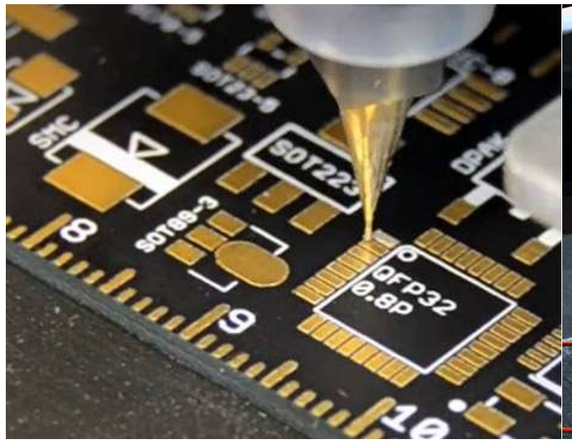
Printed Circuit Board

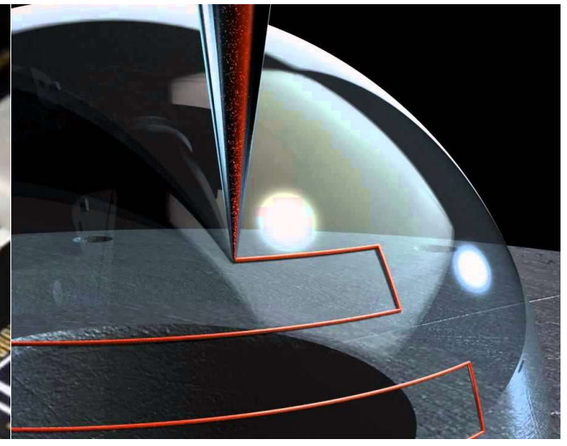
- Imaged, developed and etched (subtractive) foil on dielectric substrate (i.e. organic: glass-reinforced resin composite). Planar construction where multiple layers are achieved through lamination and the use of drilled and plated (additive) interconnecting vias.



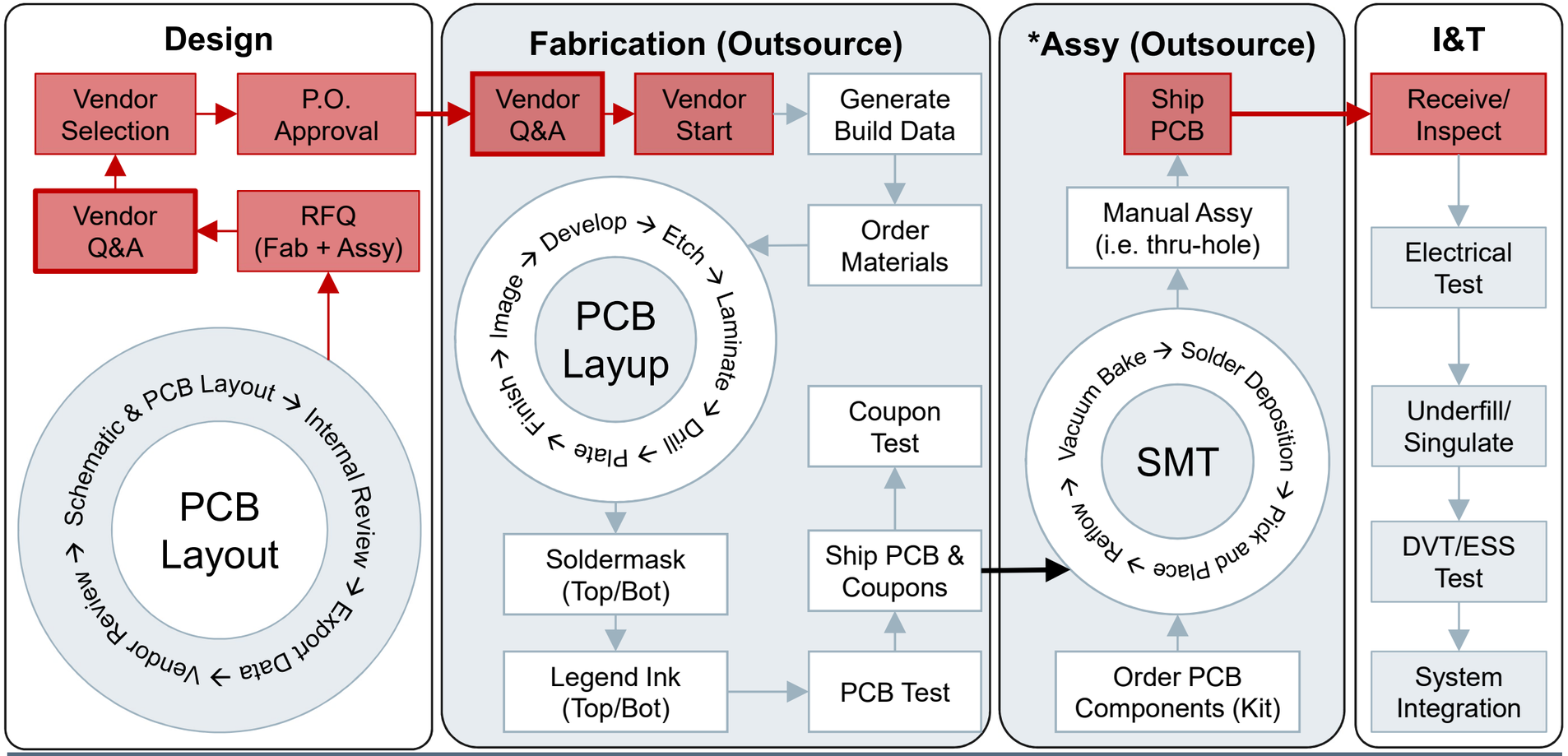
Printed Hybrid Electronics

- Printed layers of filled, conductive ink (i.e. metal, metal oxide) and dielectric resin (additive). Layers can be non-planar (3D construction).



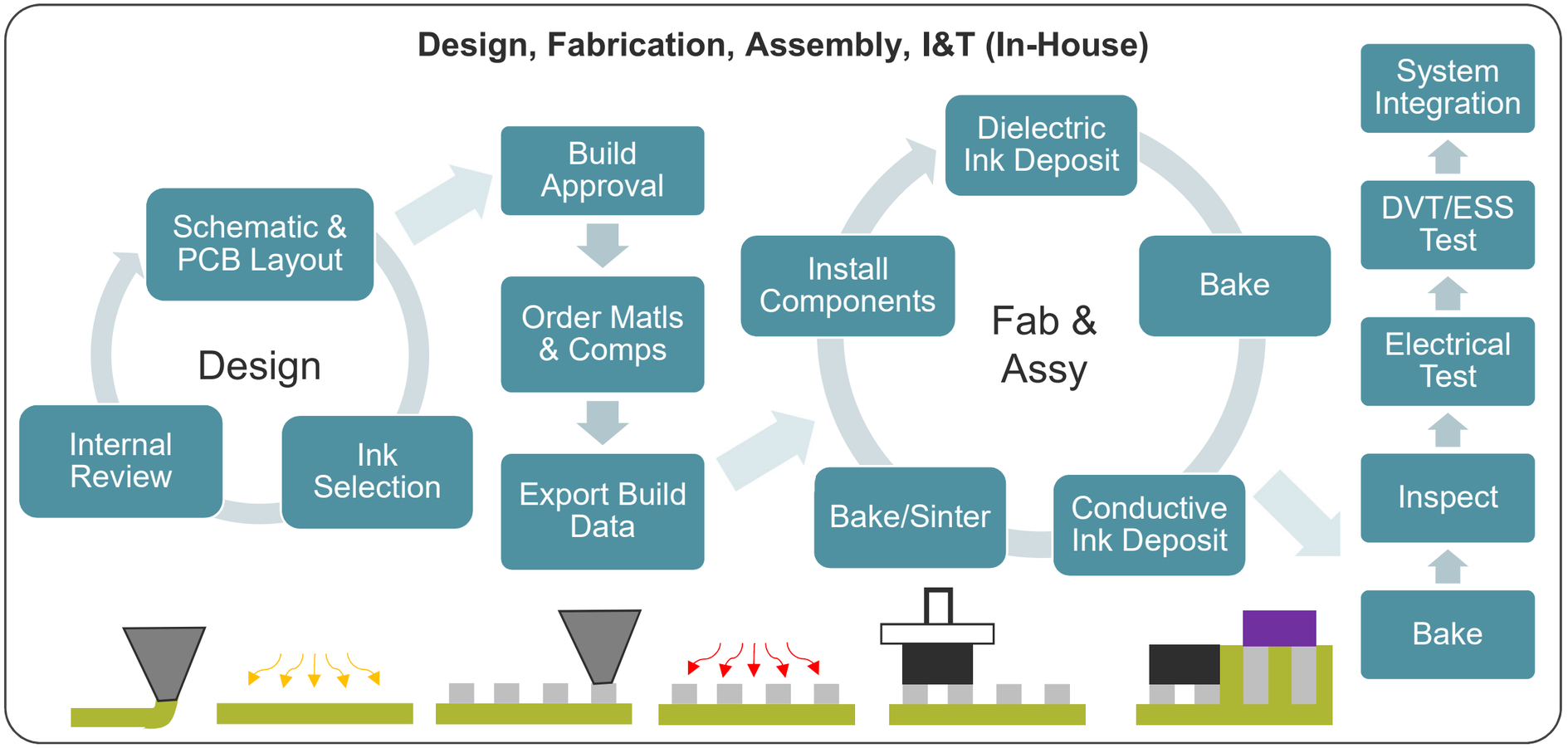


WHY PRINTED ELECTRONICS? PCB PROCESS



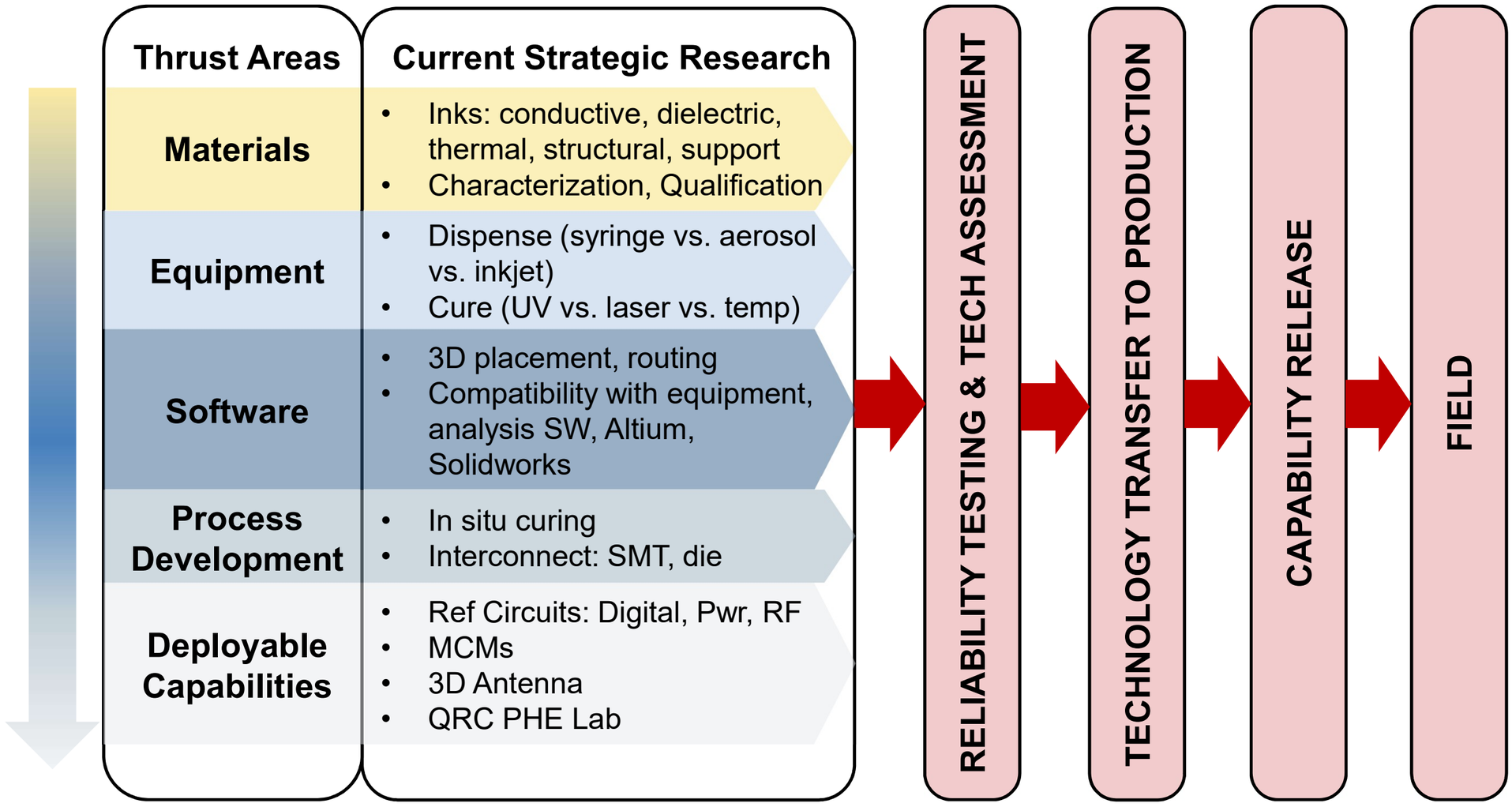
Issues: Outsourcing (Time, Information), Expensive (Volume-driven), Design Limits (Planar, Vendor Rules) *Problem is amplified for chip-level integration

WHY PRINTED ELECTRONICS? PHE PROCESS



Pros: In-house (control IP), Quick-turn & Inexpensive (low volume), Unique 3D Geometries
Cons: Immature Technology, Applications gated by Materials/Equipment/Software R&D

PHE: CAPABILITY DEVELOPMENT CYCLE



QRC PHE INITIATIVE: PHASE 1 GOALS

Establish a quick-reaction capability for the design, manufacture, test and integration of fieldable PHE solutions

- Phase 1 (FY'18) Scope
  - Set up QRC PHE Additive Manufacturing Capability
    - Collaboration with Research Labs
  - Printed MCM (low complexity) – HERCULES
    - Optomec – Aerosol Dispense
  - PCB Repair – Remove/Replace Traces, Apply Legend Ink, Dam & Fill
    - "The Haas" – Syringe Dispense, retrofitted 5-axis CNC mill
    - Image Capture/Stitching/Processing
  - Material Identification & Qualification

PRINTED MCM DEMONSTRATOR: HERCULES-PHE

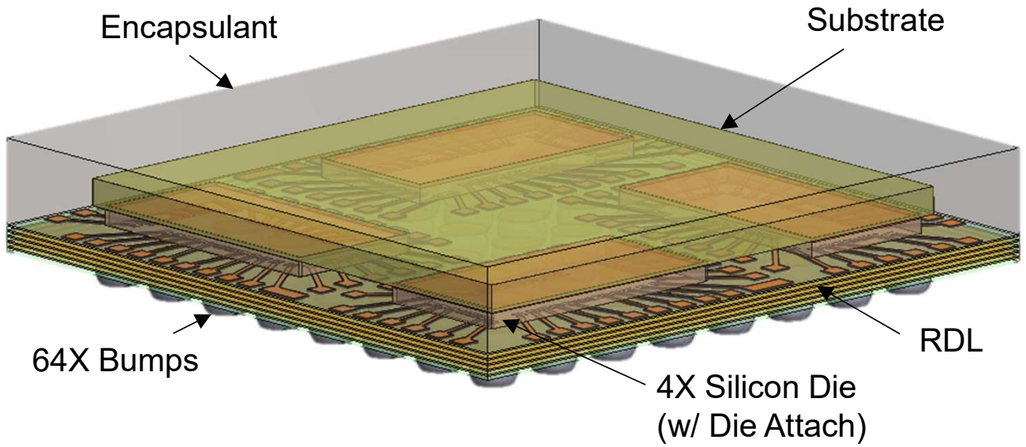
Product: Digital Multi-Chip Module (MCM)

- Low power, low speed, low thermal output
- HERCULES-WB (wirebond) – built/qualified
- HERCULES-FC (flip chip) – currently in fab

Goal: Develop a PHE version of HERCULES that is a drop-in replacement for HERCULES-FC

- Not limited by current material (resistivity, cure)
- In-house, Quick-turn
- Tech Transition: Die & BGA Interconnect

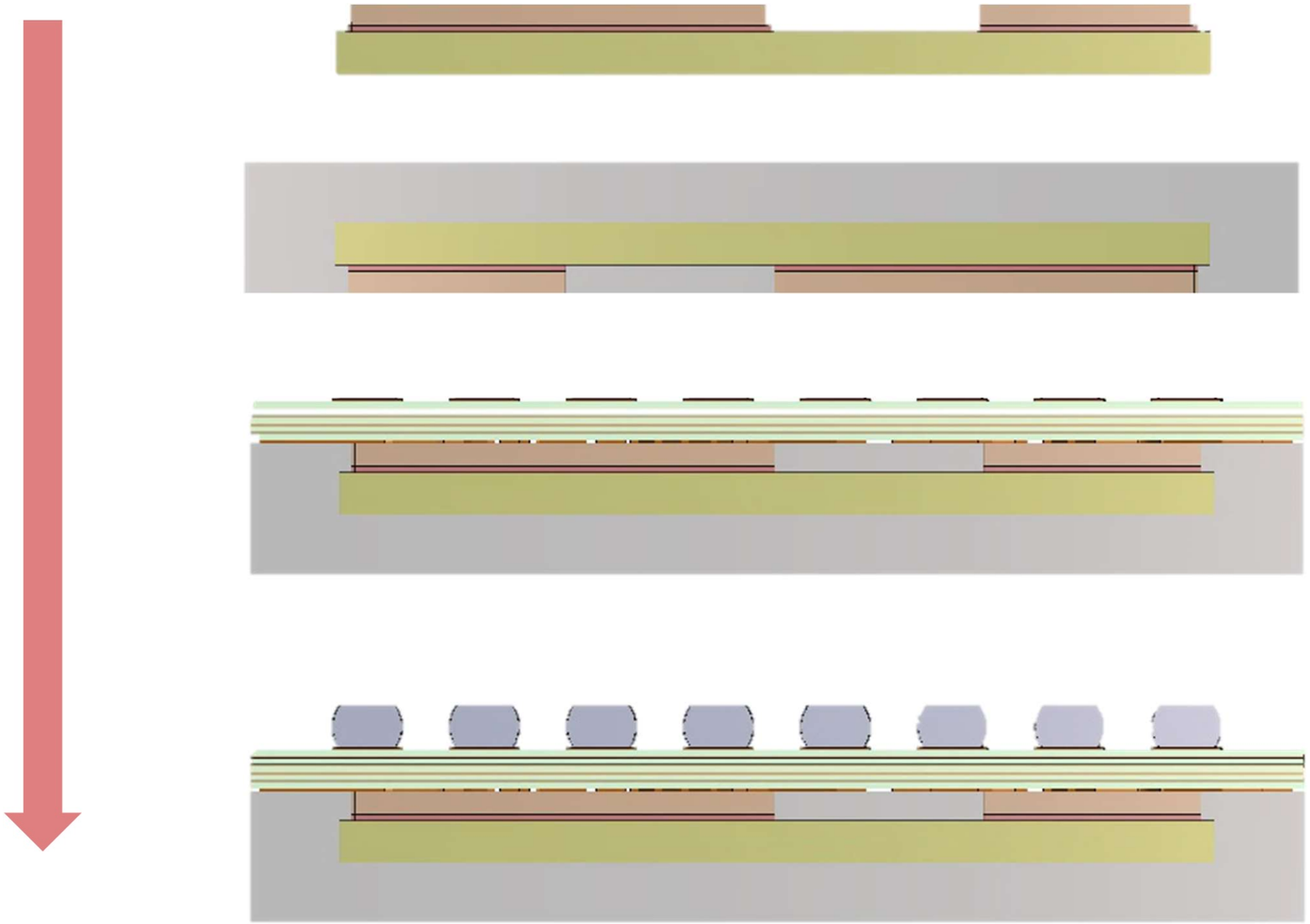
	HERCULES-WB	HERCULES-FC	HERCULES-PHE
Prototype	6wks, $38K	-	<3wk, $20K (est)
Production	3wks, $16K min lot (quote)	-	<2wk, <$12K min lot (est)
Size (mm)	7 x 7 x 1.3	4.5 x 4.5 x 1.2	4.5 x 4.5 x 1.0



Stack-Up

Encapsulant	0.25 mm
Substrate	0.18 mm
Die Attach	0.03 mm
Silicon Die (Qty 4)	0.10 mm
36 I/O per die	
75 µm Sq Pads @ 100 µm Pitch	
Redistribution Layer (13 layers)	0.22 mm
10 µm conductor, 25 µm dielectric	
Metallized Bumps (Qty 64) (0.3 mm diameter)	0.18 mm
Total Thickness	**0.96 mm**

HERCULES-PHE: BUILD SEQUENCE



Die Placement

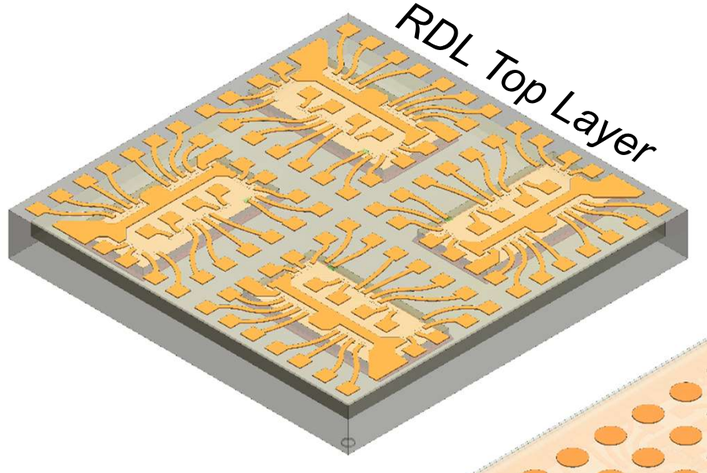
Encapsulation

Print RDL

Bump/Ball

HERCULES-PHE: REDISTRIBUTION LAYER (RDL)

Photo of printed RDL Top (~ 30 um line width)



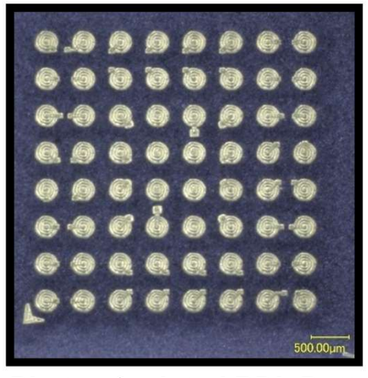
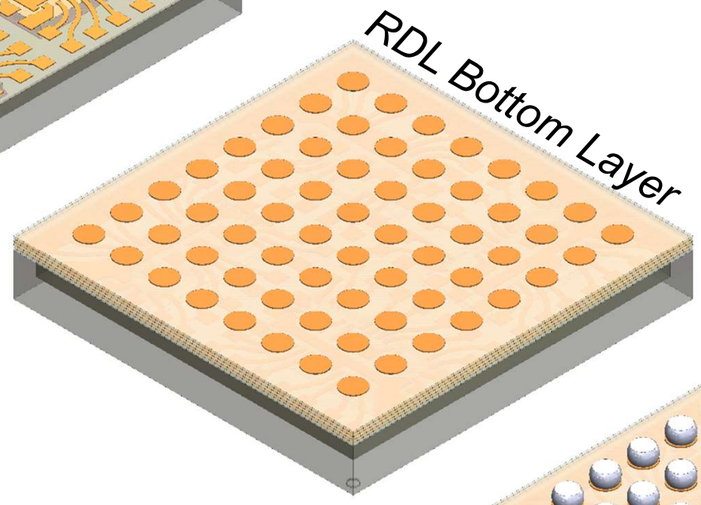
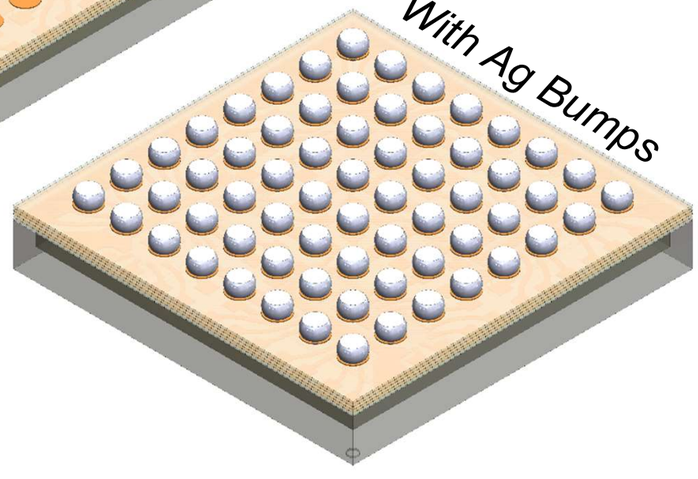


Photo of printed RDL Bottom

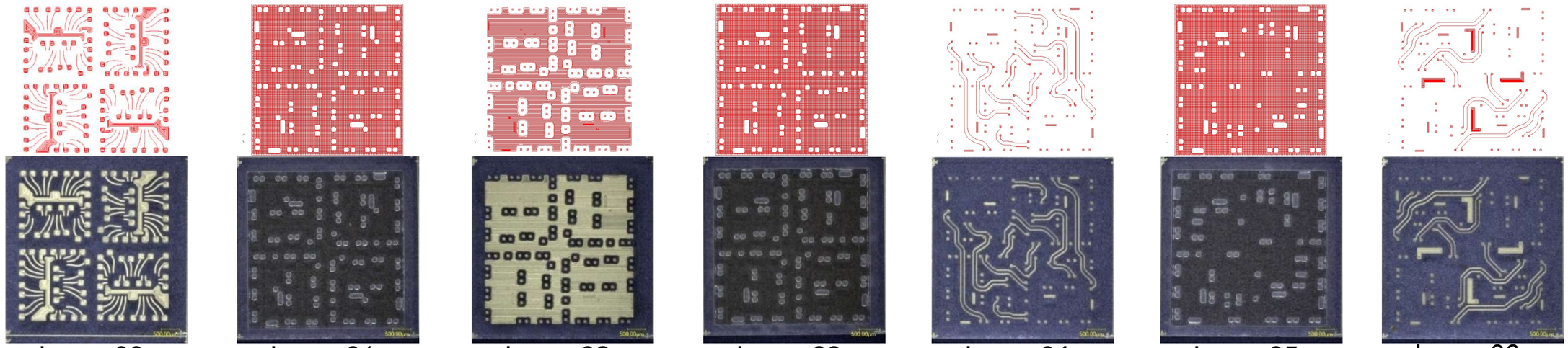




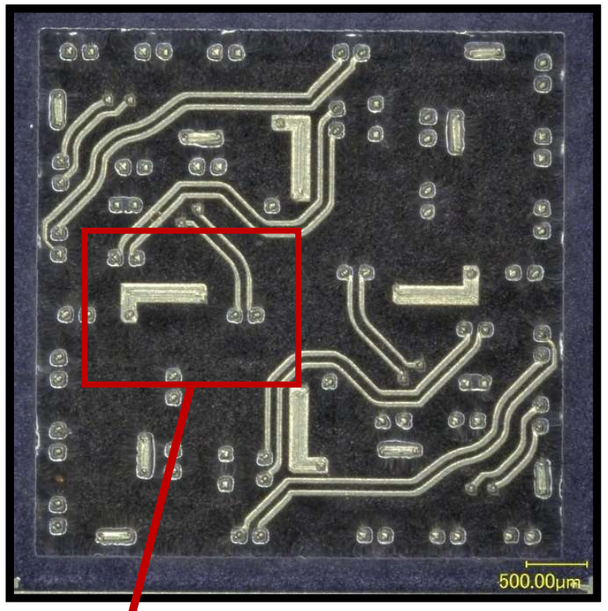
5-Layer Printed RDL

- 13 conductive & dielectric layers
- 13 separate sinter profiles (@ 225°C)
- Estimate ~15 working days to print a batch of HERCULES RDLs with current material set and required cure profile

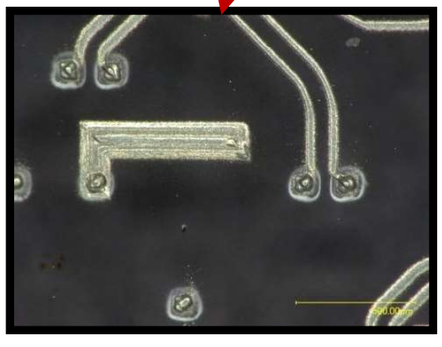
HERCULES-PHE: RDL - CAM TO PRINT COMPARISON

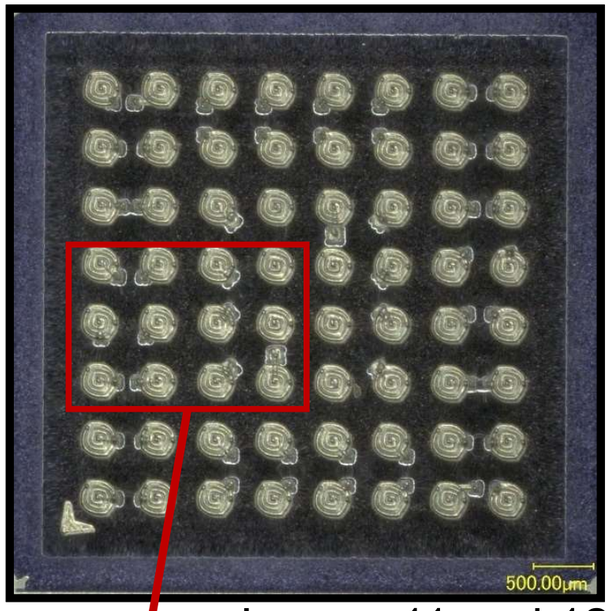


HERCULES-PHE: MULTILAYER SNAPSHOTS

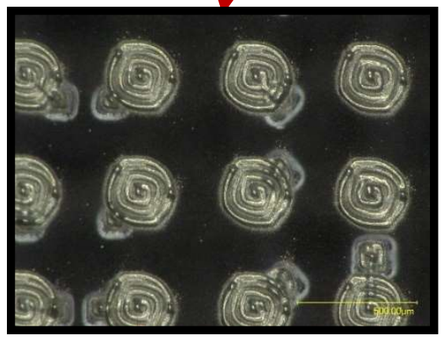


Layers 05 and 06





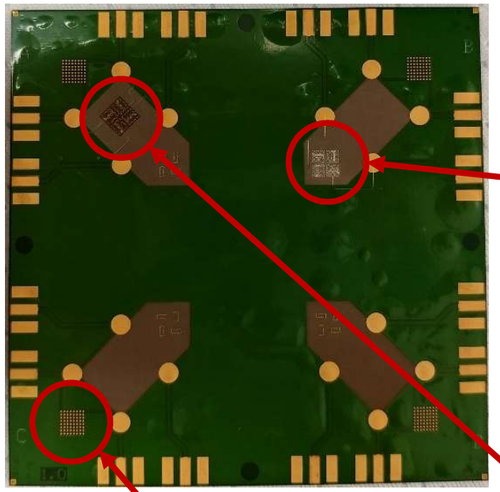
Layers 11 and 12



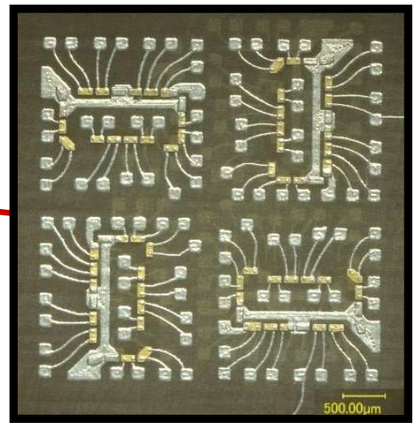
HOTTOPIC: TEST PCB

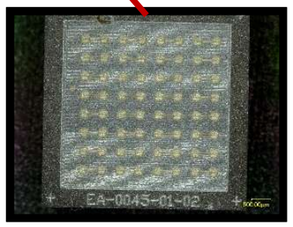
- HOTTOPIC
  - Test substrate for printing and testing daisy chain test constructions, alignment to die pads
  - Also includes a section for developing BGA placement process
  - Evaluate HERCULES RDL in parallel with wafer/die procurement & die block fabrication

HOTTOPIC

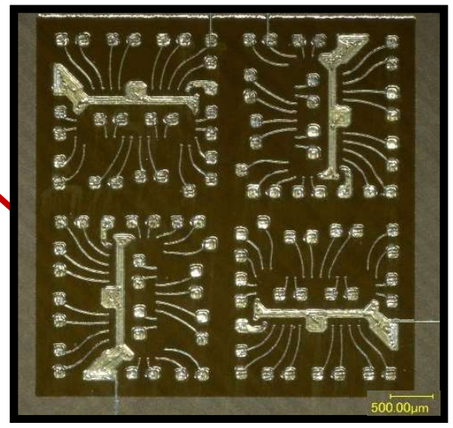


MANICPANIC
(1 of 5 layers)





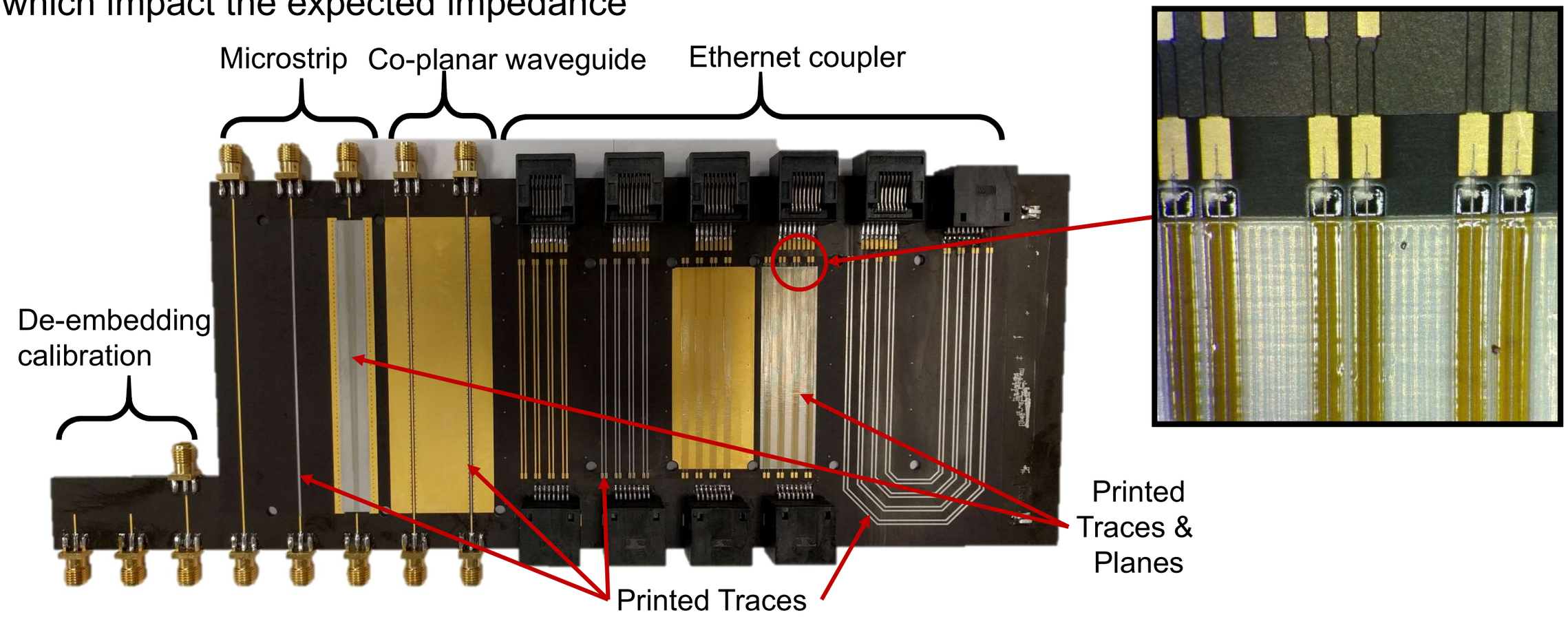
BGA dummy for test site



STUDDEDCHOKER
(2 of 5 layers)

SPEEDBOARD: MATERIAL CHARACTERIZATION FOR HIGH FREQUENCY APPLICATIONS

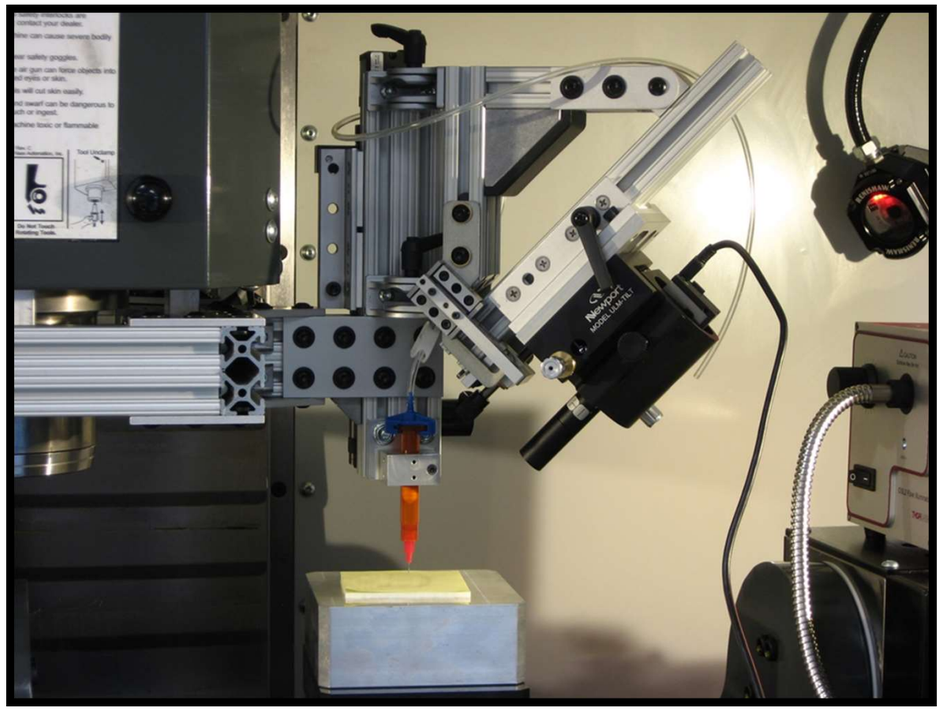
- High frequency design guidance for dielectric / conductor material sets and process variables which impact the expected impedance



PCB REPAIR: 5-AXIS SYRINGE SYSTEM (“THE HAAS”)

- Installation and initial setup of Haas VF-2TR completed
- Spindle grease packed and reinstalled 3/28

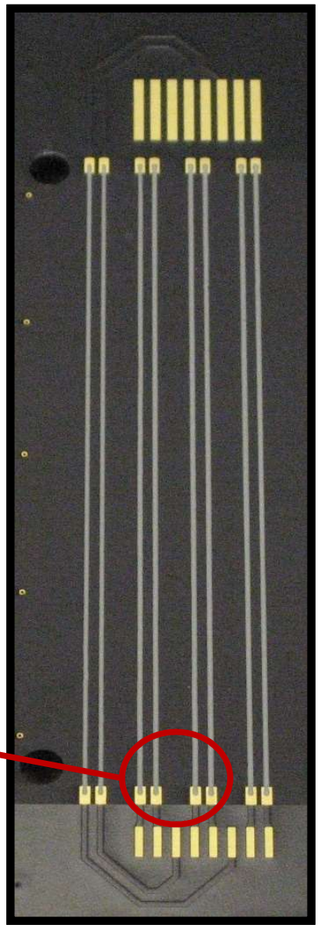
- Completed design and installation of syringe and alignment/in-situ cameras
- In-situ laser sintering system planned for ~ July / August 2018



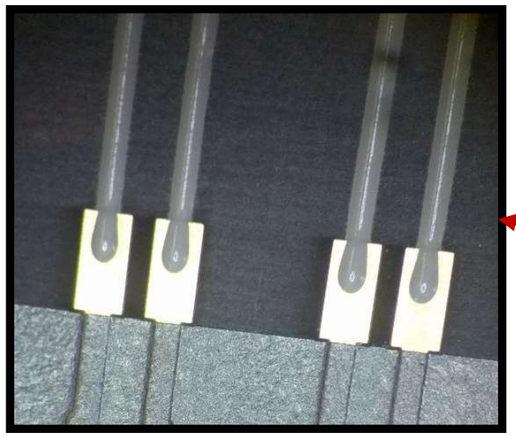
PCB REPAIR: 5-AXIS SYRINGE SYSTEM PRINTS

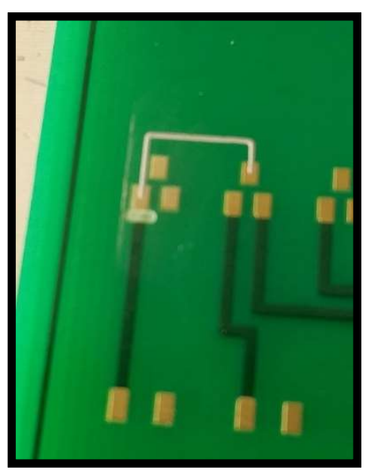
Printed Legend Ink

Printed FP4451
Damming Material



Printed Ag Traces





PCB
Repair
Demo

INK CHARACTERIZATION & SELECTION

Creating repository of ink information as design resource
Standardized ink testing procedure & coupon

Printability

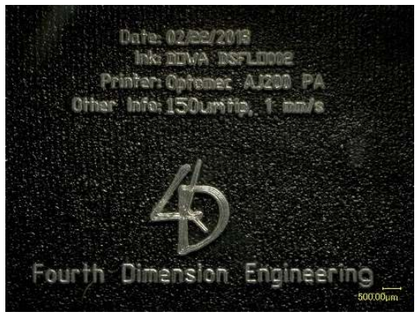
- Coupons for structures, art, lettering
- Long, continuous, reliable prints
- *Optomec, Microscope, & Profilometer*

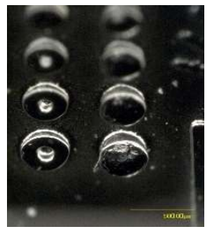
Conductivity

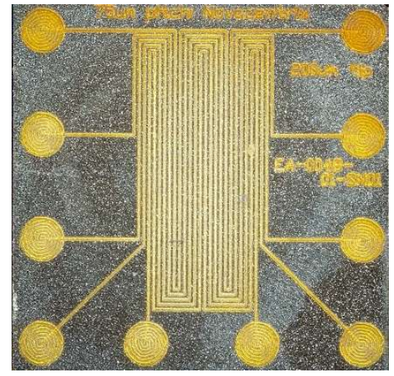
- 4-Point resistivity measurement
- *Current source & voltmeter*

Process Compatibility

- Time (deposition rate)
- Cure method (UV, temp, time)
- Adhesion, etc.







INK PROCESS DEVELOPMENT & QUALIFICATIONS

Ensuring print meets build specifications

Pre-printing

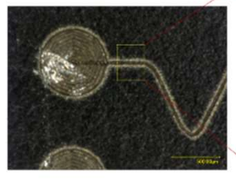
Viscosity
- *Viscometer*

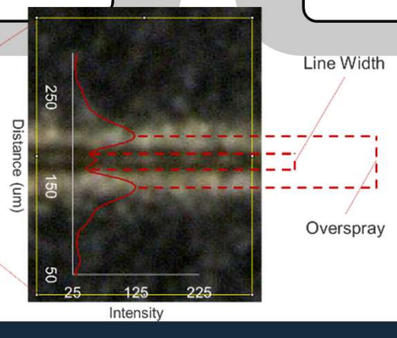
Particle loading
- *Scale, hot plate*

Post-printing

Print quality (overspray, consistency)
- *Microscope, profilometer*

Print dimensions
- *Microscope, profilometer*





Post-curing

Adhesion
- *ASTM D3359-17*

Conductivity
- *Current source & volt meter*

Accelerated life cycle testing

PHASE 2: PLANS

- Printed MCMs
  - Reliability/Life - Extended Qual for HERCULES-PHE
  - Performance - ↑Power, ↑Speed, ↑Thermal Dissipation
  - Turn-Time - Print/Cure Optimization, In-house Equip
  - Material Research/Qual - ↓Resistivity, ↓Process Temp
- Die Interconnects
  - Print to harvested/reclaimed die
  - Eliminate Encapsulation
  - Die Stacking / Flip Chip
- Higher Density Die I/O
  - Print Resolution Target: 10µm
  - New equipment and materials sets required
- PCB Repair (Haas)
  - Reliability/Life – identify/build demonstrator, extended qualification
  - Surface Trace – ↑Power, ↑Speed
  - Interconnects – SMT components, Vias
  - Imaging - High resolution, automated capture/stitching/conversion
  - Material Research: soldermask, adhesive, via fill
- Printed Antennas (2D & 3D)
- Printed Energetics

QUESTIONS?

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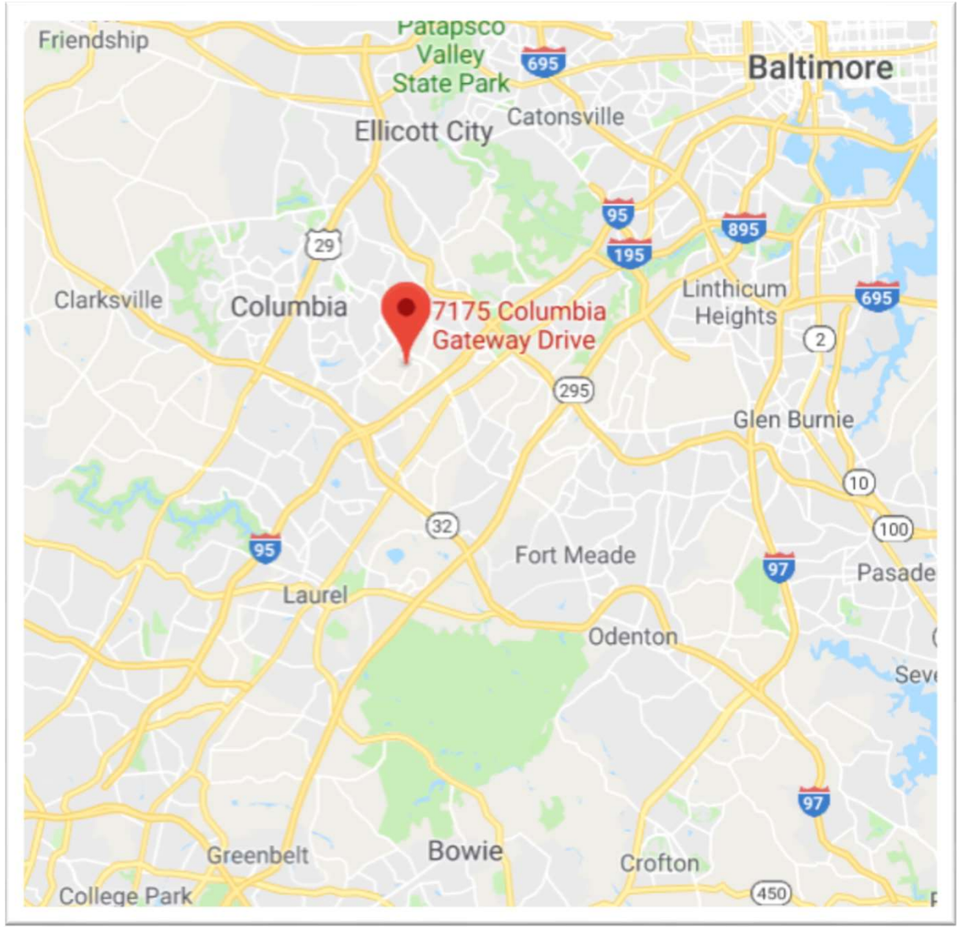
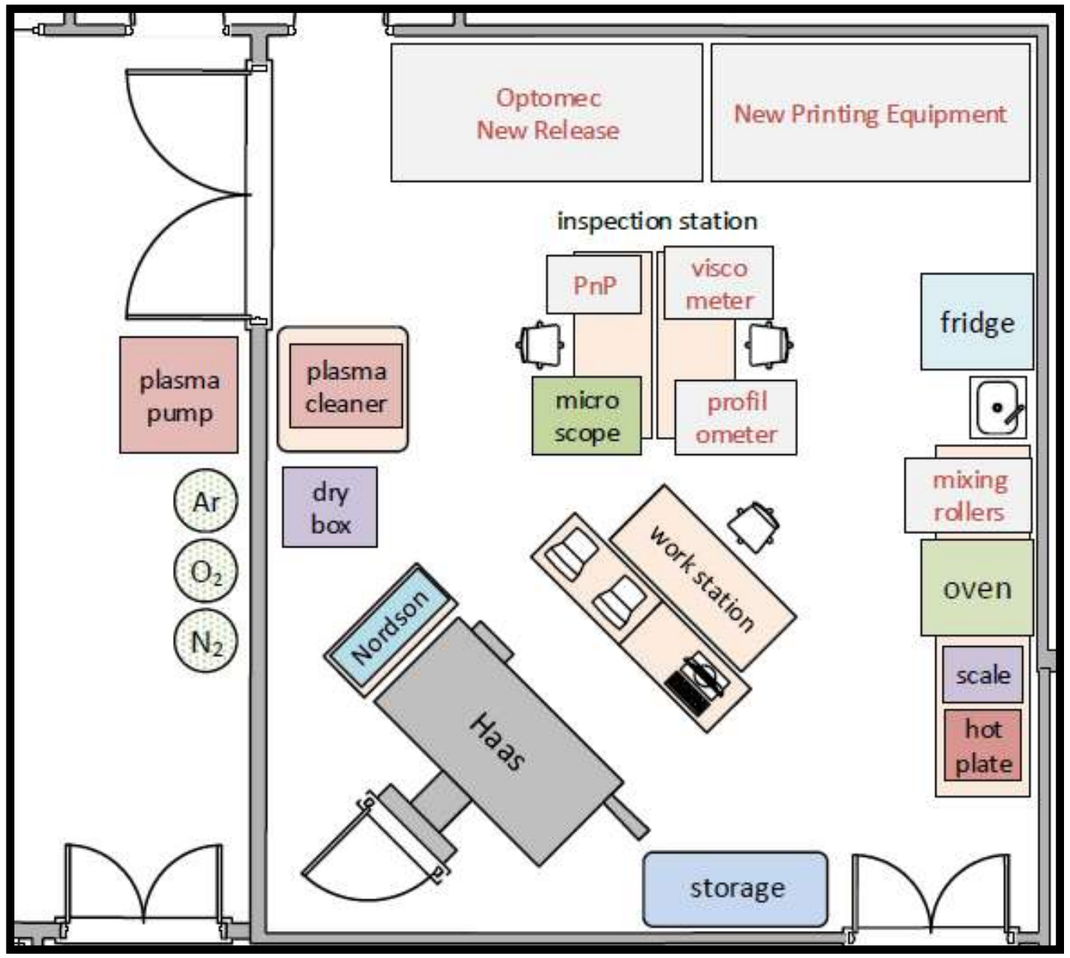


BACK-UP SLIDES

QRC PHE FACILITY & EQUIPMENT



QRC PHE Additive Manufacturing Lab
7175 Columbia Gateway Drive, Columbia, MD

Current (Onsite)

- Haas + Nordson
  - Dielectrics, conductors, legend ink
  - 100µm min. feature size
  - 5-axis movement (3D surfaces)
- X-ray
  - Advanced parts inspection

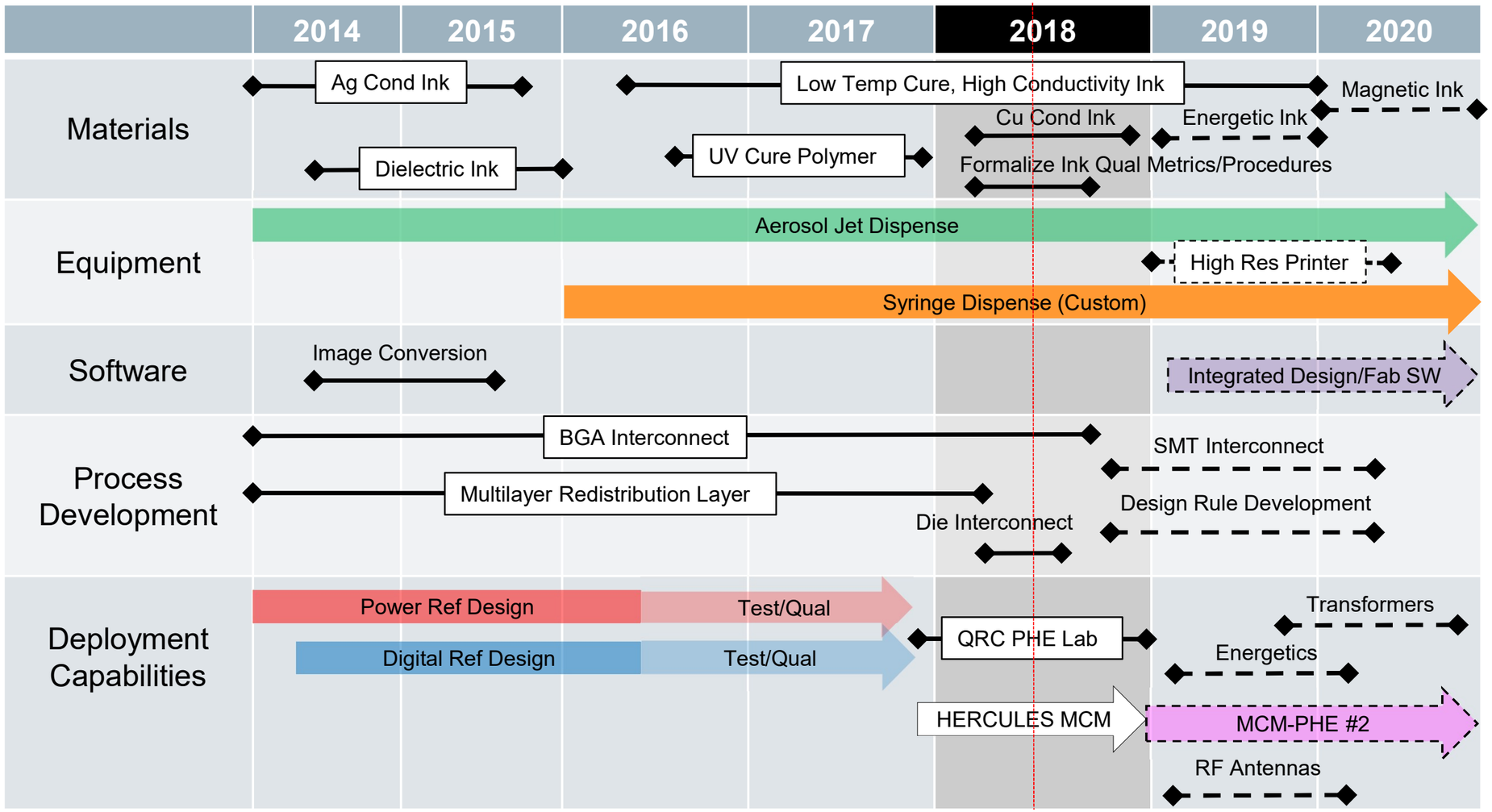
Future (Onsite)

- Optomec new release
  - 20µm min. feature size
  - 3-axis movement
- Microscope (June 2018), Profilometer & Stitching SW
  - Part inspection
- Alternate printing equipment
  - New materials: magnetic
  - Finer resolution: Down to 10µm min. feature size

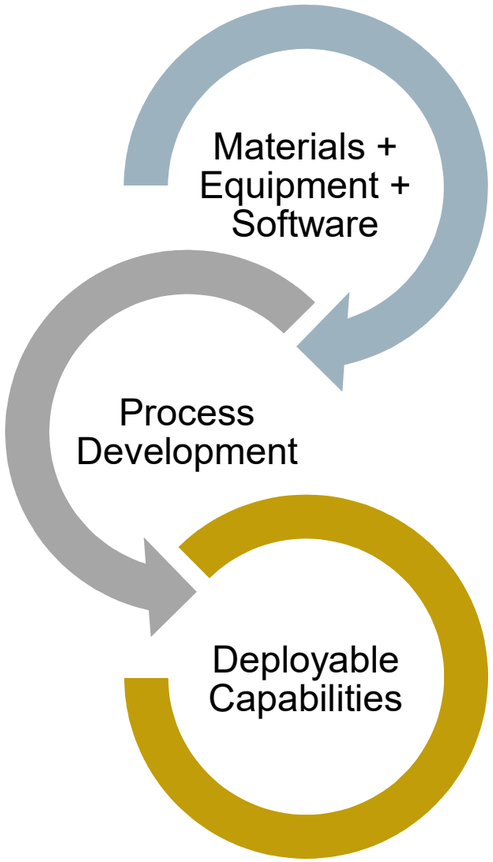
Current (Offsite)

- Optomec Aerosol Jet Printer
- Die/Flip Chip Bonder
- High Precision Pick and Place

TECHNOLOGY ROADMAP

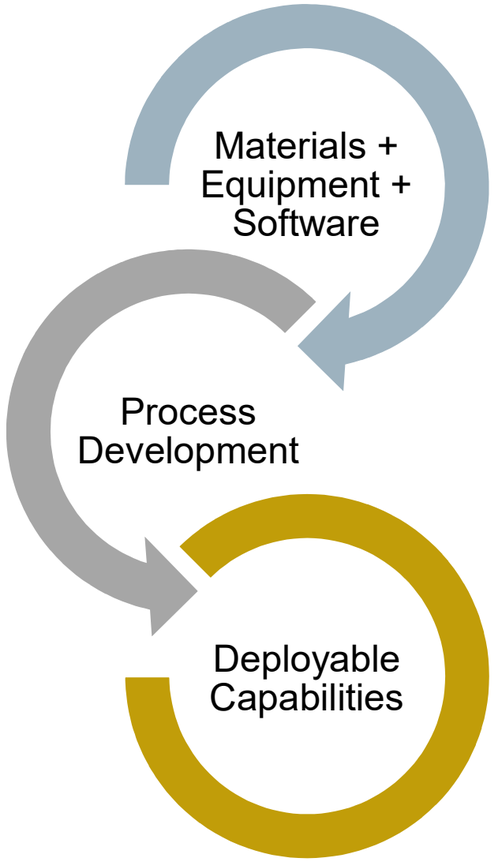


PHE: CAPABILITY DEVELOPMENT CYCLE



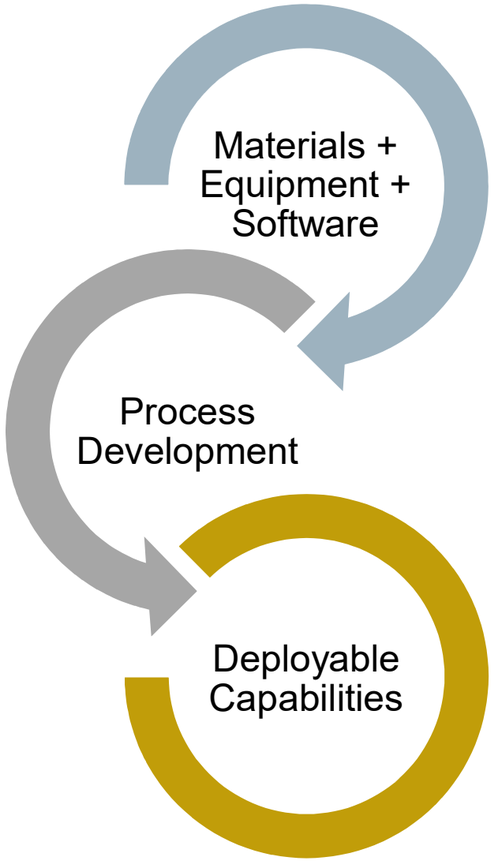
Thrust Area	Current Strategic Research Goal
Materials	***Identify cutting-edge PHE materials and provide independent characterization/qualification against key performance metrics*** • Material Properties ➢ Isotropic, CTE-matched, flexible, aerosol/syringe dispense, cure type (laser, UV, thermal) ➢ Reduce cure temp/time, trace size, price ➢ Increase electrical conductivity, thermal conductivity, yield strength • Qualification Metrics ➢ Performance – metrics listed above ➢ Cost/Availability ➢ Reliability/Life - Define environment, life target, Qualification & Accelerated Life testing (# of samples, test time)

PHE: CAPABILITY DEVELOPMENT CYCLE



Thrust Area	Current Strategic Research Goal
Equipment	***Identify and customize equipment for QRC PHE fabrication*** • Dispense method, # print heads • 3D vs. 2D • Curing method (laser, UV, thermal) • Pick and Place (Die, SMT components, etc…) • Inspection (X-ray, Optical Imaging) • Cost, Availability • Maturity of Technology/Vendor, Service/Support
Software	***Identify and customize software tools to support 3D PHE design (schematic, part libraries, layout) and manufacture*** • Component Placement & Routing (manual, auto) • Design Optimization, Job Estimator (Time, Material) • Material and Component Library • Compatibility: printers, traditional design tools (Altium, Solidworks)

PHE: CAPABILITY DEVELOPMENT CYCLE



Thrust Area	Current Strategic Research Goal
Process Development	***Develop and qualify PHE interconnects/structures to replace and integrate with traditional PCB solutions*** • Die placement, attachment, interconnect (wb, fc) • SMT placement, attachment, interconnect (BGA) • Hand-soldered interconnect • Design Rule Development
Deployable Capabilities	Integrate PHE research to demonstrate mission readiness as critical development milestones are reached. Leverage a phased approach, building from low to high complexity • Power reference circuit (low → high power) • Digital reference circuit (low → high speed) • RF reference circuit • 3D Antenna • Multi-Chip Modules • QRC PHE Lab

MILESTONES

- HERCULES-PHE (Optomec)
  - 2/1: Initial text and logo tests
  - 3/20: Printed Ag traces passed high speed traffic
  - 4/11: Ag plane / Dielectric / Ag trace microstrip completed
  - 4/24: Printed Ag plane / Dielectric / Ag trace stackup, passed high speed traffic
  - 4/11: Initial test of RDL fan out layer
  - 5/8: All layers of RDL individually printed & multi-layer print on single encapsulated die
- Haas Syringe System to Date
  - 3/28: Haas with grease pack spindle setup
  - 5/1: FP4451 Printed Dam
  - 5/4: Printed Ag traces, passed high speed traffic
  - 5/10: PCB Repair Demo

CYBER & SIGINT: BRIDGING SOLUTIONS

Successfully completed 300+ QRC (24 hour to 6 month) responses and delivered 1,000+ fielded systems since 2009

- Systems Engineering & Program Management
- Embedded Hardware, Firmware & Software Design
  - ASIC & Multi-Chip Module Design
  - Printed Circuit Board design, fab, assy & test (200+ unique designs per year)
  - FPGA design
  - Mechanical, electronics packaging design
  - RF/analog antenna design
  - Modeling & simulation (thermal, structural, RF)
  - Embedded software (ARM, MIPS, PowerPC, 8051)
  - Micro-power systems, power harvesting
  - LPI/LPD communication system development (GPS, GSM, wireless LAN, bluetooth, RFID, custom)
  - Reverse Engineering & Vulnerability Analysis
- Manufacturing – Low Volume, High Mix
  - Commercial Outsourcing
    - Hybrid – wafer foundry, chip-level assembly
    - PCB fabrication & assembly
    - Metal & plastic fabrication/finishing
  - In-house Niche Capabilities (Secure & Unclassified)
    - Electronics assembly & integration
    - Additive Mfg – Printed Hybrid Electronics
    - Machine Shop & Vehicle Bay
- Test Design & Execution
  - Functional Verification
  - Environmental – temp, humidity, shock/vibe, etc…
  - RF – anechoic chamber, indoor test range, roof access