Chiplet Technology & Heterogeneous Integration

A Leading Provider of Smart, Connected and Secure Embedded Solutions

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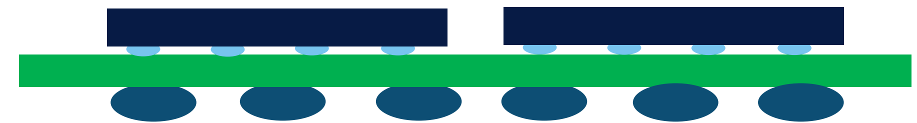
Agenda

- **Concepts of Heterogeneous Integration**
  - Definitions
  - Advantages/disadvantages
- **2.xD Ecosystem**
  - Physical interconnects
  - Interfaces
- **3D Ecosystem**
  - Stacking options
- **Technical Considerations**
- **Conclusions**

Definitions

- **Heterogeneous Integration**
  - Integration of separately manufactured components into a higher-level assembly to create a System-in-Package, SiP
- **Chiplets**
  - Die specifically designed and optimized for operation within a package in conjunction with other chiplets. Drives shorter distance electrically. A chiplet would not normally be able to be packaged separately.
- **2.x D (x=1,3,5 …) – HiR Definition**
  - Side by side active Silicon connected by high interconnect densities



- **3D**
  - Stacking of die/wafer on top of each other

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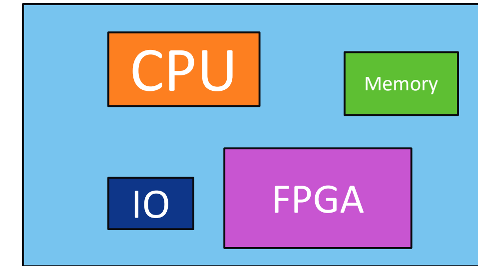
Why Heterogeneous Integration?



Advantages	Disadvantages
Smaller die → higher yield	Additional area for interface ~ 10% Additional area for TSVs ~2-5%
Flexible and optimized process selection • Use mature process for some chiplets • Shrink digital area/power for digital • Ability to re-use IP – reduce R&D cost	Packaging/assembly costs Additional design effort/complexity New methodologies

No one size fits all, need to evaluate the technology and cost of integration

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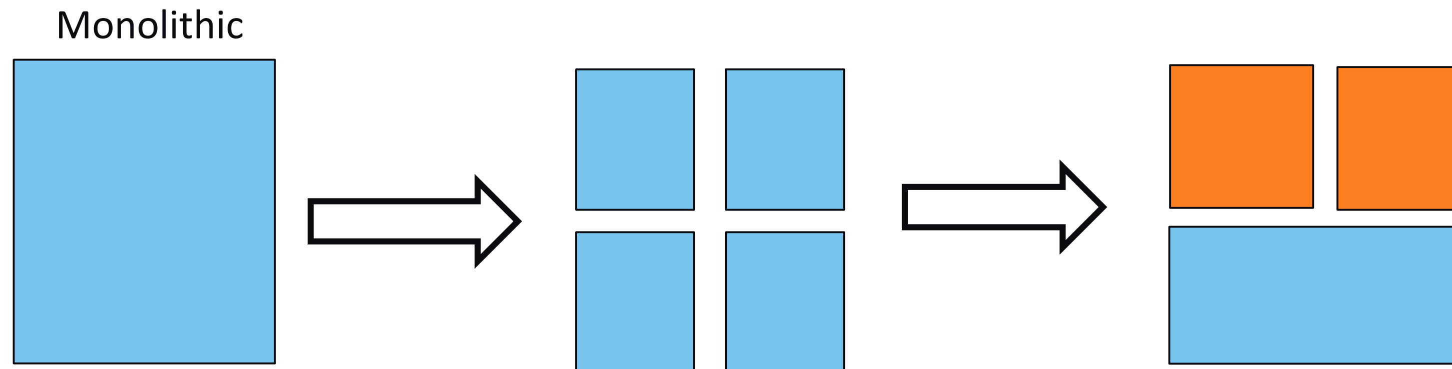
Example

- Large monolithic single die – 625 mm^2 (example)
- Split into multiple die (4) – 172 mm^2 each
- Overhead ~10% (for interconnect)
- Next, take advantage of digital scaling with process. Higher performance and lower area going to chiplet style integration



Introduction to Die-to-Die (D2D) Interfaces

How do chiplets talk to each other?

- **Similar to chip communication on a PCB**
- **Except:**
  - Chiplets are on a common substrate
  - Chiplets are much closer to each other
  - Need smaller drivers to meet this requirement (power, area)
  - The type of interface selected, and the type of packaging selected are closely tied

OCP Subgroup “Open Domain Specific Architecture”

Courtesy of ODSA

Use Case
Shrink board to package
Disaggregate a die

Transport Protocol
Custom
PCIe IP (off-the-shelf)
CXL IP (off-the-shelf)
CCIX IP (off-the-shelf)
AXI DiPort
PCIe Xn
CXL Xn
CCIX Xn
AXI DiPort
CHI
Tile Link
FIFO
Custom
New LDIF for transport protocol aggregation

Switching Protocol
Re-use existing IP for chiplets
Optional Mux
Cross chiplet switching

Link Layer Protocol
Protocol-integrated TXN/Link Layers
Open Link Layer
Open Link Layer
Intra-Chiplet Buses
Optional Mux

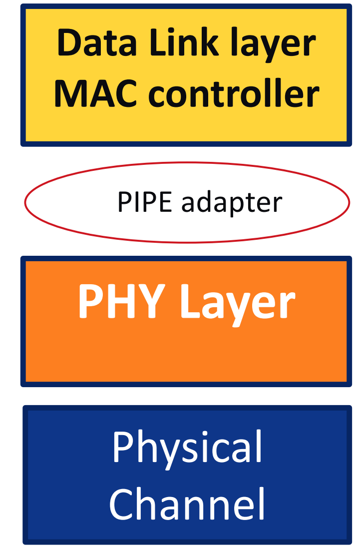
PHY Interface
PIPE Interface
LPIF Interface
LPIF Interface
LPIF Interface

PHY Adapter
PHY-specific PIPE Adapter
PHY-specific LPIF adapter
PHY-specific LPIF adapter
PHY-specific LPIF adapter

PHY Technology
PCIe
SerDes XSR, USR,..
BoW
Open HBI
AIB

Packaging Technology
Organic substrate
Interposers/bridges

Block/layer separator
Std. interface, ODSA-supported
New ODSA-defined
Standard Protocol or IP
New ODSA PHY, protocol
ODSA adapter for interface/protocol



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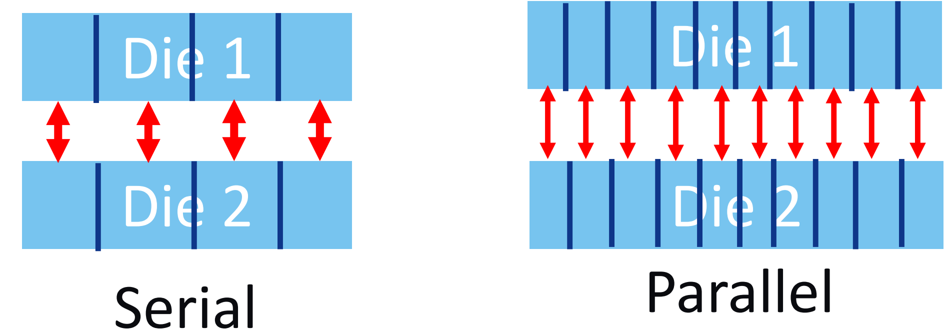
How Do You Select a D2D interface ?

- **Function/product specification**
  - Homogeneous/heterogeneous stacking
  - Which functional pieces are going to chiplet form
  - Align with a standard or choose an open/proprietary system
- **Priorities**
  - Power/performance/area
  - IO limited (beachfront)
  - Latency
  - Bandwidth
- **Packaging**
  - Cost



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High Level Representation of D2D Interface

Chiplet A

Chiplet B

Data and Clk

Chiplet A

Chiplet B

Link layer

Data

Ctrl

CLK

Tx slice

Tx/Rx slices

Data bus

Fwded CLK+/-

Rx slice

Tx/Rx slices

Data

Ctrl

CLK

Link layer

Organic/Interposer/RDL

Serial interface (XSR like)

- High data rate
- High latency
- Higher power
- Low-density routing
- Organic substrate

Parallel interface (AIB, BoW, Open HBI)

- Low data rate
- Low latency
- Lower power
- High-density routing
- Organic/interposer

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Physical Interface (D2D interface)

	AIB	Bunch of Wires (BoW)	Open HBI	XSR
Type	parallel	parallel	parallel	Serial
Clocking Scheme	Clk. forwarding	Clk. forwarding	Clk. forwarding	Clk. recovered
Signaling	DDR	DDR	DDR	Differential
Reach (trace length)	<10 mm	5 mm (unterminated) 50 mm (terminated)	4 mm	~50 mm term
Intended substrate	EMIB/interposer Organic	Organic substrate/interposer	Interposer	Organic substrate

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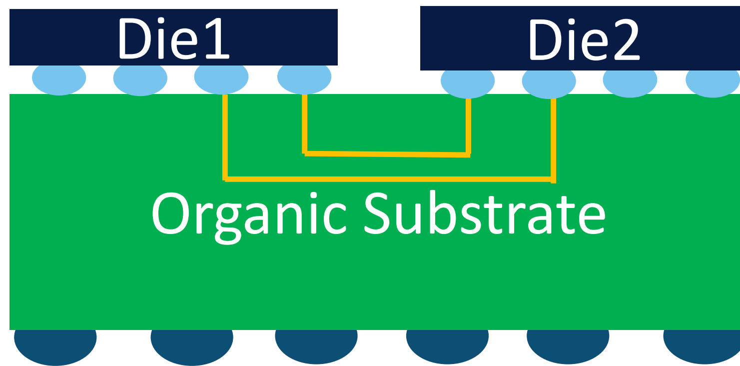
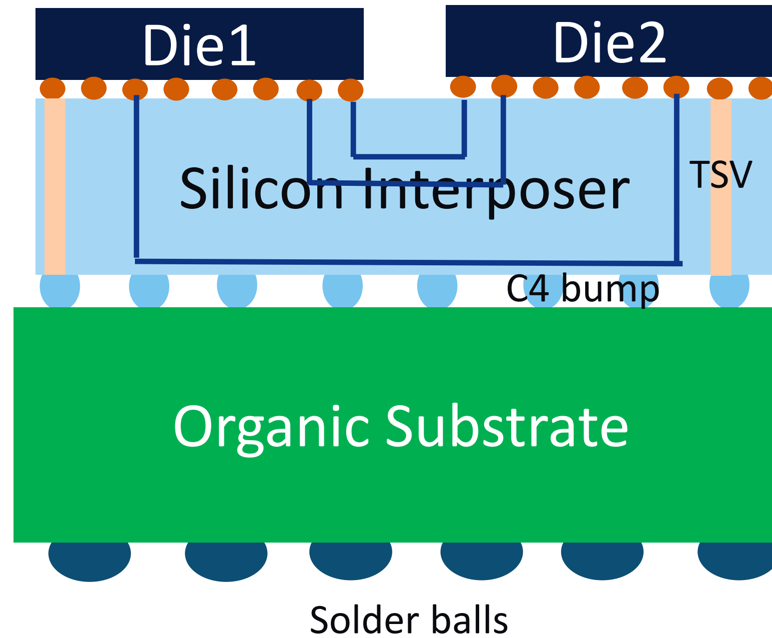
2.xD Integration

Organic Substrate



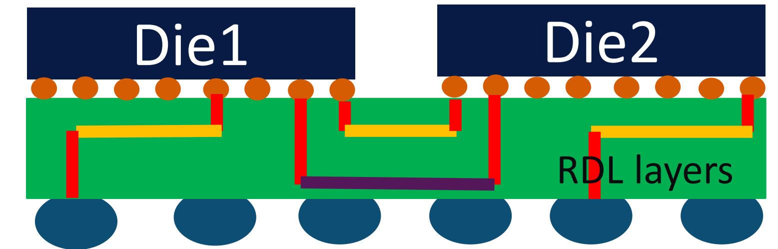
- Organic substrate
- Bump pitch: 150 um
- Low pin count
- L/S: 13 um/13 um
- >1 mm between die
- Cheaper packaging

Silicon Interposer



- Silicon interposer
- Microbump pitch : 40-55 um
- Higher pin count
- Submicron routing pitch
- <100 um between die
- Higher-cost packaging

RDL Interposer



- Up to 4 RDL layers
- Medium pin count
- 4 um pitch
- ~100 um between die
- Medium-cost packaging

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Current Volume Production in 2.xD

- **Silicon interposer**
  - FPGA slices connected using high density interconnects on a silicon interposer

  - High-Bandwidth Memory (HBM) connected to ASIC/FPGA/CPU on silicon interposer

- **ASE – HBM integration**
  - Interposer – 4 HBM2e
  - AI training

Courtesy: ASE

  - FoCoS- ChipLast
    - 3500 RDL traces (4 layers)

Courtesy: ASE

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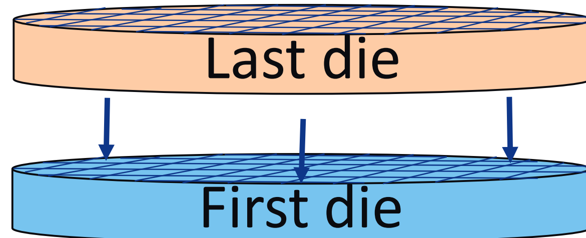
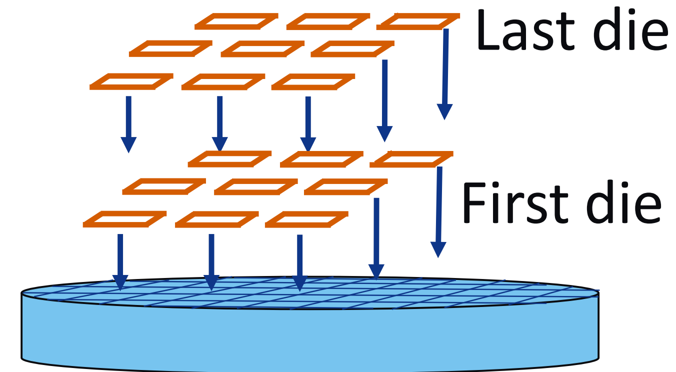
3D Stacking

Wafer on Wafer



- Lower yield
- High throughput
- Same size die

Die on Wafer/Chip on Wafer



- Pick and place of KGD
- Different sized die

Two ways to connect the die:

- Microbump – Cu pillar bump with 55 um pitch
- Hybrid bond – Cu-Cu and oxide to oxide bond

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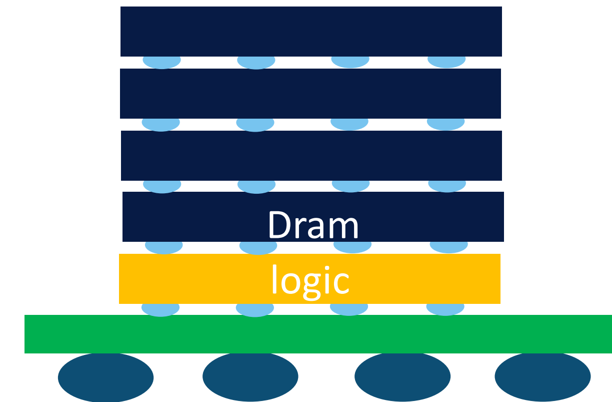
Current High Volume in 3D Stacking

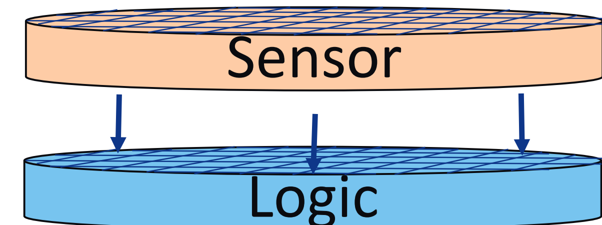
High-Bandwidth Memory

- JEDEC standard
- 3rd generation of HBM - 16 DRAM stacked on logic
- Face to Back stacking using Microbumps and TSVs



CMOS Image Sensors

- Sensor stacked on logic
- Face-to-Face stacking -WoW



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Technical Considerations

- **Disaggregating the SoC**
  - Logic partitioning to chiplets
  - System level simulations to model the system of chiplets
  - Design for test
  - ESD requirements
  - Thermal considerations especially if 3D stacking
  - Signal integrity considerations for high-speed signals through TSVs
  - Mechanical considerations for die warpage

Conclusions

- There is no one size fits all
- Evolving technology, expect to see cost reduction for assembly with time
- ODSA working to develop standards for chiplet integration
- Multiple D2D interconnect standards exist. Selection of the right interface depends on power/performance/area requirements, cost and other considerations

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Thank You