

Heterogenous Integration Packaging Technologies and Their Off-chip Interconnects in Perspective of High-reliability Space Applications

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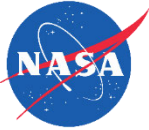
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NASA Electronic Parts and Packaging Program (NEPP)

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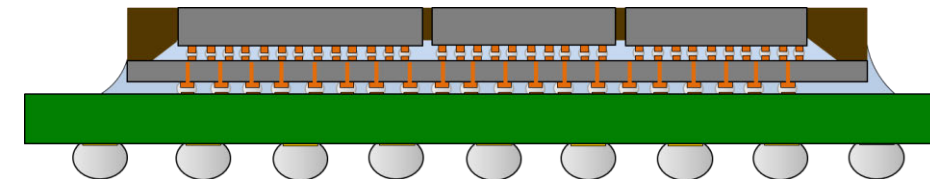
Purpose of The Presentation

- Bring up questions that can facilitate productive discussion in the community
 - For implementing this type of advanced packaging for space.
 - Assuming that some of the packaging or relevant back-end processes won't be done at major companies.
 - In the context of:
 - Developing/reviewing conditions and PIDTP, industry requirement
 - Screening conditions, Quality, Reliability
 - Starting conversation with a potential packaging supplier that does not have commercialized high-volume products
 - Mainly in perspective of component user, not manufacturer.
- Mainly focus on off-chip interconnect
 - which is one of many aspects of HI packaging.
 - Microbump
 - Hybrid bonding
 - Introduce manufacturing process and materials. Discuss related quality and reliability challenges.

***Note :** Cost and yield will not be discussed.

The presenters don't have a good understanding on how important cost related to yield is for high-rel.

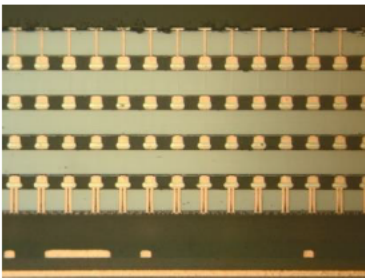
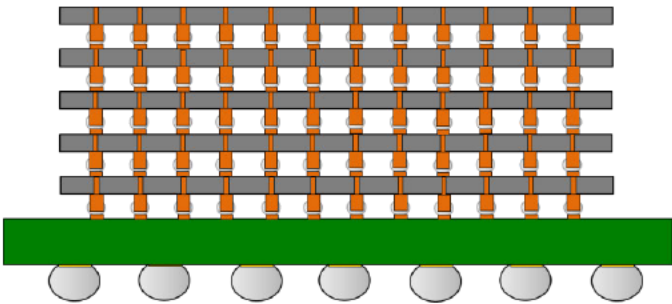
- KGDs are being integrated. And if 1 die is lost, all dies are lost.
- How important is the cost increase by yield loss? How do contracts work if packaging company loses dies?
- Major foundries or semiconductor companies have very high yield. Smaller companies may not.



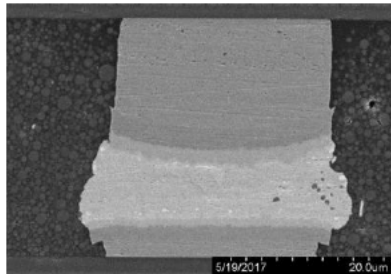
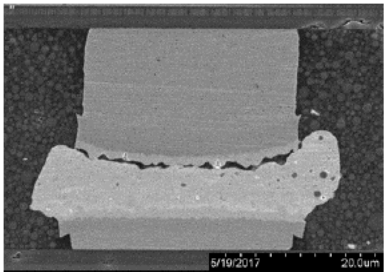


3D Stacked Die

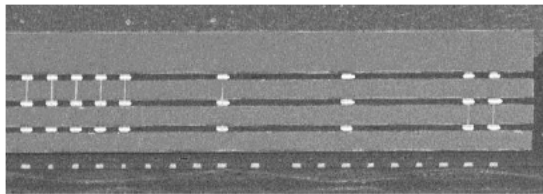
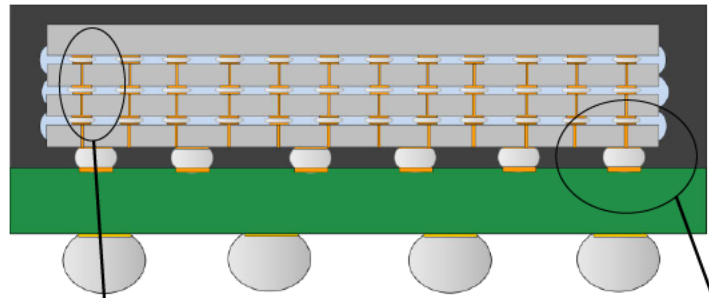
NEPP



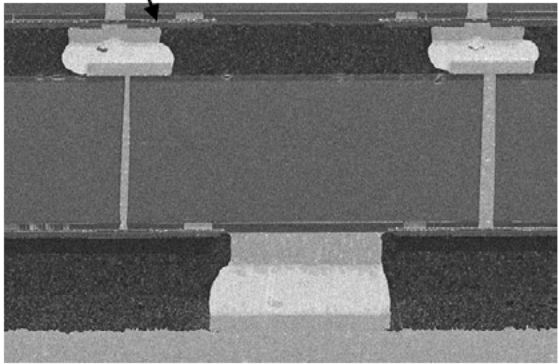
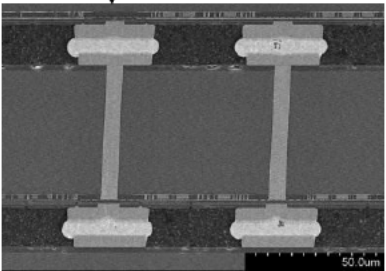
Micron HMC



Sacrificial bump



Samsung 3D DDR4

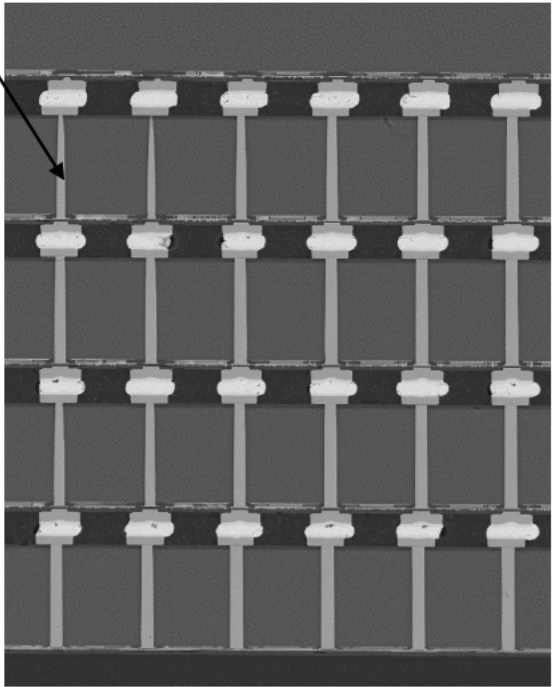
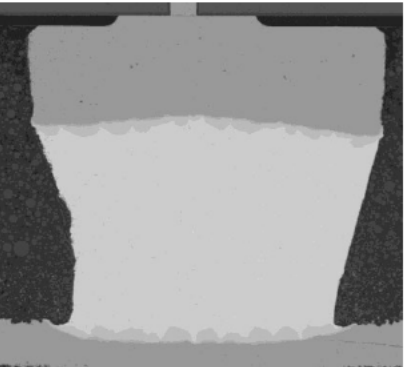
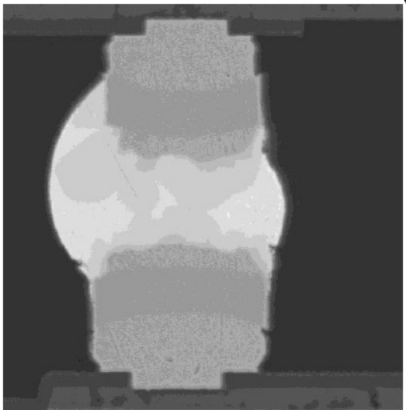
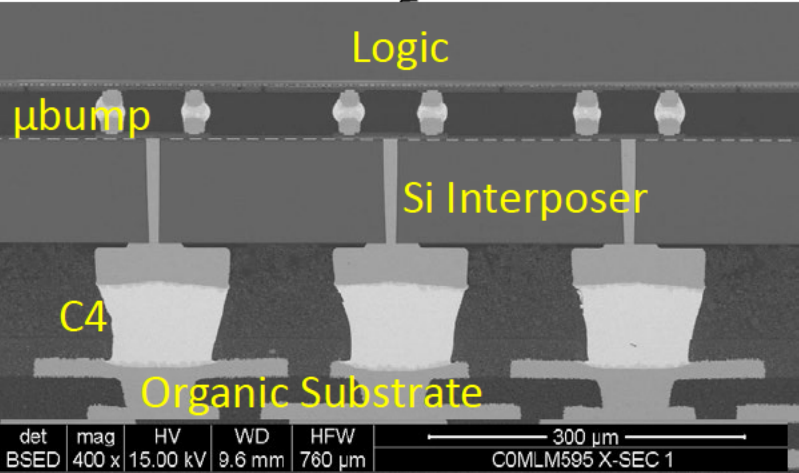
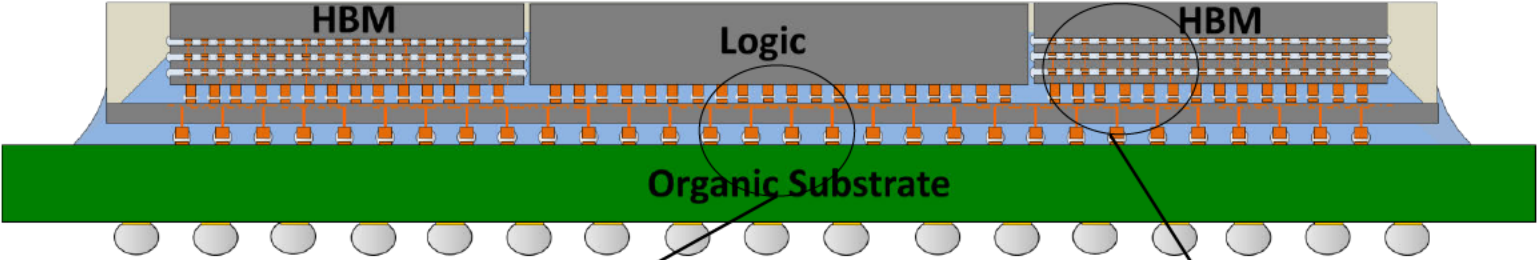




Si Interposer

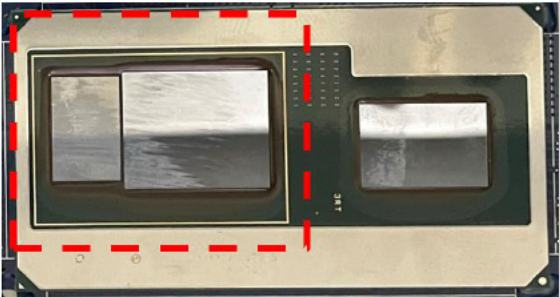


Nvidia GV100
TSMC CoWoS



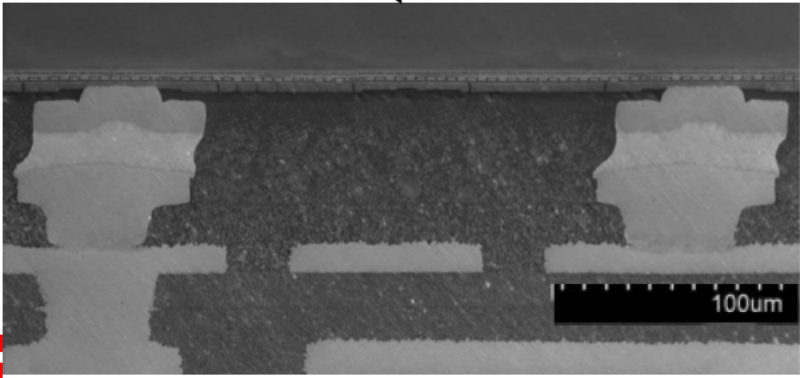
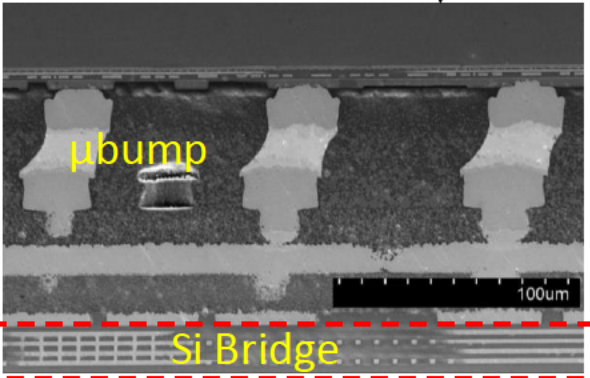
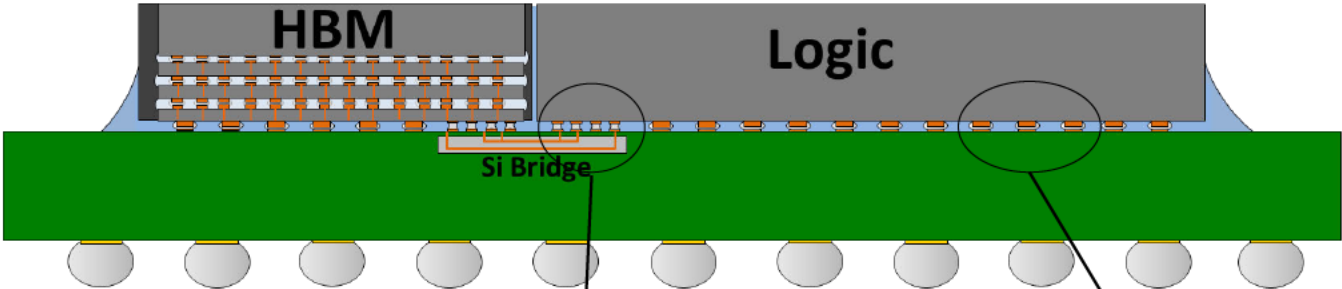
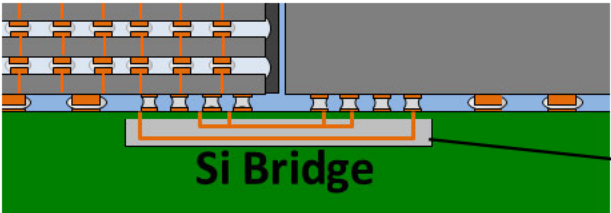


Si Bridge Embedded in Organic Substrate



60mm

i7-8705G
Intel EMIB



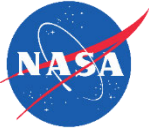
*Stratix 10 has 55μm pitch at EMIB jpl.nasa.gov



Heterogenous Integration (HI) Packaging

- **Term ‘HI’ will be used for convenience** in the current presentation for these types of advanced packaging.
 - Terminology challenges when describing these types of advanced packaging
 - Many terminologies were created in attempts to categorize architectures.
 - HI, 2.5D, 3D, 2.1D, 2.3D, 2DS....
 - Large variety of packaging architectures.
 - Virtually each trade name is its own architecture.
 - *Small number of them can be grouped together in a taxonomy.*
 - **Note : ‘HI’ does not fully represent the technology.**
 - ex) Not HI : Memory chip stacking. Die split/partition.

CoWoS-S	CoWoS-R	CoWoS-L	InFO_PoP	InFO_oS	SoIC-CoW	SoIC-WoW	EMIB	Foveros	I-CubeS	I-CubeE	H-Cube	X-Cube	FOCoS-CF	FOCoS-CL	FOCoS-Bridge	SWIFT
TSMC							Intel		Samsung				ASE			Amkor



Examples of applications

- Heterogenous integration of disparate semiconductor technologies.
 - Ex) IP blocks or functions difficult to build on the same chip, such as logic and DRAM.
- Die yield enhancement by integrating spilt pieces of a large die.
- Integration of different SoC cores for faster development for SoC. Avoid redesigning entire chip for advanced node.
- PPAC (Power, Performance, Area, and cost), PPACC (Power, Performance, Area, Cost, Cycle time to market)
 - SWaP, SWaP-C in Mil/Aero
 - Cost is often the main driver in commercial products
 - ex) No incentive if cost for : $\$(\text{Die split for yield under QML process}) > \$(\text{Building monolithic die})$



Can Be Reliable, If Built Right

- HI packages built using **well-established process** are **capable of passing mil/aero qual conditions**.
 - **Literatures** on μ bump and hybrid bonded interconnect.
 - **Qual test reports** on high-end commercial product.
 - Qual tests are not reliability characterization tests. (Qualification $\neq$ Reliability $\neq$ Robustness)
 - Based on JESD47. 38535 tests are structured differently so not apples to apples.
 - Certain failure modes can't be covered by either
 - Samples were tested far beyond qual conditions in some literatures.
 - Preconditioning prior to : TC, THB, AC, HAST, uHAST. 38535 also asks for this (JESD22-A113).
 - For COTS qual: Simulating relevant screening condition before step 2 should be considered for COTS qual. Step 2 is to simulate TC during shipping and our screening condition is far severe.
 - Many packages from major companies are considered as mature technologies by their customers.

JESD22-A113 Preconditioning prior to TC, THB, AC, HAST, uHAST			
Step	Test type	Condition	
1	Initial electrical/visual		
2	Temperature cycling	-40/+60C 5 cyc	
3	Bake	125°C, 24 hr	
4	Moisture soak	MSL3: 192hr 30°C/60%RH MSL4: 96hr 30°C/60%RH	Within 2hr after previous step
5	Reflow	3 reflows	Between 15min to 4hr after previous step
6	Flux immersion	10 sec minimum	Not required for BGA/CGA/LGA
7	Clean & dry		
8	Final electrical		



JESD47	
Temperature Cycling (TC)	
Temperature Humidity Bias (THB)	
Autoclave (AC)	
HAST	
Unbiased HAST (uHAST)	
High Temperature Storage (HTSL)	
Solder Ball Shear, Bond Pull Strength, Bond Shear, Solderability, Tin Whisker Acceptance	

From a commercial product reliability report			
TC	-55/+125°C -40/+125°C	1000 cyc	25x3
HTS	150C	1000 hr	25x3
THB or HAST	85°C, 85% RH, VDD 130°C, 85% RH, VDD 110°C, 85% RH, VDD	1000 hr 96 hr 264 hr	25x3
uHAST or AC	121°C, 100% RH 85°C, 85% RH 130°C, 85% RH 110°C, 85% RH	96 hr 1000 hr 96 hr 264 hr	25x3



Built Right

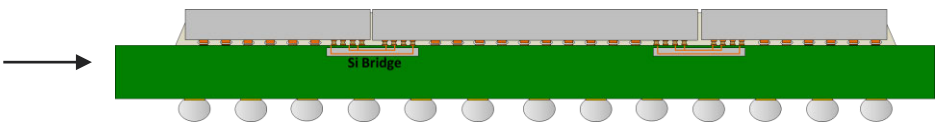
- Assembly process and materials are sophisticated and requires expensive infrastructure.
- Increasing capability gap between large and small companies
 - Packaging business started to resemble chip business.
 - Potential **quality and yield implications** related to company’s manufacturing capability.
- Ideally when choosing supplier, people who did full development and qualification should be leveraged.
 - Need to be cautious when using not well-established process or material set.

CoWoS-S	CoWoS-R	CoWoS-L	InFO_PoP	InFO_oS	SoIC-CoW	SoIC-WoW	EMIB	Foveros	I-CubeS	I-CubeE	H-Cube	X-Cube	FOCoS-CF	FOCoS-CL	FOCoS-Bridge	SWIFT
TSMC							Intel		Samsung				ASE			Amkor



HI Architectures

- It's about what it can do, not how it looks like.
 - Virtually each trade name is its own architecture.
 - Small number of them can be grouped together. (Some of them in a taxonomy.)
ex) CoWoS-S and I-CubeS
 - Chiplet-related commercial specs (ex: UCle, AIB, BoW) allow flexible architecture or do not specifically define architecture.
 - TSV is not what defines these technologies.
 - TSV is not necessary when integrating dies laterally.
 - Lateral integration
 - High-density is the key
 - Interposer, Si bridge, Fan-out, High density substrate, etc
 - Feature size beyond organic substrate
 - Vertical integration
 - TSV
- A Mil-PRF-ATM spec is under development
 - The current draft requires existence of TSV or TGV to be applicable to the spec.
 - Formulating spec with traditional methodology is difficult.



CoWoS-S	CoWoS-R	CoWoS-L	InFO_PoP	InFO_oS	SoIC-CoW	SoIC-WoW	EMIB	Foveros	I-CubeS	I-CubeE	H-Cube	X-Cube	FOCoS-CF	FOCoS-CL	FOCoS-Bridge	SWIFT
TSMC							Intel		Samsung				ASE		Amkor	



38535-like Approach is Becoming Challenging

- Traditional approach of formulating spec/requirement based on packaging architecture and feature is difficult.
- Spec has to be agnostic or highly customized to (ideally):
 - Architecture and feature
 - Diverse architectures.
 - Manufacturing process
 - Same/Similar architecture can be built in different ways.

ex) ‘How can we qualify 2.5D?’, should be worded as, ‘How can we qualify 2.5D built by ACME?’
- Nimble (ideally)
 - 1) Handle frequent process and material changes in a same product.
 - A QML part can experience many process and material changes during its product life cycle.
 - 2) Keep up with speed of change in what’s in the market.
 - The table looked very different last year. And that one looked very different 2 years before.

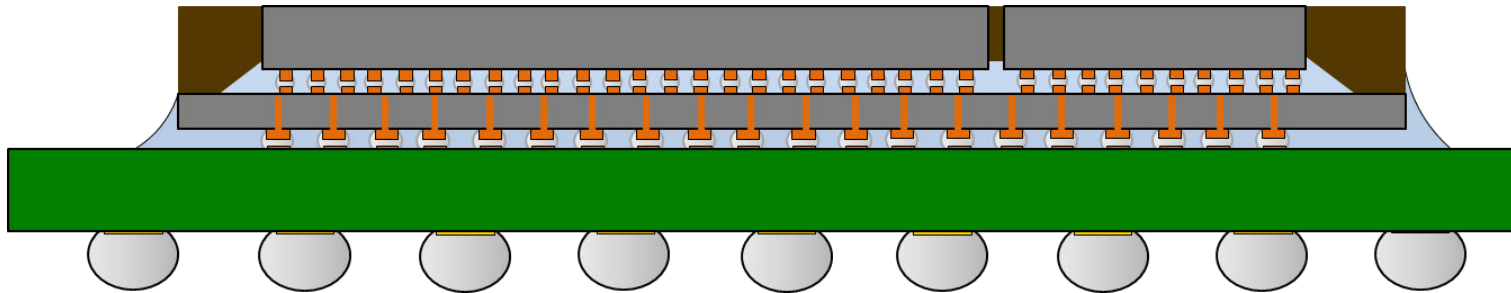
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Challenges in 38535-like Approach

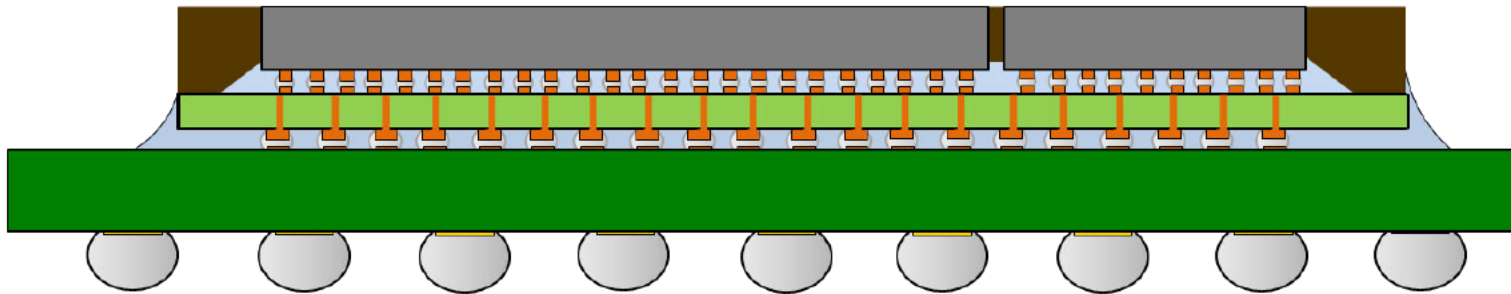
Some examples from actual architectures

- How should we define things like : Flow, Assembly Process Technology Testing, Technology Characterization Testing, Group tests, etc?
- Applicable to MIL-PRF-ATM draft (requires TSV or TGV)?

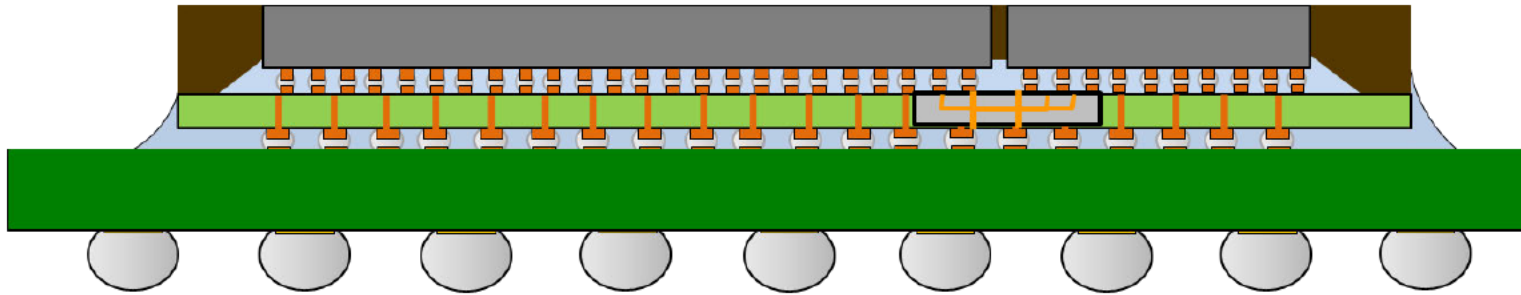
1st example:



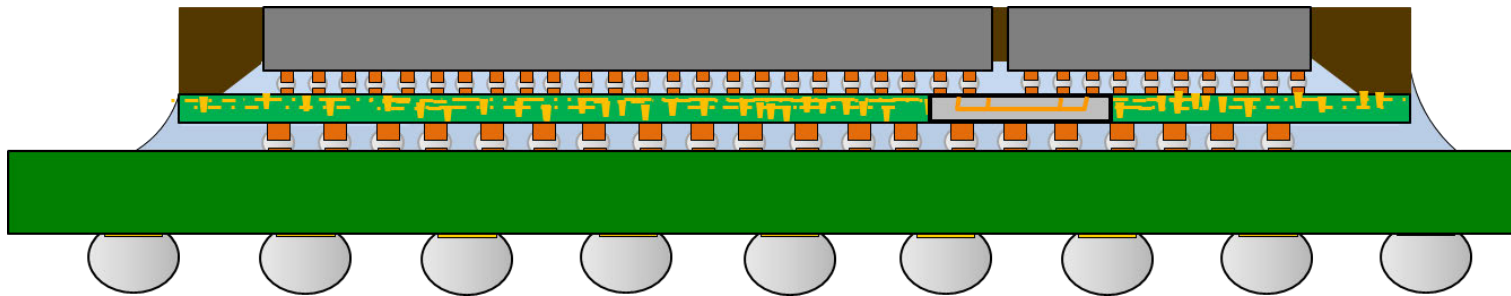
This package has Si interposer.



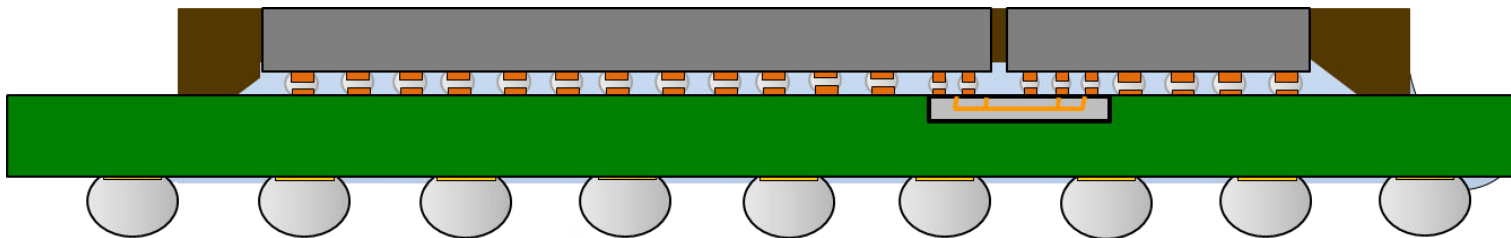
This one also has interposer, but it's not Si.
It's an organic interposer.



This one also has an organic interposer.
 The interposer has a Si bridge embedded.
 And the Si bridge has TSV.



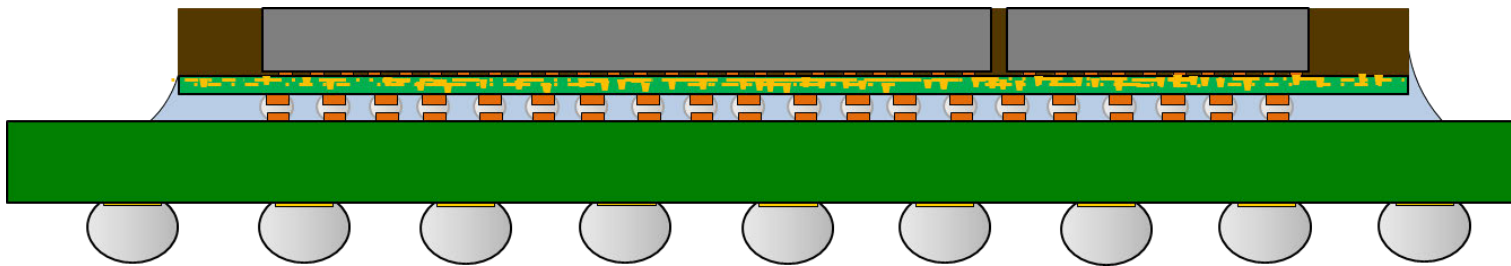
This one also has Si bridge embedded in interposer.
But the bridge has no TSV, unlike the one before.
The interposer is actually fan-out.



This one also has Si bridge.

Just like the one before, the bridge has no TSV.

Unlike all others, there is no interposer. Bridge is embedded in substrate.

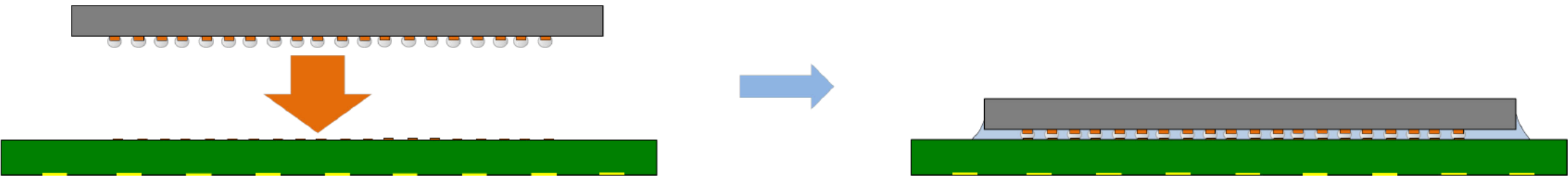


This one also has fan-out. No Si bridge.
Unlike all others, there is no μ bump.



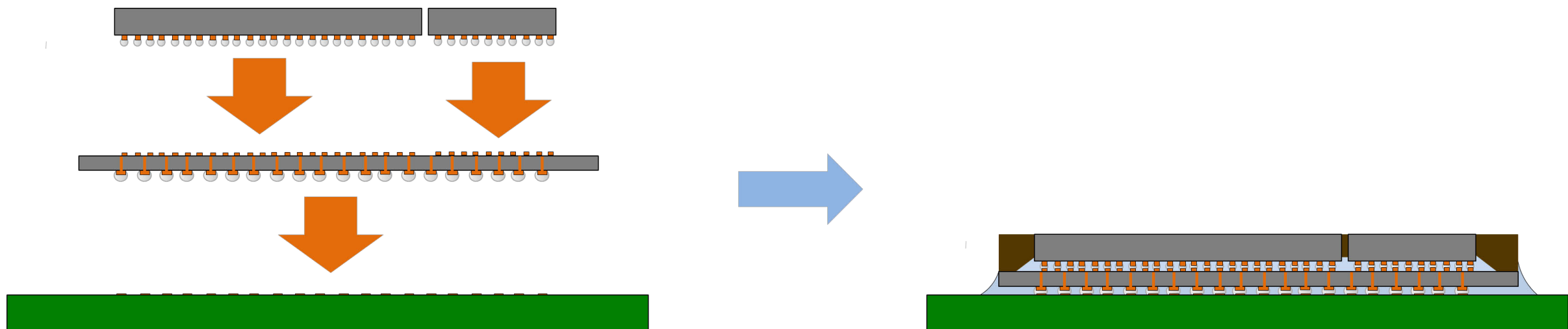
- **Agnostic or highly customized for architecture or feature?**
 - May/may not have TSV.
 - May/may not have interposer.
 - May/may not have bridge.
 - May/may not have μ bump.
 - Interposer can be made of any material.

- Agnostic or highly customized to manufacturing process?



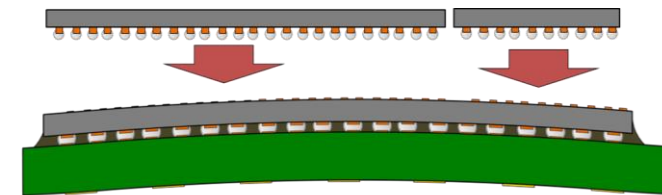
Flip Chip : Attach die to substrate

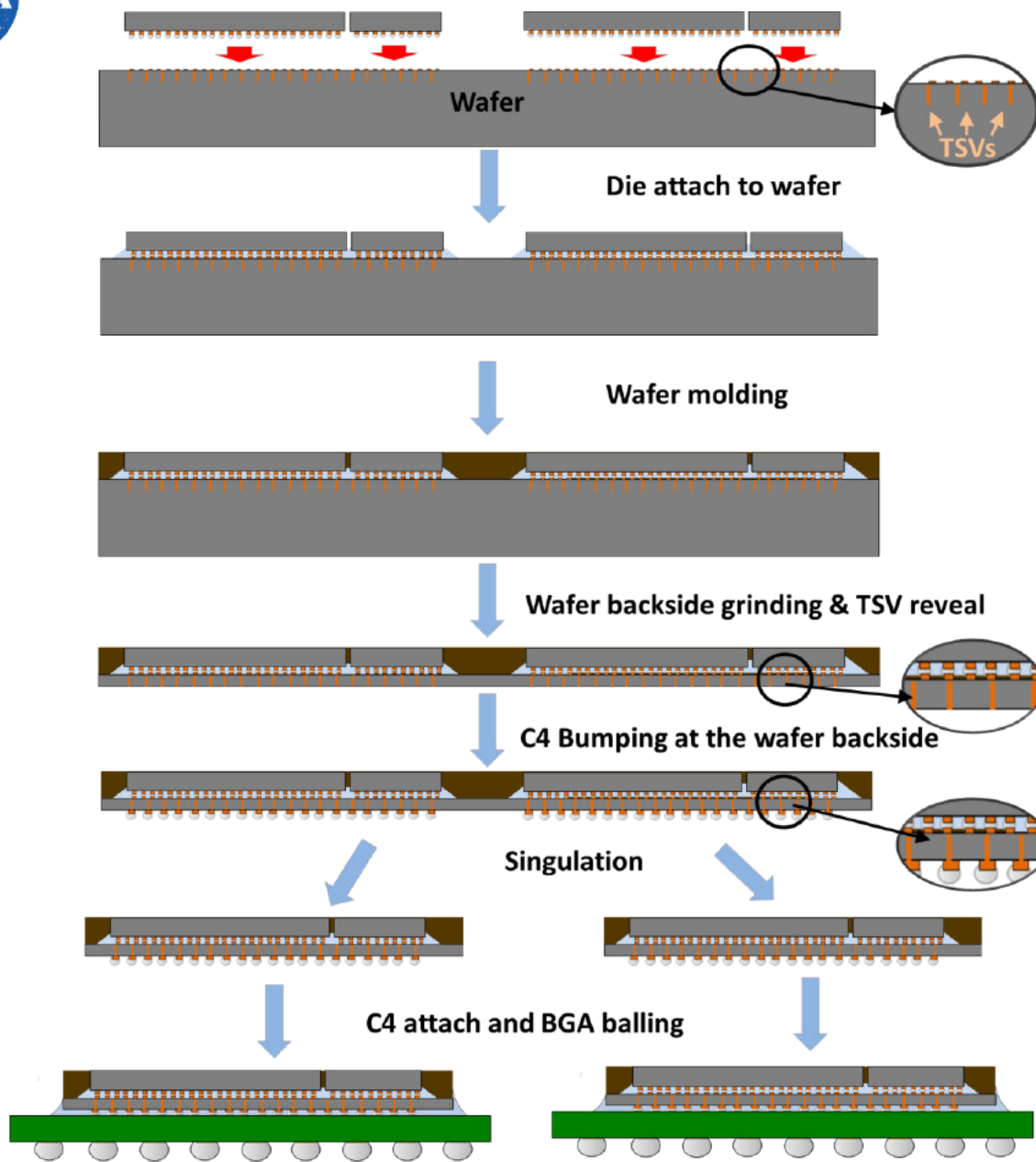
Temperature Cycling
HAST 3/
Thermal Shock
Shock and Vibe
Bump Shear Test
Die Attach Bond Strength
Die Shear Strength
Die Pull Off
Destructive Part Analysis(DPA) bump sample post-thermal cycle and thermal shock test



Si stacking : Attach lower die to substrate, then attach upper die?

.. If yield and throughput is of little importance.



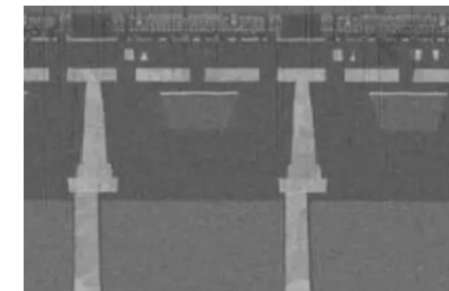
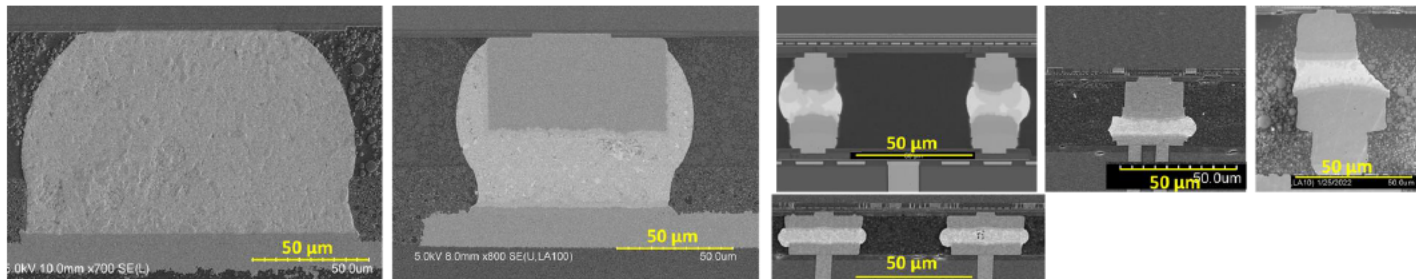
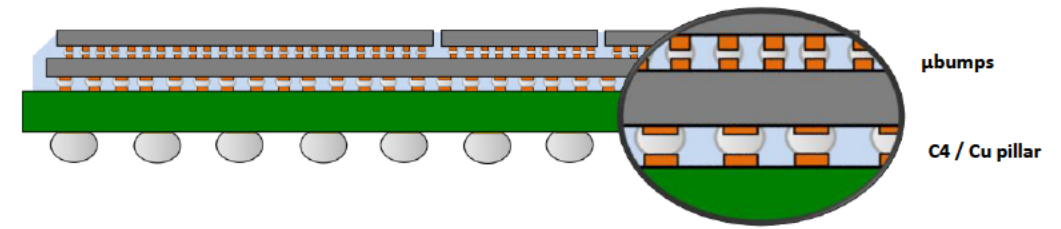
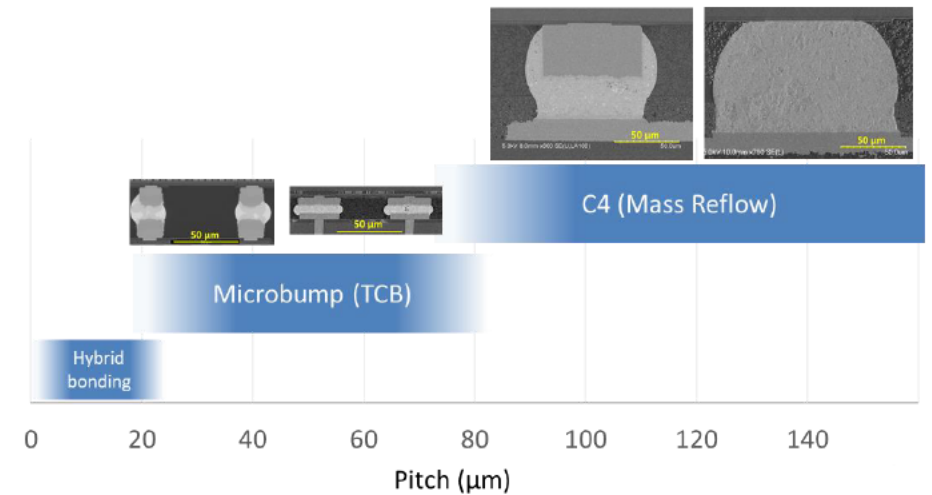


- CoWoS-S process is shown as an example
 - D2W → Wafer backside thinning & TSV reveal → Wafer C4 bumping
 - Packaging involves certain processes that are done at the back-end in traditional packages.
 - Some other architectures are also built by similar process flow. (Wafer can be active device.)
 - Other companies previously proposed different process flow.
- Fan-outs have very different process.
- ‘Chip-first’, ‘Chip-last’
- “Agnostic or highly customized to manufacturing process”



Off-Chip Interconnects : μ bump and Hybrid Bonding

- C4
 - Mass reflow
- μ bump
 - Down to $\sim 20\mu\text{m}$ pitch.
 - Thermocompression bonding (TCB)
- Underfill
 - Both for C4 and μ bump for TC reliability.
- Hybrid bonding
 - Both dielectric and copper are bonded.
 - Wafer-to-Wafer or Die-to-Wafer (Not for substrate).
 - SoA pitch range is different between W2W and D2W.
 - W2W: $2.5\sim 8\mu\text{m}$, $1\mu\text{m}$ demonstrated
 - D2W: $\sim 9\mu\text{m}$ in product.
 - Can be improved by sacrificing throughput.



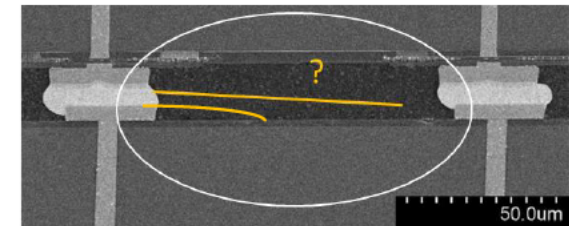
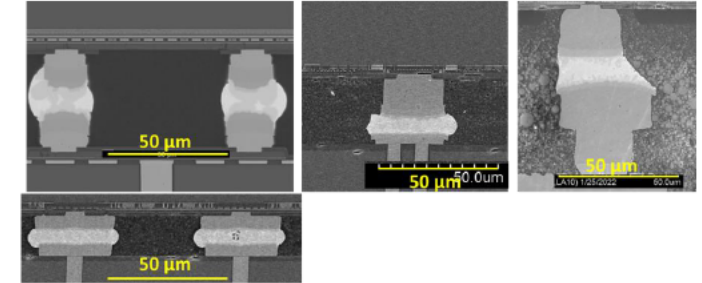
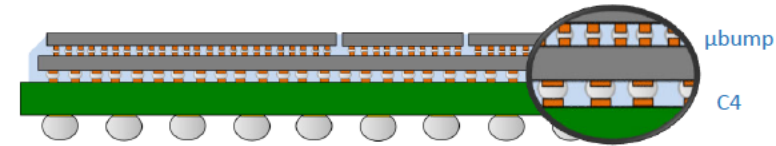
Hybrid bonded memory on CPU

<https://www.amd.com/en/technologies/3d-v-cache>

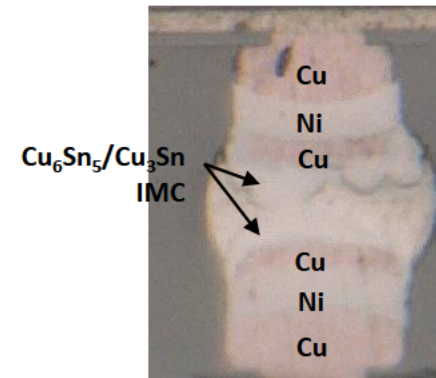
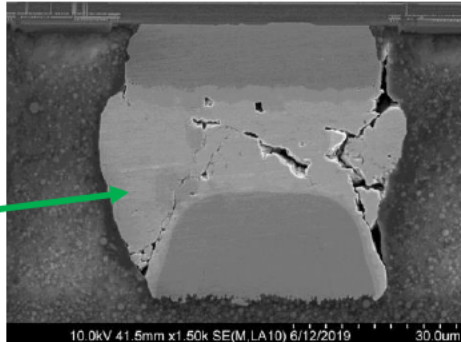
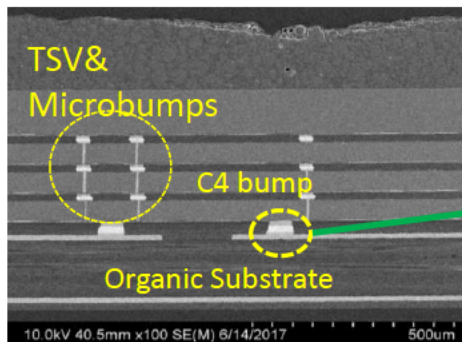


μbump and Pb-free

- We are already forced to use Pb-free bumps.
 - V5 had to switch C4 to Pb-free in CY2022 Q3.
- C4 : Supply chain availability (300mm wafer bumping)
- μbump : Can't reinvent process and materials, since the technology has evolved around Pb-free.
- SnAg is the most frequently used material, both for C4 and μbump.
 - 1.8 ~ 2.5 or 2.8 wt% Ag. (3.5wt% is eutectic.)
 - Less-than-eutectic for both production and reliability reasons.
 - Production : Liquidus temperature control (wafer bumping & reflow)
 - Reliability : Ag₃Sn control and other reliabilities.
- **μbump has diverse configuration.**
- **μbump wafer bumping needs better engineering than C4.**
 - μbump quality is a part of KGD criteria.
 - Bump coplanarity, bump surface roughness, Cu column undercutting, plating uniformity, etc
- **For high-rel : If μbump underfill has void, Sn whisker questions can be asked.**
 - It is not certain if there can be a μbump configuration with enough risk.
 - **Underfill void bridging more than 2 μbumps as the internal visual reject criteria?**
 - Is this feasible for stack-up and resolution? Could this be too much?
 - CSAM is done for flip chip internal visual as a screening.
 - BGA : Low risk based on the current understanding of whisker metallurgy.
 - Unless exposed to corrosive environment or doped with REE. Also can be attached with Sn63.
 - C4 : Likely low risk, as BGA.



- μbump has diverse configuration.
- **Many parameter choices in μbump configuration. How they are combined affects the reliability.**
 - Cu pillar stack up, solder composition, Cu pillar and solder dimension, metallization at upper & lower die, etc.
 - Electromigration (degradation mechanism and MTTF) and Interfacial reaction (diffusion, IMC growth, Kirkendall voiding)
 - Thermal cycling reliability
 - Can be more reliable than bigger C4 at the bottom die.
- The μbump metallurgy is not the scope of this presentation
 - EM alone can be a long presentation.
 - Metallurgical principles in C4 are carried over to μbump, with different boundary condition (much smaller solder volume).
 - Entire solder can transform into IMC.
 - Shrinkage voids (not Kirkendall voids) that does not form in C4 can form, as solder is transformed into IMC.
 - Sn grain orientation starts to play greater role in individual μbump than C4.
- **μbump configuration selection: if overall packaging is developed with a major company, the supplier's knowledge should be leveraged.**
 - Enough knowledge is accumulated in the field, although it's a vast subject.
 - Adequate structure need to be used for application. ex) current density, thermal / mechanical characteristics



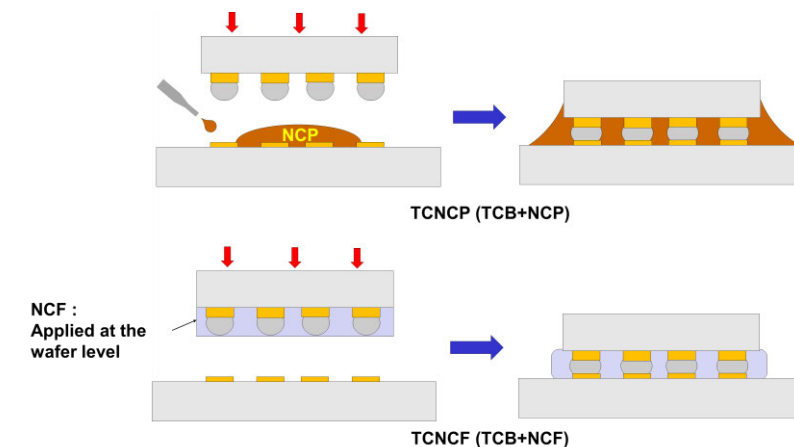
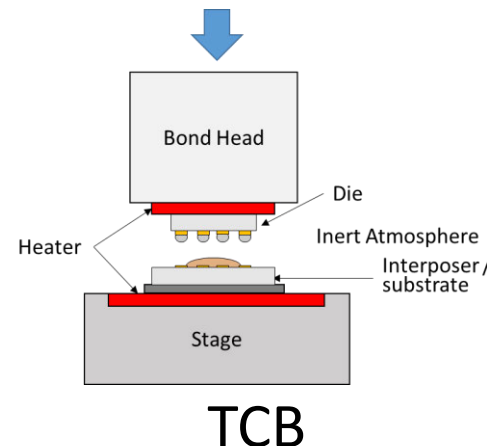
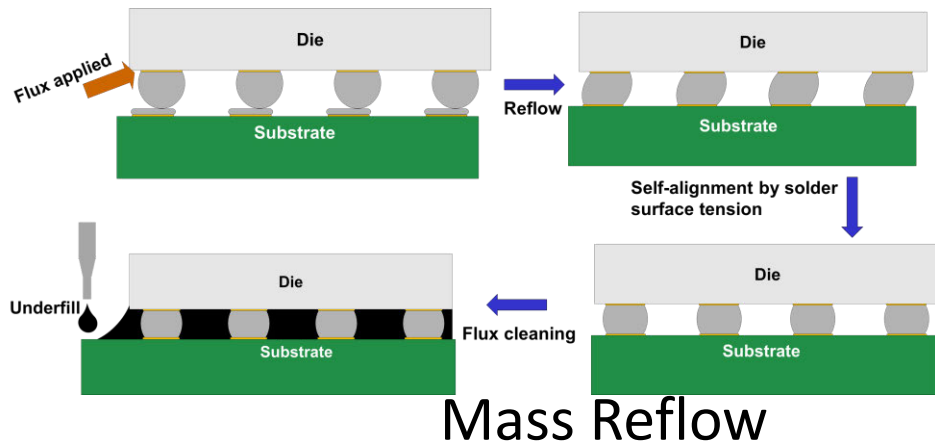
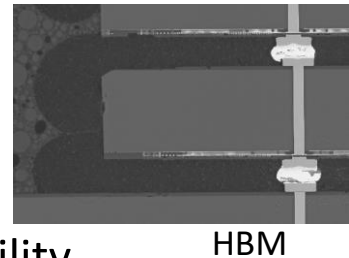
μbump Assembly Process

- Thermocompression bonding (TCB)

- Mass reflow (MR) for C4 attach cannot be used.
 - Smaller pitch : Need more precise alignment. No self-alignment by solder surface tension.
 - Thinned dies.
- More complex process than MR: Far greater number of process parameters than MR.
 - Stage temperature, bond head time-temperature profile (ramp, contact, peak, release, cool), contact & bond force, bond head displacement, dwell time, etc.
 - Process done within a few seconds.

- Underfill choices

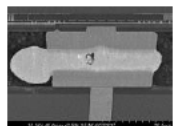
- CUF (Capillary underfill) : Capillary flow after TCB and flux cleaning.
- NCF (Non-conductive film) : Most HBM's use this. Applied at the wafer level. Has fluxing capability.
- NCP (Non-conductive paste) : Pre-applied on the die attach surface. Has fluxing capability.





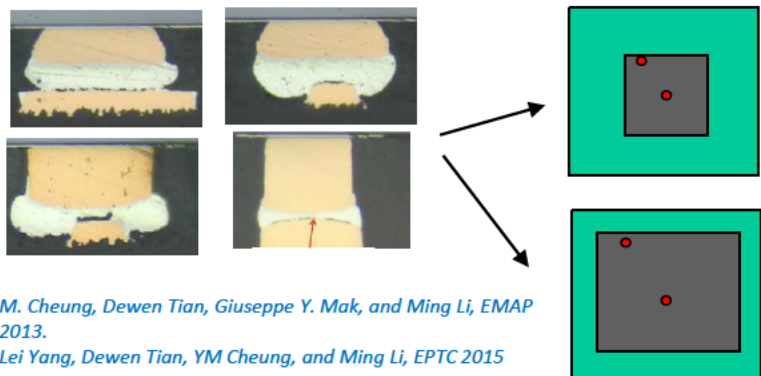
μbump Underfill and Reliability

- CUF :
 - Major companies frequently use CUF for μbump.
 - Smaller companies may have challenge in controlling void, as bump pitch reduces and die size increase.
 - Cleaning flux between μbumps & flowing CUF : Needs better engineering capability and know-how.
 - **Manufacturer needs to know how to control void for: TC reliability & whisker questions.**
- NCP and NCF
 - Pre-applied underfill with fluxing capability. Cures within seconds in real time during TCB.
 - **Fluxing capability : need to check for outgassing**
 - Easier to prevent large voids than CUF, but has drawbacks (NCP : fillet control, NCF : Die shelf life).
 - **Process defects within solder bump cannot be detected by NDT.**
 - **The defects can pass 38535 minimum TC screening (15cyc, cond B) but cause early failure.**
 - Failure can spread out, since it will depend on package design and defective bump's location. Can be benign at certain stack-up.
 - When talking to supplier:
 - **Some prototyping TCB machines are not compatible with COTS NCP/NCF**, which requires high ramp rate.
 - For attaching dies very close to each other with NCP, manufacture will need to know how to control the fillet.
- **Screening cond. & Complexity of defining lot :** Above issues can be examples.
 - Lot has to be defined in detail based on defect creation mechanism at given process and material. Screening based on failure rate from multiple lots.

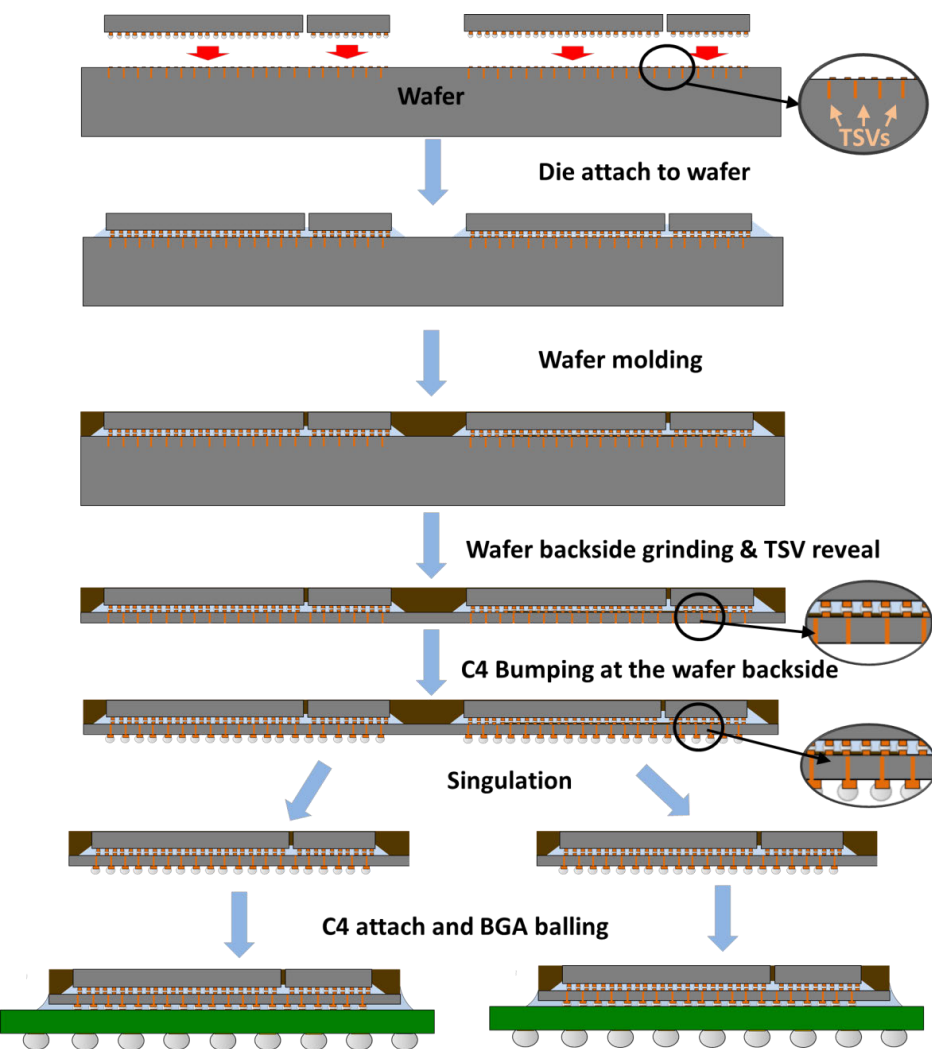


Benign case

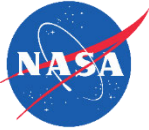
	Application challenges	Quality issues related to reliability
CUF	CUF voiding, as pitch reduces and die size increases.	Voiding : 1) Reduced thermal cycling life. 2) Sn whisker questions from customers
NCP	1) Fillet length control, when placing dies very close to each other. 2) Defect : NCP entrapment, NCP voiding (mostly small)	Early failure of solder joint by thermal cycling
NCF	1) Die shelf life (NCF is a B-stage material) 2) Defect: NCF entrapment	Early failure of solder joint by thermal cycling



Manufacturing Process Challenge Example



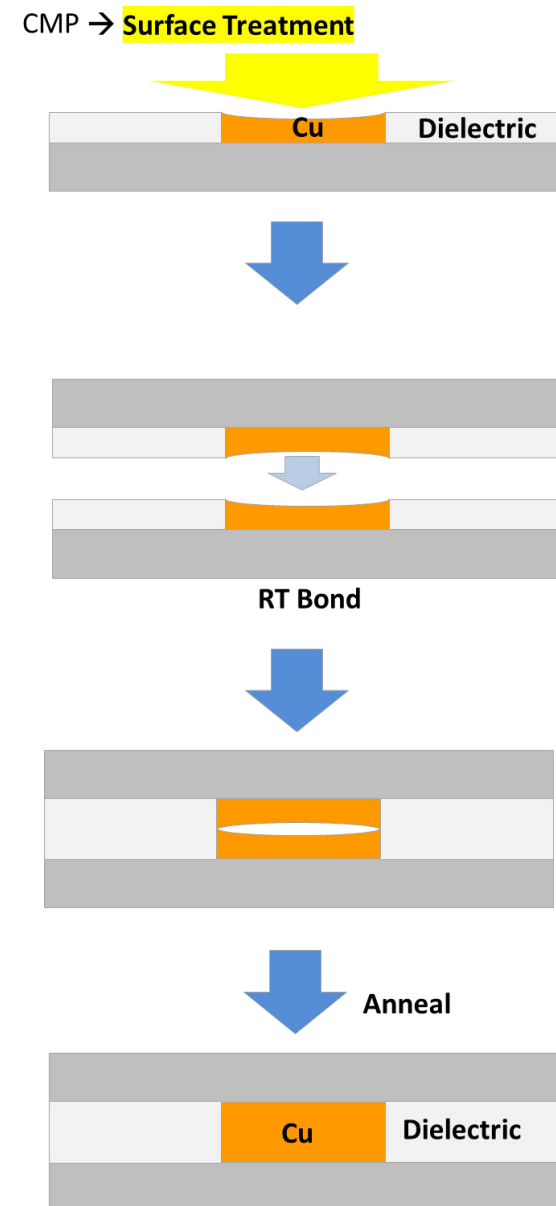
- Manufacturing challenges from a literature on TSMC CoWoS-S
 - μ bump open
 - TSV-C4 open
 - Incomplete TSV liner removal mainly at the wafer edge
 - Backside grinding process optimization per wafer warpage variation
 - ESD damage of transistors (New failure mechanism)
 - Die pick and place
 - Creation of different voltage potential between die and wafer.
 - Wafer thinning and back-side TSV reveal :
 - Creation of ESD discharging path between front side transistors and back side TSV surface.
 - Potential plasma damage during TSV reveal by recess etching.
 - **Highly iterative troubleshooting was needed to solve these issues.**
 - Inline inspection/test can't catch the defects.
 - Diagnostic test and test pattern were developed.
- **OSATs may need comparable engineering/troubleshooting capability, if yield is important.**
- **It is not clear what types of defect will form under different process and materials, or if those defects will cause long-term failure.**

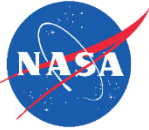


Hybrid Bonding

- The current FY23 task is shifting focus on hybrid bonding.
- Bonds both dielectric and copper. DBI (Direct Bond Interconnect) is the most commonly used process.
 - Surface plasma and chemical treatments
 - Dielectric (ex: SiO₂, SiCN, SiON) bonded at RT, without compression.
 - Post bonding annealing. → Cu thermal expansion and Cu–Cu bonding
 - Recent industry R&Ds are often focused on D2W and lowering annealing temperature.
- Need high surface coplanarity and cleanness : Only W2W or D2W, not substrate.
 - Needs surface coplanarity control (nm range): CMP and wafer warpage.
 - Requires well-controlled cleaning process and high-level clean room.
 - ISO-5, 4. Can be also done in ISO-6. Many advanced packaging OSATs use ISO-7.
- W2W
 - Long history since image detectors.
 - Smaller pitch than D2W. (2.5~8μm, 1μm demonstrated)
 - Drawback for HI
 - Can't sort KGD (yield loss, as # stack increases).
 - Upper and lower die have to the same size.
- D2W
 - Already used in a commercial product (Ryzen 7 5800x3D)
 - Manufacturing challenges : Yield loss due to defects/contaminants from singulation.
 - In addition, already singulated dies in general have more contaminant than wafer.

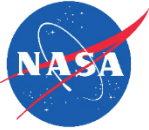
NEPP





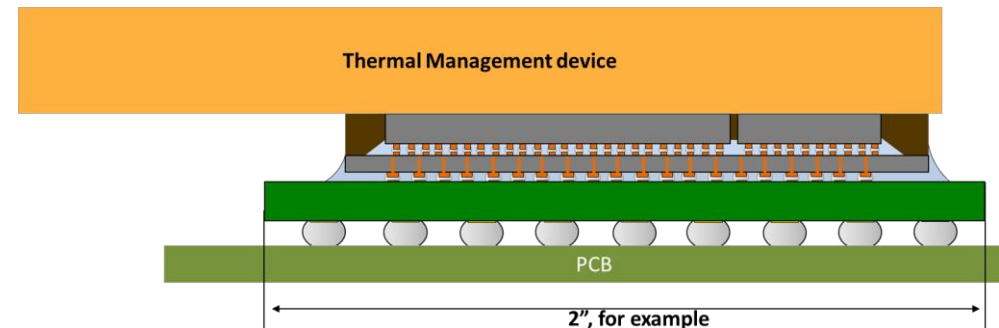
Hybrid Bonding (cont.)

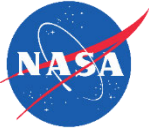
- 'Reliable if built right' seems highly applicable.
- FY23 – 24 topics to focus
 - D2W
 - Likely path for HI. Since enables selectively integrating KGD and multiple small dies on a larger die.
 - Already commercial products are using this process.
 - Manufacturing challenges, common defects, quality, and reliability.
- Examples of the current task's working investigation
 - Process defects, such as voiding in dielectric or copper
 - Void is frequently characterized during process/technology development. But voiding does not always result in yield loss.
 - Then what kind of voids are allowed/not allowed for reliability? How much void is allowed? How do can we screen them? What if there are many small voids below CSAM resolution instead of a large void?



Additional Remarks on Assembly Level Reliability

- Assembly-level reliability.
 - Often HI packages are larger than typical single-die BGA.
 - Board-level reliability (Shock, Vibe, and TC) will be lower than CCGAs with same size.
 - Heat transfer can further reduce the board-level reliability.
- Board effect on package internal reliability
 - When attached to board, a package (mostly non-hermetic) can exhibit new internal failure mechanism.
 - New or elevated chip-package interaction when assembled to board.
 - JEP150 lists many potential failure mechanisms.
 - It is difficult to know what are real. Some companies only check for thermal cycling reliability.
 - HI will have very diverse architectures and material.
 - We will need to start conversation on how to assess the assembly-level effect.
- Package stiffener
 - Since HI packages are larger than typical single-die BGAs, they will have greater substrate warping during SMT. Warping makes the part difficult to assemble.
 - Ability to design and properly attach stiffener should be considered when selecting supplier.
 - In addition to design, adequate attachment process is needed to control warpage.





Summary

- Traditional approach of developing requirement based on packaging architecture is becoming difficult.
- Reliable if built right.
 - Verifying if a manufacture's process is well-established is far more challenging than traditional flip chip.
 - Diverse process : Similar packaging architecture, different processes
 - Sophisticated process : Need expertise to understand the details of the process
- Below are some of the suggestions/questions when determining screening and qual:
 - Lot defined in detail based on potential defect creation mechanism for given assembly process and materials.
 - Screening
 - Parameters based on failure rate data. Data from multiple lots that were defined in detail.
 - Pb-free μ bump : Reject underfill void bridging more than 2 μ bump? Is it feasible for stack-up and resolution?
 - Qualification
 - If a QML part goes through frequent process and material changes, how should we handle PIDTP?
- When initiating conversation with potential packaging service provider that does not have a high-volume commercial product released in the market, detailed questions should be asked.
For example:
 - 1) In their products, how the full-stack up was built at what dimension, what was the yield at what QTY.
 - 2) How they deal with reliability-related process challenges.
 - 3) If the supplier suggests their standard materials set, do they have reliability characterization data.



- FY23 plans:

- 1) Revive industry working group telecon :

- New developments in commercial, mil/aero and government, applicability of commercial practices to mil/aero, supply chain, etc

- 2) More focus on hybrid bonding.

- 3) Investigate cases in automotive parts.

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