National Aeronautics and Space Administration

State of Memory Pattern Assessment

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

Seraina Murphy, Brayden Hesford, Ryan Ross, and Armian Hanelli[1]
Jet Propulsion Laboratory, California Institute of Technology

JPL Project Number: 107590
Task Number: 40.31.55.02.02

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

http://nepp.nasa.gov

[1]Current affiliation is Apple Inc. in San Diego, CA

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

©2022 California Institute of Technology. Government sponsorship acknowledged.

Introduction

Memory devices are a critical element of NASA spacecraft and instruments, enabling various compute, navigation, and data collection activities that are essential to mission success. Unfortunately, within space exploration, there have been multiple documented cases of anomalies that were attributed to non-radiation memory issues, such as soft or weak bits, or state-dependent layout-related interactions with neighboring cells [1-3]. Such anomalies have had varying degrees of impact to missions, and may have contributed to a total loss of spacecraft [4]. This means that the memory pattern screening tests deployed at the time were insufficient to isolate flight parts with these types of anomalies.

The memory industry as a whole has made significant progress in the development and implementation of advanced memory patterns and testing schemes, and many of these can help identify the types of anomalies that have caused previous mission failures. Improvements in memory devices and testing technology have also reduced time requirements of pattern testing. This creates an opportunity to improve our memory testing practices by implementing updated patterns and more complex testing schemes on our mature memory technologies to enhance detection of hidden reliability issues. Furthermore, memory devices are often redundantly installed in spacecraft to minimize the likelihood of failure, adding significant weight to the craft. Increased reliability of individual memories could provide justification to reduce the number of memory devices used in future applications. It is therefore the goal of this research effort to assess current industry memory pattern testing and document the extent of fault coverage of the memory patterns used on current flight parts.

Methods

The memory devices included in this research were limited to random access memory (RAM) and read-only memory (ROM) devices that encompassed the majority of memories listed in the JPL parts database. Two volatile memory types were assessed: static RAM (SRAM) and synchronous dynamic RAM (SDRAM). Multiple non-volatile types were assessed: not-and (NAND) Flash and not-or (NOR) Flash, magnetic RAM (MRAM), ferroelectric RAM (FeRAM), programmable ROM (PROM), and electrically erasable, programmable ROM (EEPROM). Descriptions of these are available in Appendix A. The pattern tests applied to these devices were obtained through a review of the part documentation at JPL and datasheets and drawings available in the public domain. In addition, manufacturers were asked to respond to questions about the patterns applied throughout the fabrication of these parts. Seven memory manufacturers were contacted for pattern test information, although only five of these were included in the final dataset. Parts from five other manufacturers were also included due to the accessibility of some pattern test information, although these manufacturers were not contacted. In total, parts from ten manufacturers were considered, and the manufacturers were arbitrarily designated 1-10 to maintain anonymity. It was observed that the die manufacturers were often different from the packaging manufacturers, but because the die manufacturers were not readily available in the JPL databases, die manufacturers were not contacted as part of this investigation.

The test patterns were recorded at four levels of memory testing: die-level screening, package-level screening, and electrical tests and radiation tests performed at JPL after the parts were received from the manufacturers. The voltages and temperatures at which patterns were applied were also recorded for each stage of testing. The scope of this investigation did not account for all parameters that should be considered for memory test procedures, such as manufacturer proof-of-concept testing or applied frequency.

Pattern test requirements were obtained from multiple sources. Memory devices with part numbers beginning with 5962- have test requirements defined in the Defense Logistics Agency (DLA) standard microcircuit drawings (SMDs), which are publicly available, and many of which contain explicit pattern tests. The SMDs were reviewed

for all 5962- devices in the JPL parts database, and any listed patterns were recorded. An assumption was made in the final data set that any pattern listed in an SMD was guaranteed to be applied to those memories at the package level. However, the accuracy of this assumption is not guaranteed, as testing to SMD requirements was only confirmed by one manufacturer. For devices without 5962- part numbers, this research relied heavily on manufacturer input, as manufacturer datasheets and the documentation received with device lots did not disclose pattern test information. Devices with JPL-assigned part numbers tended to have documented JPL screening procedures, and these test patterns were recorded.

The fault coverage of each of the applied patterns was also assessed. This was done by reviewing publications about pattern test experiments and identifying applications of patterns, which typically resulted in the detection of different fault types. It should be noted that a 'random pattern' was identified as a pattern used by at least one manufacturer, but the nature of this pattern was not defined; i.e., it was not disclosed whether one or all cells were randomly written, nor was the order of reading and writing to cells identified. Consequently, the fault coverage of this pattern was omitted. Also, although the time requirements of pattern tests were different and some tests may affect device lifespan more than others, this aspect of testing was not addressed in this research effort. The faults examined included the classical fault models, which include stuck-at faults (SAF), address decoder faults (AF), transition faults (TF), inversion coupling faults (CFin), idempotent coupling faults (CFid), and state coupling faults (SCF). These faults are summarized in Table 1. Additional fault models exist, although these were not addressed in this investigation. A short description of some of these are available in Appendix B. A summary of the pattern algorithms is also available in Appendix C.

Fault Type	Description
Stuck-At Fault (SAF)	The logic value of a cell is always 0 or 1
Address Decoder Fault (AF)	Two or more addresses or words are connected together, or certain words cannot be accessed with a specific address or addresses
State Transition Fault (TF)	A cell or line that is unable to undergo a 0→1 or 1→0 transition when it is written (the transition may occur in one direction but not the other)
Coupling Fault (CF)	Occurs between two cells when the logic value of a cell is influenced by the content or operation of another cell
Inversion Coupling Fault (CF(in))	A transition in a coupling cell (aggressor) complements the coupled cell (victim)
Idempotent Coupling Fault (CF(id))	A coupled (victim) cell is forced to 0 or 1 if the coupling (aggressor) cell transits from 0→1 or 1→0
State Coupling Fault (SCF)	A coupled (victim) cell is forced to 0 or 1 if coupling (aggressor) cell is in given state

Table 1. Summary of classical fault models.

Results

The pattern test data was compiled into a table organized by memory type, manufacturer, and stage of testing. A color-coded summary of these results is available in Tables 2 through 4. Table 2 contains a color key of the patterns found and a summary of the fault coverage of each pattern. In Table 2, although the term 'all' is used to indicate that a pattern is capable of detecting all of a given fault type, this assumes ideal testing conditions (voltage, temperature, and frequency), so it is still possible for a given pattern not to correctly identify the fault. Table 3 shows the known pattern tests performed at the manufacturers, and Table 4 contains the patterns applied at JPL during screening and radiation testing. For situations where the pattern test information could not be determined, the color grey was used. For situations where it was not clear whether a pattern was applied to some or all of a given memory type (ex. all SRAMs from manufacturer 6), an asterisk was used in addition to the pattern color.

Color Key		Fault Coverage					
Color	**Pattern**	**SAF**	**AF**	**TF**	**CF(in)**	**CF(id)**	**SCF**
	Checkerboard/ Inverse Checkerboard	All	-	Some	Some	Some	Some
	Solids (ex. all 0s)	All	Some	-	-	-	-
	CEDES Checkerboard & Inverse Checkerboard	All	-	Some	Some	Some	Some
	Marching Address	All	All	All	-	-	-
	March C-	All	All	All	Some	Some	Some
	Modified March C-	All	All	All	All	Some	All
	March X	All	All	All	All	-	-
	March Y	All	All	All	All	-	-
	March Left-Right	All	All	All	-	-	-
	March XY	All	All	All	-	-	-
	March (variation not specified)						
	GALPAT	All	All	All	Some	Some	Some
	Walking Ones/Zeros	All	All	All	Some	Some	Some
	Sliding Diagonal	All	All	All	Some	Some	Some
	Random Data Pattern						
*	Pattern may or may not apply to all memories from the specified manufacturer						
	No additional patterns applied						
	Unknown: Additional patterns may or may not be applied						

Table 2. Color key and fault coverage of applied patterns used in Tables 3 and 4. The fault coverage columns indicate the degree to which applying a given pattern would aid in the detection of that fault type (assuming ideal test conditions).

Type	Mfg.	Die-level tests						Package-level tests											
		Patterns				Voltages	Temps.	Patterns										Voltages	Temps.
PROM	1					Min/Max	25C											Min/Max	Min/25C/Max
	2							*	*	*	*	*	*					Min/Max	Min/25C/Max
	4																		
EEPROM	2							*	*	*	*	*	*					Min/Max	Min/25C/Max
	3										*							Min/Max	Min/25C/Max
	4							*	*										Min/25C/Max
	5							*										Min/Max	Min/25C/Max
	9							*										Min/Max	Min/25C/Max
	10							*										Min/Max	Min/25C/Max
FeRAM	6	*	*	*	*			*	*	*	*								
MRAM	1					Min/Max	25C											Min/Max	Min/25C/Max
	2							*	*	*	*	*	*	*				Min/Max	Min/25C/Max
NAND Flash	3										*							Min/Max	Min/25C/Max
	7																		
	8																		
NOR Flash	3										*							Min/Max	Min/25C/Max
	6	*	*	*	*			*	*	*	*								
SDRAM	1					Min/Max	25C											Min/Max	Min/25C/Max
	3										*							Min/Max	Min/25C/Max
	4																		
SRAM	1					Min/Max	25C											Min/Max	Min/25C/Max
	2							*	*	*	*	*	*	*	*	*	*	Min/Max	Min/25C/Max
	4																	Min/Max	Min/25C/Max
	5							*	*	*	*							Min/Max	Min/25C/Max
	6	*	*	*	*			*	*	*	*							Min/Max	Min/25C/Max

Color Key	
Color	Pattern
	Checkerboard/ Inverse Checkerboard
	Solids (ex. all 0s)
	CEDES Checkerboard & Inverse Checkerboard
	Marching Address
	March C-
	Modified March C-
	March X
	March Y
	March Left-Right
	March XY
	March (variation not specified)
	GALPAT
	Walking Ones/Zeros
	Sliding Diagonal
	Random Data Pattern
*	Pattern may or may not apply to all memories from the specified manufacturer
	No additional patterns applied
	Unknown: Additional patterns may or may not be applied

Table 3. Known pattern screening tests performed by the manufacturers. The manufacturers are anonymized with numbers 1-10. The color key is shown for reference.

Type	Mfg.	Additional JPL Qual/Screening					Radiation Effects Screening			
		Patterns			Voltages	Temperatures	Patterns		Voltages	Temps.
PROM	1						*	*	Min*/Max*	Min*/25C*/Max*
	2						*	*	Min*/Max*	Min*/25C*/Max*
	4						*	*	Min*/Max*	Min*/25C*/Max*
EEPROM	2						*	*	Min*/Max*	Min*/25C*/Max*
	3						*	*	Min*/Max*	Min*/25C*/Max*
	4	*	*				*	*	Min*/Max*	Min*/25C*/Max*
	5						*	*	Min*/Max*	Min*/25C*/Max*
	9						*	*	Min*/Max*	Min*/25C*/Max*
	10						*	*	Min*/Max*	Min*/25C*/Max*
FeRAM	6						*	*	Min*/Max*	Min*/25C*/Max*
MRAM	1						*	*	Min*/Max*	Min*/25C*/Max*
	2						*	*	Min*/Max*	Min*/25C*/Max*
NAND Flash	3						*	*	Min*/Max*	Min*/25C*/Max*
	7	*	*	*	Min/Max	Min/25C/Max	*	*	Min*/Max*	Min*/25C*/Max*
	8	*	*	*	Min/Max	Min/25C/Max	*	*	Min*/Max*	Min*/25C*/Max*
NOR Flash	3						*	*	Min*/Max*	Min*/25C*/Max*
	6						*	*	Min*/Max*	Min*/25C*/Max*
SDRAM	1						*	*	Min*/Max*	Min*/25C*/Max*
	3						*	*	Min*/Max*	Min*/25C*/Max*
	4						*	*	Min*/Max*	Min*/25C*/Max*
SRAM	1	*	*		Min/"Nominal"/Max	Min/25C/Max	*	*	Min*/Max*	Min*/25C*/Max*
	2						*	*	Min*/Max*	Min*/25C*/Max*
	4						*	*	Min*/Max*	Min*/25C*/Max*
	5						*	*	Min*/Max*	Min*/25C*/Max*
	6						*	*	Min*/Max*	Min*/25C*/Max*

Color Key	
Color	Pattern
	Checkerboard/ Inverse Checkerboard
	Solids (ex. all 0s)
	CEDES Checkerboard & Inverse Checkerboard
	Marching Address
	March C-
	Modified March C-
	March X
	March Y
	March Left-Right
	March XY
	March (variation not specified)
	GALPAT
	Walking Ones/Zeros
	Sliding Diagonal
	Random Data Pattern
*	Pattern may or may not apply to all memories from the specified manufacturer
	No additional patterns applied
	Unknown: Additional patterns may or may not be applied

Table 4. Known pattern screening tests performed at JPL. The manufacturers are anonymized with numbers 1-10. The color key is shown for reference.

There were multiple barriers to obtaining explicit test information for the parts in the JPL database. Of the manufacturers that did reply to the request for information, most of the replies remained vague due to the proprietary nature of their processes. Most of the patterns, voltages, and/or temperatures relayed by manufacturers were not specific to any memory category (ex. SRAMs vs EEPROMs), so it was often unclear whether a given pattern applied to some or all of the devices produced. Die-level testing was particularly limited, possibly due to the die manufacturers being different from the packaging manufacturers. Lastly, for devices with SMDs in the DLA database, it was found that not all SMDs contained comprehensive pattern test information. In particular, the SMDs for the ROM devices (PROMs, EEPROMS) and some SDRAMs contained voltage and temperature requirements but did not list any patterns. Additionally, only one manufacturer was able to confirm that they tested their memories using the patterns contained in the SMDs, so it was not clear whether all manufacturers adhered to SMD pattern testing requirements.

Based on the data that was obtained, there was no universal set of pattern requirements for any memory types, although some patterns were more commonly used than others. Most (if not all) memories were subjected to a checkerboard pattern at some stage of testing. The next most common pattern was solids (ex. all zeros). Other applied patterns depended on the manufacturer or the tests listed in SMDs. There tended to be some form of a March pattern applied, though the identified varieties of March test ranged widely and the fault coverage was not consistent across all March variations. For the devices with 5962- part numbers, the patterns that were listed in SMDs for RAM devices typically included a combination of Checkerboard and Inverse Checkerboard (with and without CE deselected), March X/Y/XY, and a modified March pattern similar to March C-.

It was discovered that the number of memory devices that were screened at JPL with pattern tests was relatively small; the majority of screening test requirements included Destructive Physical Analysis (DPA) type procedures rather than pattern applications. DPA processes are generally good for detecting more severe or systemic physical anomalies such as packaging defects or bonding anomalies, but are not intended to detect memory failures and subtle anomalies such as weak bits. There were no overarching JPL screening requirements for any given memory type, and the requirements were independent of the device manufacturer. Of the approximately 800 memory device entries in the JPL parts database, 106 of these had JPL screening procedures, and just 13 of these requirements (approximately 1.5% of all database entries) included directions for pattern testing. The majority (10 of 13) of the memories with pattern test screening were NAND Flash devices, but the requirements did not apply to all NAND Flash devices, nor did they apply to all NAND Flash memories from any one manufacturer.

Radiation testing requirements were found to be device-specific, similar to non-radiation JPL screening requirements. This testing was outlined by standard operating procedures (SOPs) MIL-STD-883 [5] and JESD57 [6], but there were no pattern testing requirements in either document. There were also no NASA-internal documents governing pattern selection for testing. Per discussions with the radiation testing team at JPL, checkerboard and solid patterns are considered to have generally adequate fault coverage. However, all test plans are ultimately dependent on the device's intended use for a project, and no pattern is guaranteed. In addition, although it is common for radiation testing to occur at the limits of a device's temperature and voltage range, JESD57 (section 5.2.5.3) recommends using 'worst-case' conditions, which does not guarantee temperature or voltage extremes, as the 'worst-case' for different memory types and tests may be achieved under varying conditions. As an example, for single-event latchup (SEL) testing it is generally recommended to use maximum operating voltage and maximum case temperature, whereas for single-even burnout tests (SEB), maximum reverse-bias voltage and minimum case temperature tend to be ideal. Ultimately, radiation test plans are at the discretion of the testers.

Assessment of the known patterns for their fault coverage revealed that there were gaps in coverage for many of the memories in the JPL database. In particular, coupling faults were the least covered by a majority of

patterns, including many of the March variations [7-10]. There were some cases where the only confirmed patterns applied to a specific device were the checkerboard, or a combination of checkerboard and solids, which do not cover all address decoder faults, transition faults, or coupling faults [9,10]. In other cases, the applied patterns included March X and/or March Y, which is a more comprehensive testing suite, but would still miss some idempotent and state coupling faults [7,9,10]. The most comprehensive coverage of the patterns assessed was found to be the modified March C- pattern [7,9-11]. This pattern was applied to many (but not all) devices with 5962- part numbers per the DLA SMDs, and only one manufacturer verified the usage of this pattern. Although it is possible the reviewed devices may have been subjected to tests beyond those compiled in this dataset, this cannot be confirmed without additional input from the manufacturers of those parts.

Another issue identified by this investigation was the limitation of applied voltages and temperatures during pattern testing. The data reveals that memories are generally tested during manufacturing only at minimum and maximum rated voltages, and at minimum, maximum, and ambient (25°C) temperatures. Given the variability of environments that can occur in a single mission (ex. during launch, in the vacuum of space, in the atmosphere of another planet, etc.), it is therefore possible for an escape to occur in conditions that fall in-between these prescribed intervals. For this reason, it may be beneficial for memory testing at JPL and NASA to include Shmoo plotting pattern applications over the functional ranges of voltage and/or temperature. Because device and testing technology advancements have reduced test time requirements substantially (a pattern test that took days to complete in the early stages of memory testing may now take minutes or seconds), more comprehensive test suites have become an accessible screening solution. Additional research would be required to assess the full impact of testing requirements on cost and schedule.

Conclusion

This study revealed that the pattern test information for memory devices is largely unknown at JPL, particularly for die-level testing, and the pattern test requirements are often left to the discretion of the manufacturers, resulting in varied testing requirements for each memory type. Furthermore, it was determined that the screening procedures at JPL typically do not contain any additional pattern testing requirements. To ensure the quality of patterns applied, particularly for memories that are not covered by DLA SMDs, it may be beneficial for NASA memory experts to request from manufacturers that the pattern tests be included in the documentation that is supplied with delivered parts. It is recommended that a review process of that data be established and general testing guidelines for each memory type be issued to ensure all memories of a given type receive a similar minimum level of testing. I In the event pattern testing at a given manufacturer is deemed insufficient, NASA may consider including enhanced pattern testing suites in memory screening procedures, which could include applying new patterns or applying existing patterns over a wider range of voltages and temperatures.

References

[1] Y. Chen et al., “EEPROM Bit Failure Investigation,” *6th Military and Aerospace Programmable Logic Devices International Conference*, Sept 2003.

[2] Y. Chen, “Body of Knowledge Guideline Document on Commercial MNOS EEPROM in Space Applications,” *NEPP 2005 Report*, pp. 6-7, Apr 2006.

[3] R. Sosland, et al., “Getting Back on the Road: Reformatting Flash Memory On-board the Mars Exploration Rover Opportunity,” *IEEE Aerospace Conference*, 2015.

[4] “Report on the Loss of the Mars Polar Lander and Deep Space 2 Missions,” *Jet Propulsion Laboratory*, pp. 68-70, 22 March 2000.

[5] Military Specification (MIL)-STD-883, *Test Method Standard for Microcircuits*, Rev. L, DOD, 16 Sept 2019.

[6] Test Standard JESD57A, “Test Procedure for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy-Ion Irradiation,” Rev. A, JEDEC, Nov 2017.

[7] J-F Li, “EE6083 VLSI Testing: Testing of Random Access Mememories [*sic*],” National Central University, PowerPoint presentation, https://eecs.ceas.uc.edu/~jonewb/Memory.pdf, Dec 2012.

[8] L-T Wang, C-W Wu, and X Wen, “VLSI Test Principles and Architectures: Design for Testability, 1st Ed.” Elsevier Inc, 2006.

[9] M. Mamatha, and M. Muralidhar, “Memory Testing Using March C Algorithm,” *VLSICS Journal*, vol 2, issue 7, pp 512-517, Oct 2014.

[10] W-B Jone, “ECECS 682 VLSI Testing and Validation: Memory Testing,” University of Cincinnati, PowerPoint presentation, https://eecs.ceas.uc.edu/~jonewb/Memory.pdf, Spring 2008.

[11] S. Hamdioui, A. J. van de Goor, and M. Rodgers, “March SS: A Test for All Static Simple RAM faults,” *IEEE Proc. Intl. Workshop on Memory Technology, Design and Testing*, Feb. 2002.

Acknowledgements

Special thanks to Gregory Allen and Leif Scheick from the JPL Radiation Effects department for their inputs on radiation testing requirements and procedures.

Appendices

Appendix A – Memory Type Definitions

This section provides brief descriptions of each of the memory types that were investigated for pattern tests.

Volatile Memory: These types of memories (SRAM and DRAM/SDRAM defined below) only retain data for as long as power is applied.

SRAM: Static Random-Access Memory is a volatile memory that retains its data contents for as long as power is connected. This type of memory does not require frequent refreshing like dynamic RAM (DRAM), and interfacing with SRAM is generally easy. However, this memory uses six transistors per bit, so the device size increases considerably when the data storage capacity is increased.

SDRAM: Synchronous Dynamic Random-Access Memory is a type of DRAM for which the clock signal is externally supplied. A DRAM needs regular refresh cycles to prevent its contents being lost, but uses only one transistor and a capacitor per bit, which allows it to reach much higher densities and have a lower per-bit cost than SRAM.

Non-Volatile Memory: These types of memory are able to retain data without requiring a constant application of power. Non-volatile memories include Flash, MRAM, FeRAM, PROMs, and EEPROMs, which are defined below.

Flash: NAND and NOR Flash memory consists of floating gate MOSFET cells, and they are named depending on whether they have NAND or NOR logic gates. These devices can be electrically erased and reprogrammed. Unlike EEPROMs, Flash memories do not need to be completely erased before they can be rewritten.

MRAM: Magneto-resistive Random-Access Memory have magnetic storage elements formed from two ferromagnetic plates separated by a thin insulating layer. Each plate can be independently magnetized: one plate is permanently set to particular polarity, and the other plate's magnetization can be changed to match the polarity of an externally applied field. If both polarities are the same, this results in a low-resistance (logic 0) in the magnetic tunneling junction, and if they are opposing, this yields a high resistance (logic 1). The advantages of MRAM over other non-volatile memories is faster speed, lower power consumption, and can be scaled down for reduced device size, but these devices also typically have lower storage densities and higher cost.

FeRAM: Ferroelectric Radom Access Memory is similar in construction to DRAM but using a ferroelectric layer instead of a dielectric layer to achieve non-volatility. These devices have significantly faster read/write times and lower power consumption than other non-volatile varieties like EEPROMs and Flash.

PROM: Programmable Read-Only Memory is a device where the contents can only be programmed once, after which the device can be read but the data can never be re-written.

EEPROM: Electrically Erasable Programmable Read-Only Memory is a device for which the contents can be re-programmed multiple times with a pulsed voltage. This type of memory typically has small erasable and is used in applications with smaller storage requirements, but the devices typically have a longer lifespan than other non-volatile varieties.

Appendix B – Other Fault Definitions

This section provides a brief description of additional fault types that were not considered when assessing patterns for fault coverage.

Neighborhood Pattern Sensitive Fault: Cell is affected by what happens around it usually during writing (can be thought of as a capacitive coupling fault)

Write Destructive Fault: Non-transition write operation in a memory cell causes the cell to flip (ex. cell is 0, write 0, cell reads 1)

Read Destructive Fault: Non-transition read operation in a memory cell causes the cell to flip (ex. cell is 0, read 0, cell changes to 1)

Deceptive Read Destructive Fault: Read command flips the value from the incorrect one to the correct one and reads correct value

Data Retention Fault: Memory is not able to hold data for a specific amount of time

Parametric Fault: The electrical parameters of the circuit components are outside their expected ranges of values (between the min and max range of fault-free operation)

Bit-Pattern Fault: Occurs in programmable ROMS where programming faults may occur, a 0 may be programmed rather than a 1 for example

Sense Amplifier Recovery Fault: Occurs in the RAM when the sense amplifier saturates after a long run of logic 0 and/or 1 read/write operations

Write Recovery Fault: Occurs when a write operation is followed by a read/write operation at a different location but the operation results in a read/write operation at the original location

Appendix C – Pattern Algorithms

This section contains a table of the patterns that were found to be applied to any of the memory devices in the JPL parts database. The algorithms for each pattern are described.

Pattern	Algorithm
Checkerboard/ Inverse Checkerboard	Complementary data are written into alternate memory locations in a checkerboard pattern. Then the checkerboard is read in up addressing order. The inverse pattern is then written and read.
Solids (Zero-One)	Also known as MSCAN. Write uniform data to all cells from minimum address to maximum address, then read all. Write complement data to all cells from minimum address to maximum address, then read all.
CEDES Checkerboard & Inverse Checkerboard	Checkerboard is loaded to memory, device is deselected, an attempt is made to load the inverse checkerboard, and then the checkerboard output pattern is verified. Repeat process with patterns inverted.
Marching Address (Marching Ones/Zeros)	1. Load memory with background data to all cells in any order (ex. all "0's"). 2. Read data in location 0. 3. Write complement data to location 0. 4. Read complement data in location 0. 5. Repeat steps 2-4 incrementing address sequentially for each location in the array. 6. Read complement data in maximum address location. 7. Write data to maximum address location. 8. Read data in maximum address location. 9. Repeat steps 6 through 8 decrementing address sequentially for each location in the array. 10. Write complement background data to all cells in any order. 11. Read complement data in location 0. 12. Write data to location 0. 13. Read data in location 0. 14. Repeat steps 11-13 incrementing address sequentially for each location in the array. 15. Read data in maximum address location. 16. Write complement data to maximum address location. 17. Read complement data in maximum address location. 18. Repeat steps 6 through 8 decrementing address sequentially for each location in the array.
March C-	1. Load memory with background data to all cells in any order (ex. all "0's"). 2. Read data in location 0. 3. Write complement data in location 0. 4. Repeat steps 2 and 3 incrementing address sequentially for each location of the array. 5. Read data in location 0. 6. Write complement data in location 0. 7. Repeat steps 5 and 6 incrementing address sequentially for each location of the array. 8. Read data in maximum address location. 9. Write complement data in maximum address location. 10. Repeat steps 8 and 9 decrementing address sequentially for each location of the array. 11. Read data in maximum address location. 12. Write complement data in maximum address location. 13. Repeat steps 11 and 12 decrementing address sequentially for each location of the array. 14. In any order, read data from all addresses.

Pattern	Algorithm
Modified March C-	1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's"). 2. Read data in location 0. 3. Write complement data to location 0. 4. Read complement data in location 0. 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array. 6. Read complement data in maximum address location. 7. Write data to maximum address location. 8. Read data in maximum address location. 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array. 10. Read data in location 0. 11. Write complement data to location 0. 12. Read complement data in location 0. 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array. 14. Read complement data in maximum address location. 15. Write data to maximum address location. 16. Read data in maximum address location. 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array. 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.
March X	1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's"). 2. Read data in location 0. 3. Write complement data to location 0. 4. Read complement data in location 0. 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array. 6. Read complement data in maximum address location. 7. Write data to maximum address location. 8. Read data in maximum address location. 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array. 10. Read data in location 0.
March Y	1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's"). 2. Read data in location 0. 3. Write complement data to location 0. 4. Read complement data in location 0. 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array. 6. Read complement data in maximum address location. 7. Write data to maximum address location. 8. Read data in maximum address location. 9. Repeat steps 6 through 8 decrementing Y-fast sequentially for each location in the array. 10. Read data in location 0.

Pattern	Algorithm
March Left-Right	1. Increment address from minimum to maximum writing each address with alternating data pattern (x55). 2. Increment address from minimum to maximum while performing 2a and 2b 2a. Read and verify an address. 2b. Write the address with complement data. 3. Decrement address from maximum to minimum while performing 3a, 3b, 3c, 3d. 3a. Read and verify an address. 3b. Write the address with complement data. 3c. Read and verify the address. 3d. Write the address with complement data. 4. Decrement address from maximum to minimum while performing 4a and 4b 4a. Read and verify the address 4b. Write the address with complement data 5. Decrement address from maximum to minimum while performing 5a, 5b, 5c, and 5d 5a. Read and verify the address 5b. Write the address with complement data 5c. Read and verify the address 5d. Write the address with complement data 6. Decrement address from maximum to minimum while performing 6a 6a. Read and verify the address
March XY	1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's"). 2. Read data in location 0. 3. Write complement data to location 0. 4. Read complement data in location 0. 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array. 6. Read complement data in maximum address location. 7. Write data to maximum address location. 8. Read data in maximum address location. 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array. 10. Read data in location 0. 11. Write complement data to location 0. 12. Read complement data in location 0. 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array. 14. Read complement data in maximum address location. 15. Write data to maximum address location. 16. Read data in maximum address location. 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array. 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.
March (variation not specified)	No algorithm specified: the manufacturer indicated that some variation of a march pattern is used during memory testing, but the exact variation was not given.
GALPAT (Ping-Pong)	A background of zeroes written into all memory cells. Then the first cell becomes the test cell, which is complemented and read alternately with every other cell in memory. Each succeeding cell then becomes the test cell in turn and the entire read process is repeated. All data are complemented and the entire test is repeated.
Walking Ones/Zeros	Similar to the GALPAT except the test cell is read once and then all other cells are read. To create a Walking Pattern from the GALPAT program, omit the second read operation in the testbench
Sliding Diagonal	Similar to GALPAT, but instead of shifting a one through memory, a complete diagonal of 1s is shifted
Random Data Pattern	Not standardized: a random pattern could consist of a solid pattern with a single, randomly-placed, complementary cell, or all cells could have randomly generated data. The data may be written to all cells and then read, or random data is written and read at incrementing addresses.