Observation of Low-Energy Proton Direct Ionization in a 72-Layer 3D NAND Flash Memory

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***Abstract*—Single-event upsets are observed in a 72-layer 3D NAND flash memory operated in single-level cell mode after low-energy proton (500 keV-1.2 MeV) and heavy ion irradiation. The layer-by-layer error count is analyzed to visualize the stopping of low energy protons within the memory stack, and Monte Carlo simulations are correlated with the experimental data. Direct ionization by low-energy protons is identified by three-dimensional data analysis and the energy dependence of device sensitive cross-section. Heavy ion data is also presented for comparison.**

***Index Terms*—Direct ionization, flash memory, proton, single-event upset, three-dimensional NAND**

I. Introduction

NAND flash memories continue scaling in the third dimension [1] by vertically stacking floating-gate and charge-trap cells. State of the art products from multiple manufacturers have reached 128 to 176 layers [2], [3] and 1 Tb [4], [5] of memory within a single, monolithic silicon die. Substantial previous work exists on both planar [6]–[8] and 3D [9]–[11] NAND flash total ionizing dose (TID) and single-event effect (SEE) response; evidence of direct ionization by protons in a highly-scaled (25 nm node) planar flash device has been shown when operated in multi-level cell mode [12]. Here, direct ionization by low-energy (<1 MeV) protons [13]–[15] is observed in a 72 layer 3D NAND flash process operated in single-level cell (SLC) mode. Heavy ion and Monte Carlo simulation data are provided for comparison and additional insight into the device response.

II. Test Setup

A. Component Description

A 4 Tb, triple-level cell (TLC) 3D NAND flash device (Hynix H25QFT8F4A9R-BDF) consisting of eight die stacked in a plastic 132-ball low-profile ball grid array (LBGA) was commercially procured for heavy-ion and proton testing. Internally, each 512 Gb die is a 72-layer TLC 3D NAND charge-trap flash memory. The core voltage (V_{CC}) is 3.3 V nominally while the I/O (V_{CCQ}) is 1.8 V. The listed capacities apply when operating in 3-bit per cell mode (TLC), though it may also be operated in a one-third capacity mode with one data bit per cell (SLC) for enhanced retention and endurance [16]. For this testing, all operation was in the lower-capacity single-level cell mode as it traditionally presents a more appealing combination of reliability and lifetime for typical space missions.

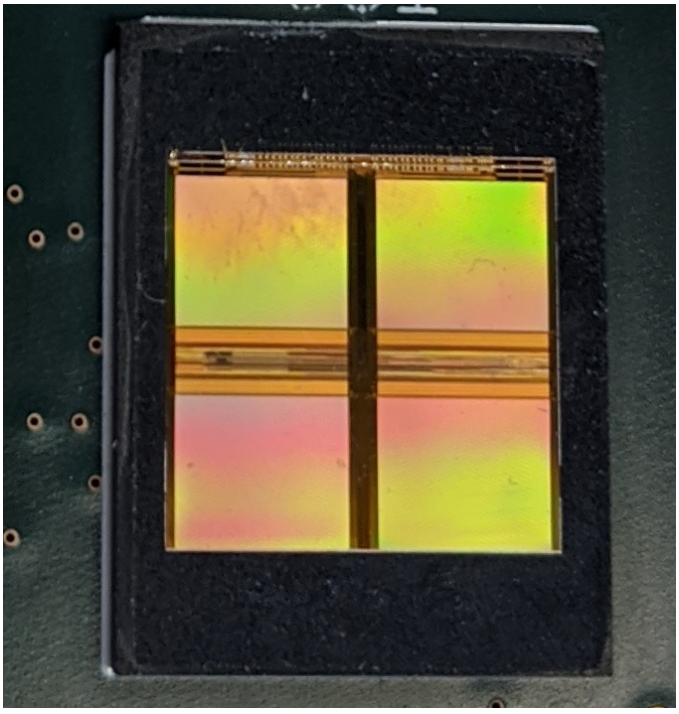

Fig. 1. Decapsulated eight-die H25QFT8F4A9R-BDF mounted on test board.

Devices were prepared for testing by chemical/laser decapsulation to remove the plastic packaging material, as shown in Fig. 1. Decapsulation is necessary for ground-based heavy-ion testing with particles that typically do not have the range of higher energy particles in a natural space environment. It is not typically required for proton testing; however, for low-energy proton testing the particle ranges are extremely limited and the bare silicon die must be exposed.

A scanning electron microscope (SEM) cross-section of a highly similar part (Hynix 72 layer TLC NAND, but 256 Gb

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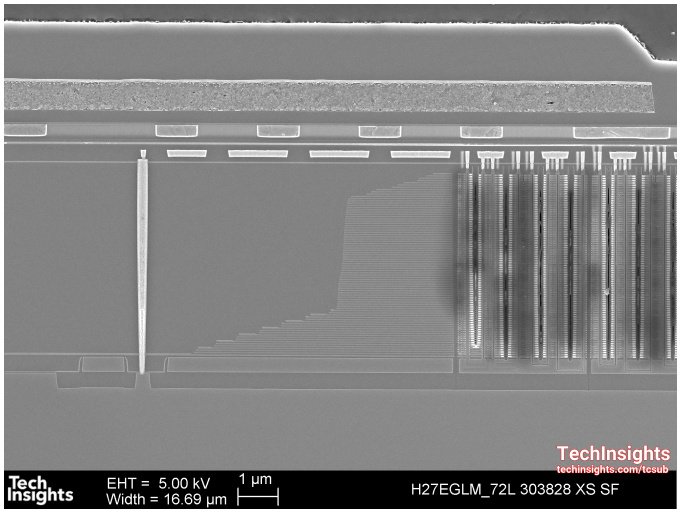

Fig. 2. SEM Cross-section in bit line direction showing device from top of die to bottom of memory stack (used with permission, courtesy of TechInsights).

per die capacity) is shown in Fig. 2; the 72-layer memory structure is visible on the right side, and the passivation and packaging layers are shown at the top.

B. Test Setup

The flash memory was powered with an external Keithley 2230-30-1 power supply during erase, program, and readback operations. Data and control signals were generated by a custom-built test board that includes an ARM Cortex-M4 microcontroller (MCU) running up to 240 MHz and providing effective test data rates to a host PC of about 10 MB/s.

III. Heavy Ion Testing

Heavy-ion testing was conducted at the Lawrence Berkeley National Laboratory's (LBNL) 88" Cyclotron facility. Most testing was performed at normal incidence, but certain angular irradiations with multiple axes of rotation were performed to evaluate three-dimensional angular dependencies. The test setup at the facility is pictured in Fig. 3, and the specific ion beams used are listed in Table I, with surface linear energy transfer (LET) and ranges independently computed with SRIM 2013 [17].

Heavy-ion testing for single-event upsets (SEU) was performed with static, unpowered irradiations to remove any secondary effects caused by control circuitry or page buffer upsets and limit data errors to true bit cell upsets in the memory array. Each run was typically performed to a fluence of $1x10^6$/cm^2 with a flux between $2x10^4$/cm^2/s and $9x10^4$/cm^2/s. Sixteen blocks each of four data patterns (all zeros, all ones, checkerboard, and pseudorandom), totaling about 85 MB per pattern, were programmed and read back prior to each irradiation. Errors existing prior to the run (common with any advanced flash memory) were masked for analysis. Testing was performed in vacuum at room temperature, and the heavy-ion SEU cross-section is shown in log-log format in Fig. 4.

The trend of SEUs plotted in Fig. 4 shows a roughly power-law relationship between SEU cross-section and LET down

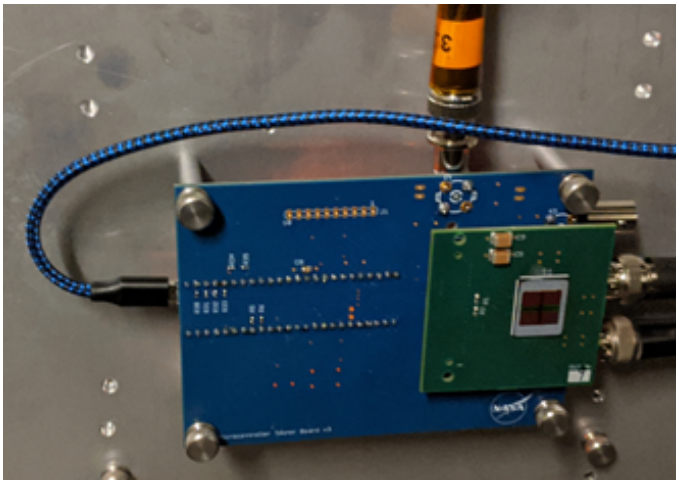

Fig. 3. Flash memory mounted to motherboard in LBNL test chamber prior to heavy ion irradiation.

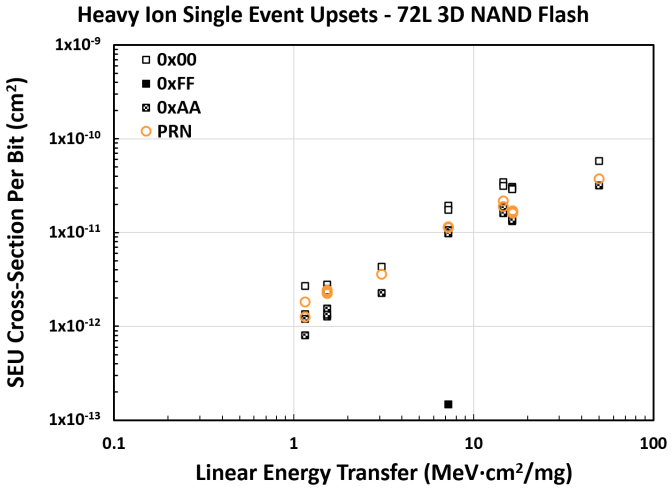

Fig. 4. SEU cross-section from heavy-ion irradiation, unpowered, in SLC mode.

to the lowest LET tested (1.2 MeV· cm^2/mg). Based on this trend, it is hypothesized that low-energy protons (peak LET 0.5 MeV· cm^2/mg) [6] could directly upset the flash cells. No error-free LET threshold could be identified with the heavy ion beams available.

A data pattern dependence is observed in the heavy ion data, with fully erased cells (all ones pattern) essentially impossible to upset, all zero pattern most susceptible, and mixed data patterns somewhere in between. Such a relationship suggests

TABLE I
Beam List for Heavy Ion Irradiation

Ion Species	Energy (MeV)	Surface LET (MeV· cm^2/mg)	Range in Si (μm)
N	233.7	1.16	505.7
O	277.3	1.54	462.4
Ar	642.4	7.27	255.6
Cu	1007	16.5	190.3
Kr	1225	25.0	165.5

Facility configured for 16 MeV/amu tune, in vacuum.

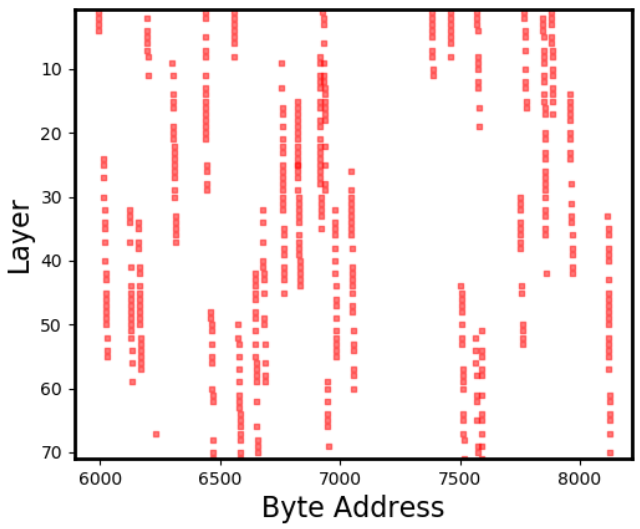

Fig. 5. Heavy ion SEU data processed to show ion tracks created by 1225 MeV Kr ions passing through the physical memory structure.

a direct mapping of logical bit value to physical cell program state, and has been shown in previous NAND flash memories, including from the same manufacturer in [11].

The relationship between logical address and physical memory layer was experimentally determined using heavy ion bit upset tracks as a reference, as shown in Fig. 5 and previously demonstrated in [18]. Each NAND string within the array is 144 bits long, with a U-shaped tunnel at the base of the structure. The heavy ion SEU data are processed first by grouping the word lines in sets of 144 and then reversing lines 72-143 such that line 0 and 143 both represent the top-most physical layer and lines 71 and 72 are the bottom-most. As an example, 1225 MeV Kr ions created the vertical stripes in Fig. 5 when normally-incident ions upset a series of cells in the same address but across multiple layers. The same technique will later be used with the proton data.

IV. Low-Energy Proton Testing

A. Proton Facility

Low-energy proton testing was performed at the NASA Goddard Space Flight Center's (GSFC) Radiation Effects Facility (REF), using a 2 MeV Van de Graaff accelerator. The REF personnel constructed an aluminum masking plate (Fig. 6) to protect the test board from possible electrical charging effects in the beamline. All proton tests were performed with the device powered off during irradiation. The proton fluence for most operational runs was 10^8/cm^2 over 100 seconds, though irradiation to a lower fluence, 10^7/cm^2, was used to evaluate any variation in error cross-section as a function of fluence. Depending on the energy of the beam, a total ionizing dose of between 281 and 409 rad(Si) was delivered per run, with a cumulative dose of 7.22 krad(Si) on the irradiated sample. As in the heavy ion testing, the memory was erased between runs, verified, programmed, and then pre-rad errors were saved as a mask.

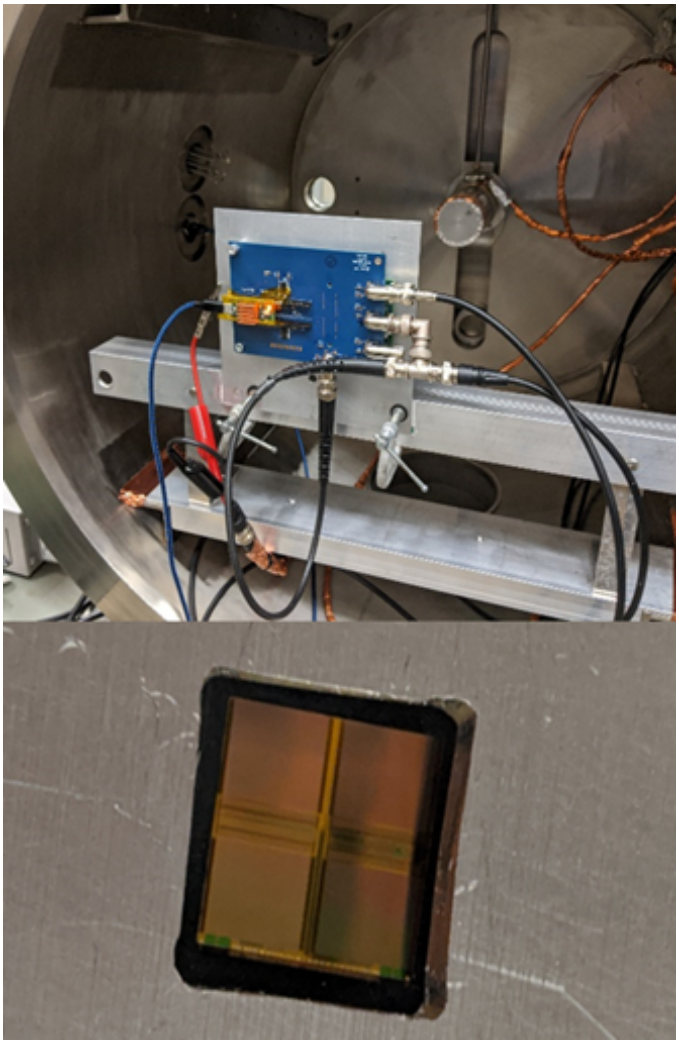

Fig. 6. Reverse view of test board mounted in accelerator for proton testing (top), with closeup of aluminum masking plate on front of PCB (bottom).

The energy width of the beam is specified by the facility to within $\pm 2\%$ at the DUT, and the energy level is calibrated with a solid state detector against a known source. The Faraday cup current used to compute flux is measured with an electrometer verified with a calibrated current source to within 10% agreement for each test.

B. SRIM Simulations

SRIM simulations of the penetration of a proton through a uniform silicon target are presented in Fig. 7, plotted as if particles of different initial energies are encountering the silicon target from the left (depth 0 μm) and slowing as they move deeper into the material. The vertical axis is LET at each depth in the material, and separate curves cover initial proton energies between 500 keV and 1200 keV to illustrate the progression of the Bragg peak deeper into the material as the accelerator tune is increased. For comparison of physical scale, a cross-section of the 72 layer flash memory is shown in Fig. 8. The entire 72-layer stack is approximately 4.5 μm deep. From this information, it was hypothesized that movement of

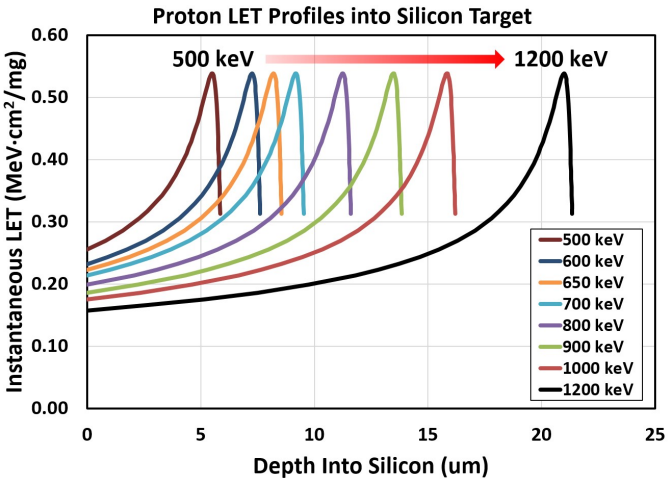

Fig. 7. Simulation of proton LET vs depth in a uniform silicon material for energies used in test.

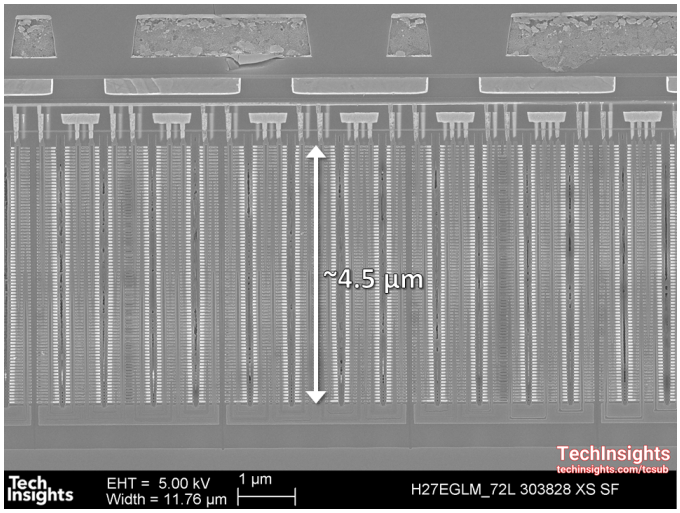

Fig. 8. Close up SEM of the memory array (used with permission, courtesy of TechInsights).

the Bragg peak through the material might be visible with this 3D memory technology.

C. Proton Testing

A single decapsulated device, selected from parts left over from heavy ion testing (but not itself previously irradiated) was tested using the same hardware and software as heavy ion testing. A larger memory area was exercised, with 45 blocks per pattern (≈255 MB per pattern) under test. Like the heavy-ion data presented previously, the device was operated in SLC configuration.

The SEU cross-section from proton irradiation (Fig. 9) reveals a clear dependence on proton energy for all data patterns tested as expected. The characteristic peaking of direct ionization [7] is present at an energy of approximately 700 keV; errors tail off rapidly as energy decreases because the beam is no longer able to penetrate the memory stack. At higher energies, the range is no longer a limiting factor, but

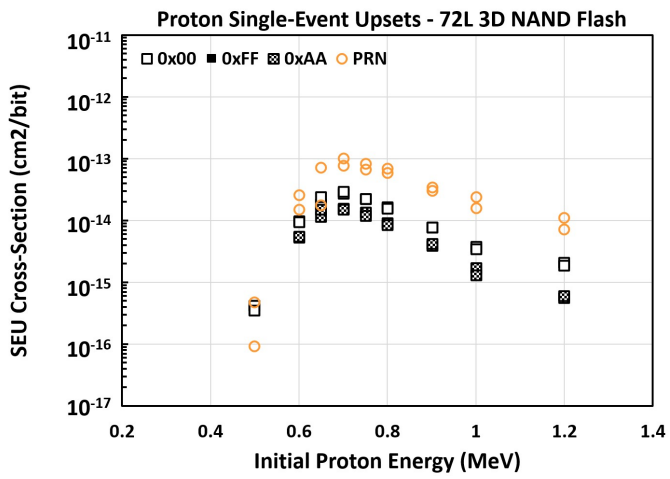

Fig. 9. SEU cross-section vs. initial proton energy.

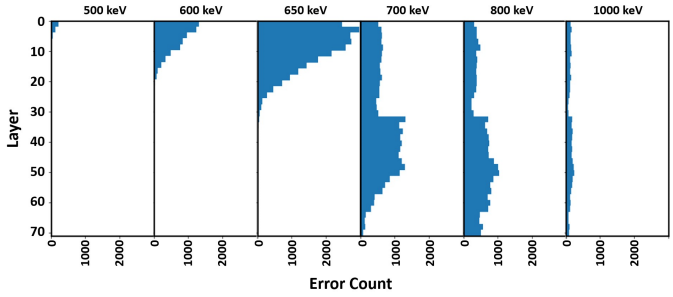

Fig. 10. Histograms of errors in by layer as proton energy increases from 500 keV (left) to 1000 keV (right)

the increased energy of each particle results in a lower LET (Fig. 7), reducing upset counts. Eventually as proton energy increases further, indirect ionization resulting from nuclear interactions should become the dominant source of proton-induced SEU [13].

Analysis of the proton SEU data within the three-dimensional volume confirms movement of the Bragg peak from surface of the die to the base of the memory stack as predicted. Proton upsets were sorted by physical layer (0-71) in the same manner previously described for heavy ions, then plotted in a series of histograms; selected energies are shown in Fig. 10 to illustrate movement of the Bragg peak. The vertical axis of Fig. 10 is the physical depth in the material, while the horizontal axis is the count of errors at each grouping. For the lowest energy tested (500 keV, Fig. 10, left) only a small number of errors are created at the top-most memory layer. By increasing to 650 keV, a distribution of errors over the 30 upper-most layers appears. At 1000 keV and beyond (Fig. 10, right), few errors are created due to reduced LET, but they are more uniform through the memory as LET is more constant throughout the material (Fig. 7).

Statistical evaluation indicates that the number of cells expected to receive multiple proton strikes at these fluences is insignificant and does not account for a significant portion of the proton-induced upsets. Fig. 11 shows a mathematical expectation of the number of cells receiving a single hit versus

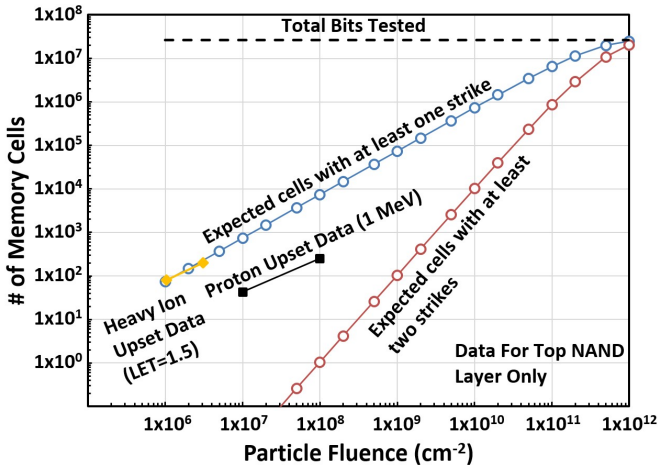

Fig. 11. Expected number of cells with single and multiple particle strikes for given fluences, overlaid with heavy ion and proton data.

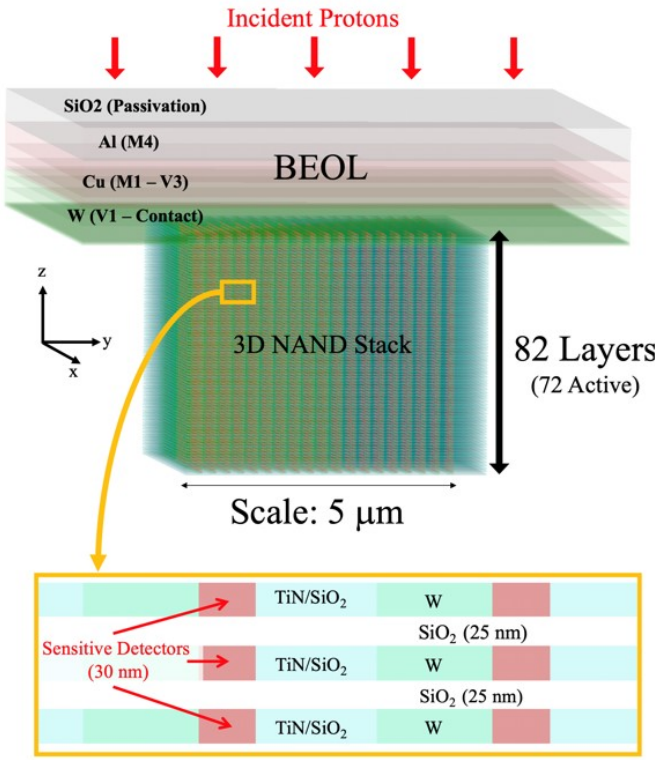

Fig. 12. MRED simulation structure for 72-layer 3D NAND. The total BEOL thickness is approximately 3.5 μm, and the NAND stack is just over 4.5 μm thick. The NAND stack consists of alternating layers of SiO_2 and a more detailed layer (as shown in the bottom part of the figure) composed of TiN, SiO_2, and W. Each sensitive detector is defined by an SiO_2 region 30 nm thick and 50 nm in both transverse directions.

two or more hits for a given fluence based on a bins and balls problem approach. The single-hit curve is calibrated to overlay the heavy ion data taken at low LET. The proton data have the expected 1 decade per decade slope of the single-hit line and are several orders of magnitude higher in occurrence than the estimated double-hit data.

To further explore the layer-by-layer error distribution, including the apparent discontinuity of data between 650 keV and 700 keV (Fig. 10), a Monte Carlo simulation approach is employed as described below.

V. Monte Carlo Simulation Details

Monte Carlo Radiative Energy Deposition (MRED) is a radiation transport tool developed at Vanderbilt University to study radiation effects in semiconductor devices [19], [20]. MRED is built using primarily the simulation libraries of Geant4 [21], with added functionality included to account for screened Coulomb scattering (particularly important for proton irradiation) [22] and other custom physics modules.

Using SEM images of the 3D NAND device as a guideline, the simulation model is constructed as shown in Fig. 12.

The back-end-of-line (BEOL) is defined with thicknesses and materials also taken from the SEM images of the device. It takes up the entire 10 μm x 10 μm simulation world size (in the x- and y- dimensions), with the memory array below defined within the center 5 μm x 5 μm region; the material outside this center area is set to SiO_2 (transparent in the figure).

Immediately below the BEOL are three layers of tungsten which are 25 nm thick. These represent the three layers of control gates which sit on top of the memory array. The memory stack itself then contains 79 more layers, each consisting of a transistor layer, followed by a 25 nm layer of SiO_2. Each transistor layer contains a repeated pattern of 3 regions tiled across the array. These material regions are W, TiN, and SiO_2, of (x, y) dimensions (5 μm, 100 nm), (5 μm, 55 nm), and (5 μm, 100 nm) respectively. Four dummy layers are included at the top of the stack, and two more dummy layers are defined at layer number 40. The only difference between the dummy layers and the standard transistor layers is the lack of sensitive detectors in the dummy layers (i.e. no energy deposition is tracked).

Sensitive detectors are set as SiO_2 regions 30 nm thick and 50 nm in the x- and y-directions, tiled uniformly throughout each transistor layer in the TiN region adjacent to the tungsten word-line. This approximately corresponds to the physical size of the transistors in the memory array. Each sensitive region has a unique sensitive detector attached so that multiple-bit upsets do not artificially increase the cross section for a single bit.

The material composition of the transistors is in reality more complex than simply SiO_2, with each transistor containing silicon nitrides, silicon and aluminum oxides, as well as the polysilicon channel. However, each new physical boundary in MRED forces a stepping action for tracks which traverse the region, and as each of the 72 vertical layers in the simulation already contains 361 sensitive detectors, including these extra boundaries would significantly increase the computation time required while providing very little if any difference in terms of the overall energy deposition profile as a function of depth in the stack. The key assumptions made in this model are thus that the densities of the transistor materials are sufficiently similar to that of SiO_2 to allow for full material substitution, that the BEOL may be approximated as full metal layers, and that upsets are caused by charge deposition events which occur in the immediate physical vicinity of the transistors which

make up the memory array.

By integrating the event weights over the energy deposition bins of the histogram from high to low energy and normalizing to the simulated fluence, one obtains a cross section (in units of cm^2). The cross section taken at a specific energy, E_{crit}, corresponds to the relative probability that a single event will deposit E_{dep} within the volume such that $E_{dep} \geq E_{crit}$, where E_{crit} is the energy required to induce an upset. If the path length l of an ion is small compared to its range, the LET can be approximated as a constant value and the critical energy calculated by (1):

$$E_{crit} \approx LET \times \rho \times l \tag{1}$$

To approximate E_{crit} of this device, it is thus appropriate to use the LET values from the heavy ion experiments rather than LETs from the short-ranged low energy protons which may stop within the device. Using the smallest LET value from the heavy ion testing (1.16 MeV$\cdot$ cm^2 / mg), and taking the thickness of each transistor to be 30 nm (from SEM images), E_{crit} for this device is approximated as 9.2 keV (or critical charge $Q_{crit} \approx 0.41$ fC).

Simulations were completed at proton energies of 500 keV, 600 keV, 650 keV, 700 keV, 800 keV, and 1 MeV, with the ion beam randomized over the top surface of the structure (shown in Fig. 12) in a unidirectional flux. The total number of ions sampled in each run is at least 14 million, which corresponds to a total fluence of at least 10^{13}/cm^2.

VI. Simulation Results

Fig. 13 summarizes the results of the simulations described above. The cross section, which represents the relative probability of generating sufficient charge to induce an upset at a node in the memory array, is given as a function of the proton energy and depth in the stack. There are two notable differences between simulation and experiment: the lack of events at 700 keV below layer 40 in the simulated results, and the presence of a step-like feature between layers 30 and 40 for proton energies greater than 650 keV in the experimental results. While these two features are not necessarily connected, further research is required as the range of protons at 700 keV should in theory not result in direct ionization in the deeper cells of the memory array. Error may also be introduced in the simulated results by any combination of the approximations used, such as defining the BEOL using full layers of just metal (not including oxide), the simplified geometry and materials of the transistor layers, or the presence of alternative material structures or dimensions in the dummy memory layers.

Not only are the general shapes in the depth profile consistent with the experimental results, but the average cross section values over the entire memory array (Fig. 14) are also on the same order of magnitude as those observed from experimental proton testing (Fig. 9) and peak in the same energy range.

In this model, the transistor area is approximated as pure SiO_2 while the actual transistors have other materials as mentioned above. Using the densities of SiO_2 and pure silicon to bound the range of material densities present in the physical transistor structure, there is strong agreement with the range of cross section values recorded from experiment.

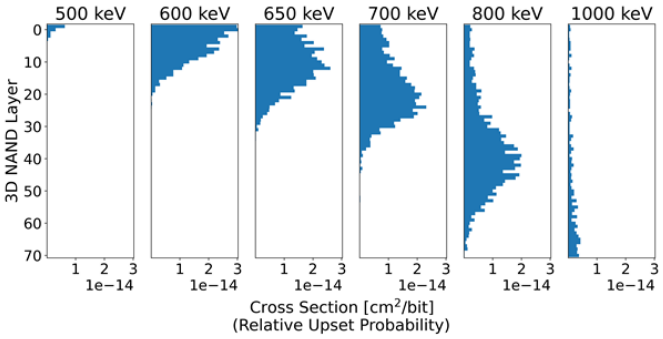

Fig. 13. Depth profile of simulated proton-induced upsets in 3D NAND memory array.

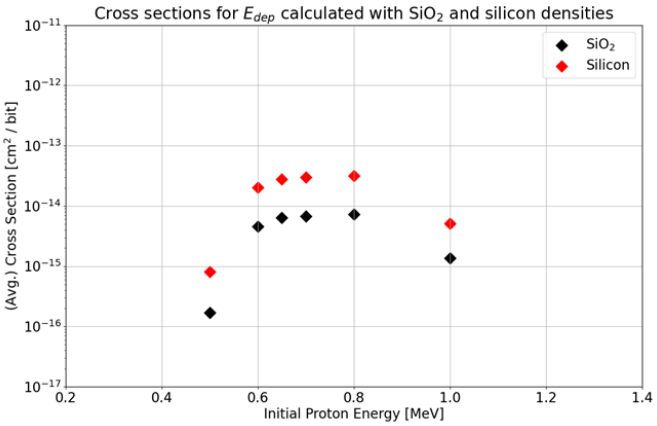

Fig. 14. Simulated cross sections as a function of initial proton energy, averaged over all layers for $E_{dep} \geq E_{crit}$. Data is shown for E_{crit} as calculated in (1) using silicon and SiO_2 densities.

VII. Conclusions

Experimental evidence of direct ionization in a 72-layer 3D NAND flash memory operating in SLC mode has been obtained through a combination of heavy-ion and low-energy proton irradiation and verified with Monte Carlo simulation. The overall error cross section curves show a clear peaking at approximately 700 keV both in experimental and simulation data, which is consistent with direct ionization caused by low-energy protons. Three-dimensional analysis of the error data shows the progression of the error peak from the surface (at 500 keV), to the middle of the memory stack (700 keV), and beyond (1000 keV), which is consistent with expectations from the SRIM-derived LET curves and the device cross-sectional measurements. However, the abrupt variation of the experimental proton error distribution in deeper layers of the memory array leaves questions not yet resolved by Monte Carlo simulation.

Ultimately the proton-induced error cross sections of this device are relatively low for a device technology that requires error-correcting code (ECC) for normal, terrestrial operations. However, as 3D NAND technology continues to mature and scale at a rapid pace both in physical (layer count, bit size) and logical (bits per cell) dimensions, the susceptibility to even lower LET particles will continue to increase. Prudent design of error detection and correction (EDAC) systems for high-

reliability applications like space flight may require knowledge of the susceptibility to both heavy ions and traditionally untested particles like low-energy protons or electrons, as well as the non-uniform distribution of errors in large 3D devices. Operational decisions driven by specific r adiation environments (e.g. the South Atlantic Anomaly or a lengthy transit through the Van Allen belts) may assume that a powered-down condition is safest. Indeed, a non-volatile memory with low SEU LET threshold will continue to accumulate upsets when powered down, but without a functioning EDAC mechanism to detect and scrub errors. The number and distribution of errors expected on power-up then becomes worth consideration during trade studies of a mission's operational plan.

VIII. Acknowledgments

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