National Aeronautics and Space Administration



# Supplementary Digest on Performance of COTS EEE Parts Under Extreme Temperatures

# NASA Electronic Parts and Packaging (NEPP) Program Office of Safety and Mission Assurance

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#### Scope

As stated in the first published digest [1], the NASA Glenn Research Center (GRC) has been performing reliability studies and performance evaluation of commercial-off-the-shelf (COTS) Electrical, Electronics, and Electro-mechanical (EEE) parts under typical harsh space environmental conditions, in particular extreme temperature exposure and wide-range thermal cycling. These efforts spanned several years under the support of the NASA Electronic Parts and Packaging (NEPP) Program. In some instances, the studies were executed in collaboration with other NASA Centers, including Goddard Space Flight Center (GSFC), Langley Research Center (LaRC), Marshall Space Flight Center (MSFC), and Jet Propulsion Laboratory (JPL). Test articles included devices such as operational amplifiers, semiconductor power switches, capacitors, oscillators, voltage references, flexible printed circuit boards, sensors, and DC/DC converters. This digest provides a synopsis on test results obtained on selected parts, but more detailed findings specific to these and other COTS parts are posted on the NASA NEPP website [1].

Experimental investigations focused mainly on determining performance of COTS electronic parts upon exposure to both high and low temperatures (occasionally beyond their specified limits), thermal cycling, and re-start capability at temperature extremes; however, functionality determination of NASA-developed parts, assembled circuits, and materials were also covered. The tested devices were based on various semiconductor technologies that include silicon (Si), silicon germanium (SiGe), and silicon-on-insulator (SOI). Test findings of germanium (Ge), gallium nitride (GaN), and silicon carbide (SiC) technology-based devices will be reported in a future document.

The objective of this task is to establish a baseline on the functionality and to determine suitability of the devices/circuits for use in space exploration missions. The findings are then disseminated to mission planners and circuit designers so that proper selection of electronic parts can be made, and risk assessment and mitigation techniques are established to use such devices in space missions. It should be noted that the findings reported here are based purely on in-house experimental work, and the results, therefore, should not be construed as NASA endorsement of any or all of these products but rather used as a guide to aid in the proper selection of parts for use in specific applications. In addition, tests performed were not comprehensive and the thermal cycling activities were limited due to time constraints. The results rather serve as a down-select process for parts with potential for use in space environment and, thus, further screening and qualification per NASA, military, and/or industry standards need to be followed prior to deeming them appropriate for space use.

## Si Technology

Voltage Reference ADR3430

A micropower, high accuracy voltage reference, Analog Devices ADR3430 chip [2], was evaluated under a wide temperature range and thermal cycling to determine its functionality at temperatures beyond its specified operating limits. The low temperature test was restricted to -100°C because the output began to exhibit instability at that point, while the upper test temperature was confined to +140°C, a value that exceeded the part's high temperature operating limit but fell short of the absolute maximum junction/storage rated temperature of +150°C. The output voltage at no load is shown in Figure 1 as a function of applied input voltage for various test temperatures. The voltage reference was able to produce a stable, steady 3.000 V output regardless of the magnitude of the input voltage except at the cryogenic temperature of -100°C where the output slightly increased to 3.007 V. This impact of subjecting the voltage reference to -100°C on its output level is further illustrated in Figure 2.



Variation in the output voltage of the ADR3430 reference device using an input voltage of 3.5 V as a function of load current at various test temperatures is depicted in Figure 3. The reference voltage displayed superb performance in terms of load regulation at any temperature in the test range from -70°C to 140°C. Such was not the case though at the test temperature of -100°C where the output voltage dropped when either a low input voltage of 3.2 V or a higher input level of 5.0 V was used particularly under heavy load, as illustrated in Figure 4.



#### Voltage Reference REF5025-HT

Texas Instruments' REF5025-HT chip, a low noise, very low drift, precision voltage reference [3] was evaluated under a wide temperature range and thermal cycling between -190 °C and +210 °C. Figure 5 shows its no-load output voltage as a function of applied input voltage for various test temperatures. The output voltage of the regulator maintained a steady value of about 2.5 V at any test temperature in the range between -50 °C and +200 °C. Outside this temperature envelope, however, the output voltage exhibited a decline in its value that was dependent on the test temperature. That is, while the output voltage dropped slightly at the extreme temperatures of -190°C (2.32 V) and +210°C (2.43 V), it experienced more decrease in the intermediate test temperatures of -100°C and -150°C where output levels of 2.03 V and 1.90 V were obtained, respectively.

The variation in the output voltage of the REF5025-HT voltage reference device as a function of load current at the various test temperatures is depicted in Figure 6. The voltage reference exhibited good load regulation in the temperature range of  $-50^{\circ}$ C to  $+200^{\circ}$ C as its output did not change significantly from the nominal value of about 2.51 V. At the extreme test temperatures of  $-100^{\circ}$ C and  $+210^{\circ}$ C, however, the device experienced some changes in its output. At 210°C, for example, the output voltage ranged from 2.44 V to 2.40 V for all load levels except at 10 mA where it appreciably dropped to about 0.2 V. When the voltage reference was exposed to the cryogenic test temperature of  $-100^{\circ}$ C, its output held a steady value of 2.03 V while the device was not loaded or while it was sinking current of -5 or -7 mA. Under source-current conditions, though, the output switched to the normal 2.51 V level under loads of 5 or 10 mA but collapsed back to 2.03 V under a 7 mA load, as shown in Figure 6. Although it might be thought that the internal heat generated by the device when loaded tends, in general, to lessen the impact of the cold temperature on its operation, the peculiar behavior at 7 mA condition is not fully understood, or could have been due to some experimental error.



The semiconductor chip was able to restart at  $-190^{\circ}$ C and at  $+210^{\circ}$ C, and thermal cycling did not influence its characteristics and had no impact on its packaging. Pre- and post-cycling reference output voltage levels are shown in Figures 7 and 8, respectively.



#### Half-bridge Driver LM5113

The operation of a half-bridge LM5113 driver, designed to drive enhancement-mode GaN FETs (Field effect transistor) in a synchronous buck or a half bridge configuration [4], was characterized in terms of its high-side gate drive output (HO), low-side gate drive output (LO), outputs rise time, fall time, and turn-on delay time at specific test temperatures. The propagation delay times included  $t_{LPLH}$  (LI Rising to LO Rising) and  $t_{HPLH}$  (HI Rising to HO Rising). The rise and fall times of the driver output signals as well as the supply current were also recorded. Its operational characteristics were recorded over the test temperature range of -194°C to +150°C at a switching frequency of 200 kHz.

Waveforms of the LM5113 low-side driver (LO) and the high-side driver (HO) output signals along with the input signals for the low-side (LI) and high-side (HI) drives recorded at various temperatures are shown in Figure 9-11. The driver maintained proper operation and no major change was observed in the shape or magnitude of these waveforms as test temperature was changed throughout the range of  $-194^{\circ}C$  to  $+150^{\circ}C$ .



Figure 9. HI (trace 1), HO (trace 2), LI (trace 3), and LO (trace 4) signals at +23°C. (Scale: Vertical 5V/div; Horizontal 2µs/div, for all signals)



Figure 10. HI (trace 1), HO (trace 2), LI (trace 3), and LO (trace 4) signals at -194°C.



Figure 11. HI (trace 1), HO (trace 2), LI (trace 3), and LO (trace 4) signals at +150°C.

Figure 12 shows that both the turn-on propagation delay time  $t_{LPLH}$  for the low-side drive (LI rising to LO rising) and the turn-on propagation delay time  $t_{HPLH}$  for the high-side drive (HI rising to HO rising) of the half-bridge driver were comparable and exhibited gradual but slight increase as the test conditions varied from cryogenic to the high temperature end.



Figure 12. Turn-on propagation delay times, tLPLH and tHPLH, as a function of temperature.

The rise and fall time times of the output signal of the low-side driver are shown in Figure 13 as a function of temperature. Little effect of temperature was found on these

characteristics of the driver as their values held almost a steady value throughout the test temperature range. Similar behavior was observed for these properties of the other drive, i.e. high side, as shown in Figure 14.



Limited thermal cycling did not induce much change in the behavior of this half-bridge driver integrated circuit chip as depicted by the data in Table I.

	Delay Time		Delay Time		LO Signal		HO Signal		Input Current	
	t <sub>LPLH</sub>	(ns)	t <sub>HPLF</sub>	t <sub>HPLH</sub> (ns)		t <sub>f</sub> (ns)	t <sub>r</sub> (ns)	t <sub>f</sub> (ns)	(mA)	
Temp (°C)	Prior	Post	Prior	Post	Prior	Post	Prior	Post	Prior	Post
+23	33	34	35	36	2.67	2.89	2.86	2.81	0.72	0.73
-194	21	20	22	22	2.40	2.83	2.59	2.63	0.50	0.50
+150	47	47	48	48	2.61	3.08	2.76	2.72	0.76	0.76

Table I. Pre- & post-cycling propagation delays, switching times, & input current.

## Si Oscillators

Silicon oscillators, including those built using MEMS (Micro-Electro-Mechanical Systems) technology, are widely replacing ceramic and quartz counterparts as they offer a wide frequency range operation, exhibit great tolerance to shock and vibration, and are immune to electro-static discharge. These attributes make them ideal candidates for use in space exploration missions. Performance of Si oscillators from five manufacturers [5]-[9] were evaluated for extreme temperature exposure, restart-capability at extreme temperatures, and thermal cycling. Characterization of each oscillator was obtained in terms of output frequency, duty cycle, rise and fall times, and supply current at specific test temperatures.

All five oscillators exhibited good and stable operation in a temperature range that exceeded their individual specified region. The temperature range for which stability was maintained differed from one device to another. While some displayed excellent stability throughout the whole test temperature range, the operation of others became unsteady at certain temperature test points, reflected by fluctuation in the output frequency or distortion of the output waveform. Such temperature-induced changes were not permanent, as the affected oscillators completely recovered upon removal of the thermal stress. The temperature range through which stable

operation was maintained for these devices is shown in Figure 15. It should also be noted that all oscillators were able to restart at the extreme test temperatures and to withstand the limited thermal cycling without undergoing any significant changes in their characteristics, as shown in Table II.



Figure 15. Temperature range of stable operation of the tested silicon oscillators.

Dovico	T(°C)	Cycling	f (MH7)	Duty cycle	Trise	T <sub>fall</sub>	Is
Device	1(0)	Cyching	I (IVIIIZ)	(%)	(ns)	(ns)	(mA)
	22	pre	99.990	50.12	50	51	0.054
90		post	99.981	50.11	49	51	0.054
)69	55	pre	103.964	50.15	47	49	0.058
IČ	-33	post	103.639	50.13	47	50	0.058
Ľ	+140	pre	99.485	50.17	56	59	0.049
	+140	post	99.473	50.18	55	58	0.049
	22	pre	1.8432	49.94	49.94	12.4	10.9
	22	post	1.8432	49.94	49.94	12.0	10.4
E N	100	pre	1.8469	49.92	49.92	11.7	10.5
SFJ	-190	post	1.8467	49.93	49.93	11.4	10.1
A	+140	pre	1.8425	49.94	49.94	13.6	11.4
	+140	post	1.8426	49.94	49.94	13.5	11.2
	22	pre	1.00002	50.04	3.0	2.8	11.40
-	ZZ	post	1.00000	50.04	2.9	2.8	11.29
K2	-112	pre	0.99987	50.02	2.7	2.6	10.63
M		post	0.99987	50.02	2.6	2.5	10.56
	+110	pre	1.00001	50.05	3.2	3.1	11.65
		post	1.00001	50.05	3.1	3.0	11.63
	21	pre	10.0413	44.09	6.77	5.31	2.18
00	21	post	10.0290	44.03	6.86	5.36	2.20
,11	105	pre	5.1197	48.62	12.56	9.09	1.01
Ç	-195	post	5.1159	48.67	12.67	9.19	1.03
LS	+120	pre	10.0322	42.80	8.78	6.96	2.29
	+130	post	10.0312	42.80	8.66	6.84	2.28
	21	pre	1.00000	50.03	1.8	1.8	11.15
AI	21	post	1.00001	50.03	2.0	2.1	11.20
00	110	pre	0.99988	50.02	1.7	1.6	10.32
<b>Г11</b>	-110	post	0.99992	50.02	1.8	1.8	10.40
Si	+100	pre	0.99998	50.04	1.9	1.9	11.19
	+100	post	0.99998	50.04	1.8	1.8	11.21

Table II. Pre- and post-cycling characteristics of the silicon oscillators.

## Si Optocouplers/Isolators

The effects of extreme temperature exposure and thermal cycling on the performance of a COTS optocoupler, Fairchild FOD3150 [10], were evaluated in the range of  $-190^{\circ}$ C to  $+110^{\circ}$ C. The device was found to operate properly without any major changes in its characteristics in the temperature range from about  $-100^{\circ}$ C to  $+110^{\circ}$ C, well beyond its specified range of  $-40^{\circ}$ C to  $+100^{\circ}$ C. At temperatures below  $-100^{\circ}$ C, however, the device maintained operation but exhibited a marked increase in its output's duty cycle and a significant increase in its high-to-low transition

time,  $t_{PHL}$  as temperature decreased. At -190°C, for example, the duty cycle reached about 73% as compared to the steady 50 % level held between -100°C and +110°C.

Waveforms of the input and the output signal for the FOD3150 optocoupler at  $23^{\circ}$ C,  $-190^{\circ}$ C, and  $+110^{\circ}$ C are shown in Figure 16, and temperature-induced variation in its parameters are shown in Figure 17.



Figure 16. Optocoupler input (blue) and output (red) signals at 23 (left), -190 (middle), & +110 °C (right).



Figure 17. Duty cycle, rise & fall time, propagation delays, and current versus temperature.

Thermal cycling introduced mild changes in the operational characteristics of the optopcoupler, as shown in Table III.

<b>T</b> (° <b>C</b> )	I <sub>s</sub> (mA)		tr (ns)		t <sub>f</sub> (ns)		τplh (ns)		τ <sub>PHL</sub> (ns)	
	Prior	Post	Prior	Post	Prior	Post	Prior	Post	Prior	Post
-190	3.69	4.15	77	57	68	57	291	375	23605	15327
+23	5.15	5.22	86	70	74	63	240	361	289	237
+110	4.82	4.94	94	81	80	70	306	312	328	265

Table III. Pre- and post-cycling data at selected temperatures.

Similar work was carried out on a Giant Magneto-Restrictive (GMR) digital isolator IL510, a potential replacement for traditional means used for isolation such as optocouplers or inductive and capacitive coupling. These GMR isolators, which work on the principle of large variation in the electrical resistance of ferromagnetic and non-magnetic thin-film materials with applied magnetic fields, produce rather large output signal resulting in improved sensitivity and higher accuracy. In addition, this technology is compatible with semiconductor integrated circuit manufacturing and, thus, it can be easily incorporated into system-on-chip packages [11]-[12].

The device performed very well throughout the test temperature between -190 °C and +120 °C, a range that extends beyond its specified regime, as no significant changes occurred either in its function or in its output signal timing characteristics. Waveforms of the input and the output signal for this digital isolator at 23 °C, -190 °C, and +120 °C are shown in Figure 18, and temperature-induced variation in its parameters are shown in Figure 19.



Figure 18. Isolator input (red) and output (blue) signals at 23 (left), -190 (middle), & +120 °C (right).



Figure 19. Duty cycle, rise & fall time, propagation delays, and current versus temperature.

Similarly, thermal cycling did not any noticeable changes in the operational characteristics of the digital isolator, as shown in Table IV.

							1			
T (°C)	I <sub>s</sub> (mA)		t <sub>r</sub> (ns)		t <sub>f</sub> (ns)		$ au_{PLH}$ (ns)		$\tau_{\rm PHL}$ (ns)	
	Prior	Post	Prior	Post	Prior	Post	Prior	Post	Prior	Post
-190	1.95	1.95	12.7	12.9	12.6	12.6	18.1	17.7	24.0	24.9
+23	1.67	1.67	14.4	14.4	13.2	13.4	20.4	20.1	26.5	27.4
+120	1.56	1.56	15.7	15.5	15.0	14.4	22.4	22.5	28.8	29.1

Table IV. Pre- and post-cycling data at selected temperatures.

### Diodes

Automotive-grade, fast switching diodes 1N4448WSF diodes, qualified to AEC-Q101 (Automotive Electronics Council) standards for high reliability [13] were examined in terms of their forward and reverse voltage-current (V/I) characteristics over a wide temperature range between -192 °C and +150 °C. This was a collaborative effort with the U.S. Naval Surface Warfare Center and NASA MSFC.

The forward V/I characteristics of the 1N4448 diode at various test temperatures are shown in Figure 20. Although the diode maintained operation throughout the test temperature range, its forward voltage, increased with a decrease in temperature. For

example, while the forward voltage had a value of about 0.7 V at room temperature, it increased to slightly over 1 V at the extreme cryogenic temperature of -192°C. At the other extreme temperature, i.e. +150°C, the trend is reversed as the voltage drop decreased to about 0.5 V



Figure 20. Forward V/I characteristics of 1N4148 diode versus temperature.

The diode seemed to maintain low reverse current over the temperature range of  $-192^{\circ}$ C to  $+50^{\circ}$ C. At higher temperatures, however, it exhibited significant increase with temperature, notably at  $+150^{\circ}$ C, as shown in Figure 21. In addition, the onset of the breakdown voltage in the reverse operation mode seemed to vary with temperature. At all test temperatures, the onset of breakdown voltage occurred at lower values when compared to its room temperature level. These changes were more dramatic at the test temperatures of -192, +100, and  $+150^{\circ}$ C, as shown in Figure 21.



Figure 21. Reverse V/I characteristics of 1N4148 diode versus temperature.





Figure 22. Pre-(left) and post-cycle(right) forward and reverse diode's V/I characteristics.

## SiGe Technology

#### Oscillator

A monolithic voltage-controlled oscillator (VCO), MAX2622, based on silicon germanium technology, and combines an integrated oscillator and output buffer in a miniature 8-pin package [14] was examined for operation between -195°C and +85°C. Performance characterization was obtained in terms of output frequency and its dependence on the tune voltage ( $V_{tune}$ ).

The oscillator output frequency at various tune voltages is shown as a function of temperature in Figure 23. For any given test temperature, the output frequency increases with an increase in the external control tune voltage. It can be also seen that the frequency increases, almost linearly, as the temperature is decreased from  $+85^{\circ}$ C to  $-150^{\circ}$ C. This trend is observed at all levels of the applied tune voltage. As the temperature is further decreased beyond  $-150^{\circ}$ C, down to  $-195^{\circ}$ C, the oscillating frequency experiences insignificant increase. These temperature-induced effects on the frequency of this voltage-controlled oscillator are depicted in Figure 24, at various levels of tune voltage.



Figure 23. Oscillator frequency versus temperature for various tune voltages.



Figure 24. Oscillator frequency versus tune voltage at different temperatures.

A typical waveform of the oscillator frequency as recorded by a spectrum analyzer at  $+20^{\circ}$ C is shown in Figure 25. Those obtained at the extreme temperatures of  $+85^{\circ}$ C and  $-195^{\circ}$ C are shown in Figures 26 and 27, respectively. Once again, the shift in frequency of this voltage-controlled oscillator is evident with change in test temperature. These waveforms were recorded with an applied external voltage of 1.5 V to the tune voltage pin of the device.







Figure 26. Oscillator output frequency at +85°C.



Figure 27. Oscillator output frequency at -195°C.

A comparison of the output frequency of the oscillator as a function of tune voltage at test temperatures of +20, +85, and -195°C for pre- and post-cycling conditions are shown in Figures 28. It can be clearly seen that the post-cycling frequency/voltage curves at any given temperature were the same as those obtained prior to cycling; an indicative of no effect of thermal cycling.



Fig 28. Frequency vs tune voltage for pre-(left) and post-cycling(right) conditions.

# SOI Technology

#### Half-bridge driver

The operation of an SOI high temperature, half-bridge driver geared for driving both the highside and the low-side power of N-channel, metal-oxide semiconductor field-effect transistors (MOSFETs) in DC-DC converters and electric motor control applications, CHT-HYPERION [15], was investigated as a function of temperature between -190°C and +225°C. Providing a 200 kHz square wave as the control signal for the pulse-width-modulation (PWM) input pin, the SOI driver chip was characterized in terms of its high-side and low-side output signals, propagation delay times, and supply current at specific test temperatures. The propagation delay times included  $t_{pdl}$ , the transition delay between the PWM signal and the low-side driver output signal (LSDRV), and  $t_{pdh}$ , the transition delay between the high-side (HSDRV) signal and LSDRV; sometimes referred to as "dead time". The HSDRV output was configured to follow the PWM logic.

Waveforms of the CHT-HYPERION high-side driver (HSDRV) and the low-side driver (LSDRV) output signals along with the external PWM signal are recorded Figures 29-31. The driver maintained proper operation and no major change was observed in the shape or magnitude of these waveforms as test temperature was changed throughout the range of  $-190^{\circ}$ C to  $+225^{\circ}$ C.



Figure 29. Signals of HSDRV (#1), LSDRV (#2), & PWM (#3) at +20°C. (Scale: Vertical 5 V/div; Horizontal 2 µs/div)



Figure 30. Signals of HSDRV (#1), LSDRV (#2), & PWM (#3) at -190°C.



Figure 31. Signals of HSDRV (#1), LSDRV (#2), & PWM (#3) at +225°C.

Figure 32 shows the propagation delay time  $t_{pdl}$  between the PWM signal and the low-side driver output signal (LSDRV), and the transition delay  $t_{pdh}$  between the high-side (HSDRV) signal and LSDRV of the half-bridge driver as a function of temperature. It can be seen that while the delay time  $t_{pdl}$  decreased, almost linearly, with decreasing temperature, the transition delay between the high-side (HSDRV) signal and LSDRV, i.e.  $t_{pdh}$ , remained largely unaffected with temperature between - 100°C and +225°C. As the test temperature was

further decreased below  $-100^{\circ}$ C, however, this transition delay time experienced a noticeable increase with decreasing temperature; reaching a value of 80 ns at the cryogenic level of  $-190^{\circ}$ C as compared to that at room temperature of 52 ns.



Figure 32. Transition delay times,  $t_{pdl}$  and  $t_{pdh}$ , as a function of temperature.

The duty cycle of the half-bridge driver exhibited similar behavior with temperature to that of the transition time,  $t_{pdh}$ . As shown in Figure 33, the duty cycle began to increase slightly only at test temperatures of -100°C and lower. The input current of the driver chip showed some modest dependency on temperature as it increased when temperature increased and the reverse was true, as shown in Figure 34. The variation in the supply current amounted to about 0.9 mA over the temperature span of -190°C to +225°C.



Figure 33. Duty cycle of the CHT-HYPERION as a function of temperature.



Figure 34. Supply current of the CHT-HYPERION as a function of temperature.

The SOI half-bridge driver was able to successfully restart at both extreme temperatures and thermal cycling produced no effect on its investigated parameters, as illustrated in Table V.

	Trans	sition	Tran	sition	Duty Cycle (%)		Input Current (mA	
	Time t <sub>p</sub>	odl (ns)	Time t <sub>pdh</sub> (ns)					
Temp. (°C)	Prior	Post	Prior	Post	Prior	Post	Prior	Post
+20	22.2	22.3	50.8	50.2	50.4	50.4	1.20	1.20
-190	16.8	16.7	79.9	78.0	56.0	55.9	0.94	0.94
+225	30.7	30.4	53.3	52.9	49.8	49.8	1.82	1.82

Table V. Pre- & post-cycling values of transition delay times, duty cycle, and input current.

## Circuits

## Timer

An electronic timer was assembled in a monostable circuit configuration using an SOI CHT-555 chip and a few passive devices [16]. Circuit schematic and board photograph are shown in Figure 35. The circuit was evaluated in terms of output waveform, pulse duration, and supply current as a function of temperature between  $+100^{\circ}$ C and  $-195^{\circ}$ C and under thermal cycling.



Figure 35. Monostable CHT-555 timer circuit.

The trigger, output, and threshold voltage waveforms of the timer circuit were obtained at various temperatures but, for illustrative purpose, only those pertaining to room temperature,  $-195^{\circ}$ C, and  $+100^{\circ}$ C are shown in Figures 36-38, respectively. No significant changes occurred in the output's waveform, duty cycle, and frequency with variation in test temperature. The timer was able to successfully cold-restart at  $-195^{\circ}$ C, and thermal cycling had no impact on the behavior of this SOI timer.



Figure 36. Waveforms of trigger (1), output (2), and threshold (3) signals at +20 °C.



Figure 37. Waveforms of trigger (1), output (2), and threshold (3) signals at -195 °C.



Figure 38. Waveforms of trigger (1), output (2), and threshold (3) signals at +100 °C.

### **Circuit Boards**

#### Flexible printed circuit board

Flexible printed circuit boards and those employing flip chip technology are finding widespread use in many industrial and aerospace applications. NASA is currently exploiting the use of such boards in electronic systems

designed for future space missions. In a collaborative effort between NASA GRC and NASA LaRC, two flexible printed circuit boards were characterized in terms of their dielectric properties and physical structure under thermal cycling in the temperature range between  $-125^{\circ}$ C and  $+100^{\circ}$ C. The flexible boards were designed and built by NASA LaRC. Each board had a three-layer structure of LaRC-SI (Soluble Imide) insulating material with seven serpentine-shape copper traces sandwiching the board between them [17]. While both boards had LaRC-SI polyimide as the base insulation, half of board #2 also included boron nitride as an additive on two flex layups in order to facilitate local changes in capacitance by serving to initiate delamination during extreme environmental testing. Photographs of board #1 and board #2 are shown in Figures 39 and 40, respectively.



Figure 39. Photograph of Board #1.



Figure 40. Photograph of Board #39.

Besides visual examinations for delamination and other physical damage, the two flexible printed circuit boards were tested at various temperatures before and after thermal cycling in terms of capacitance and dissipation factor of the seven traces over a wide frequency range. Similar results were obtained in the dielectric properties of all traces for both boards due to extreme temperature exposure, and limited thermal cycling produced no noticeable effect on the physical integrity of either board. For illustrative purposes, the capacitance and dissipation factor for trace 4 of board #2 are shown in Figure 41 as a function of frequency at different temperatures, and capacitance test data at intervals up to 20 cycles of all seven traces of board #1 are listed in Table VI at 1 kHz.



Figure 41. Capacitance and dissipation factor of trace 4 of board #2 versus frequency.

	original		value after consecutive								
	value	1 cycle	3 cycles	5 cycles	10 cycles	20 cycles					
Trace 1	105.06	104.92	104.32	105.10	103.73	105.19					
Trace 2	109.94	110.30	108.82	110.15	107.03	110.19					
Trace 3	108.50	108.51	107.90	108.24	106.24	108.09					
Trace 4	119.83	119.69	119.04	118.94	116.95	119.48					
Trace 5	116.94	117.20	117.29	115.95	114.28	115.90					
Trace 6	118.39	117.78	117.39	116.70	114.58	117.07					
Trace 7	110.06	109.55	109.55	108.81	106.35	109.75					

Table VI. Room temperature capacitance (pF) for board #1 at 1 kHz as a function of thermal cycling.

#### Flip chip printed circuit board

In a collaborative effort between NASA GRC and JPL, a flip chip printed circuit board was provided by JPL for in-house evaluation under thermal cycling to extreme temperatures. The Flipchip Technologies, Inc. board (FB250/500 REV-A) was populated with a total of ten chips and had a 20-connector termination. A photograph of the flip chip printed circuit board is shown in Figures 42. The flip chip board was characterized in terms of electrical continuity of the various circuit traces between the connector terminals 1 through 20. The board was examined for physical integrity and condition prior to and after completion of the tests [1]. Resistance measurements were made in the temperature range of  $+90^{\circ}$ C to  $-125^{\circ}$ C before and after thermal cycling. The printed circuit board was also checked for changes in physical integrity, such as delamination, warping, and discoloration that might have occurred due to the extreme temperature exposure and thermal cycling.



Figure 42. Top view of the flip chip printed circuit board.

Changes in the resistance, i.e. trace continuity, between terminals 1 and 2 and that between terminals 19 and 20 versus temperature before thermal cycling are shown in Figure 43 as a function of temperature. It can be clearly seen that the resistance changes in direct proportion to the test temperature. Such was the case for all traces as depicted in table VII. Thermal cycling had little effect on the resistance (continuity) of all traces as the corresponding data listed in Tables VII and VIII for pre- and post-cycling conditions, respectively, were very comparable. Following the thermal cycling, the printed circuit board appeared to undergo no changes in its structural integrity as no delamination or warping was revealed upon examination visually or under a microscope.



Figure 43. Pre-cycle resistance between terminals 1-2 (left) and 19-20 (right) versus temperature.

		Resistance $(\Omega)$ between terminals									
Temp (°C)	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	17-18	19-20	
90	2.445	2.525	2.525	2.585	2.465	2.445	2.345	2.425	2.365	2.485	
25	1.964	2.024	2.004	2.084	1.964	2.004	1.804	2.004	1.804	2.004	
-125	.862	.842	.882	.902	.862	.862	.822	.842	.842	.862	

Table VII. Trace resistance before thermal cycling.

		Resistance ( $\Omega$ ) between terminals									
Temp (°C)	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	17-18	19-20	
90	2.445	2.525	2.525	2.605	2.465	2.425	2.345	2.425	2.365	2.485	
25	1.984	2.044	2.024	2.104	1.964	1.964	1.924	1.944	1.924	1.964	
-125	.882	.902	.882	.922	.862	.862	.822	.862	.822	.882	

Table VIII. Trace resistance after thermal cycling.

#### Summary

Representative data obtained on several COTS electronic parts of various electronics technologies were presented in this supplementary digest. This work was performed under the support of the NASA NEPP Program and addressed performance and reliability of the investigated test articles under extreme temperature exposure and wide-range thermal cycling. Detailed test results and discussions pertaining to these specific parts are posted on the NASA NEPP website. Another follow-on digest covering other tested COTS parts will follow.

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#### Acknowledgements

This work was performed in support of the NASA Electronic Parts and Packaging (NEPP) Program. Part of this effort was done at the NASA Glenn Research Center under GEARS Contract 80GRC020D0003.