Thermal Cycling/Shock Behavior of CSP Assemblies

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Abstract

A JPL-led chip scale package (CSP) Consortium of enterprises, composed of team members representing government agencies and private companies, recently joined together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. The experience of the Consortium in building more than 150 test vehicle assemblies, single- and double-sided multilayer PWBs, and the environmental test results has now been published as a chip scale package (CSP)guidelines document and distributed by Interconnection Technology Research Institute (ITRI).

The Consortium assembled fifteen different packages with I/Os from 48 to 784 and pitches from 0.5 to 1.27 mm on multilayer FR-4 printed wiring board (PWB). Another test vehicle was designed and assembled by a team member using their internal resources and was identified as TV-H. The TV-H assemblies were subjected to numerous thermal cycling conditions including -55°C to 125°C with two ramp rates, one thermal cycle with 2° to 5°C/min and the other near thermal shock. Cycles-to-failure (CTF) test results to 1,000 cycles and 400 cycles under these conditions are presented for 180 and 208 I/O fine pitch ball grid arrays (FPBGAs) with three die sizes. Decrease in CTFs due to ramp rate and die size increase for different I/O FPBGAs with 0.8 mm pitch are compared and analyzed.

Introduction

Chip scale packages are now widely used for many electronic applications including portable and telecommunication products. The CSP definition has evolved as the technology has matured and refers to a package with a pitch of 0.8 mm and lower. Packages with fine pitches, especially those with less than 0.8 mm, and high I/Os may require the use of microvia printed wiring board (PWB) which is costly and they may perform poorly when they are assembled onto boards. A test vehicle (TV-1) with eleven package types and pitches was built and tested by the JPL MicrotypeBGA Consortium during 1997 to 1999. Lessons learned by the team were published as a guidelines document for industry use[1].

The finer pitch CSP packages which subsequent to TV-1 became available were included in a follow-on test vehicle of the JPL CSP Consortium [2]. The Consortium team jointly concentrated their efforts on building the second test vehicle (TV-2) with fifteen (15) packages of low to high I/O counts (48 to 784) and pitches of 0.5 mm to 1.27 mm. In addition to the TV-2 test vehicle, other test vehicles were designed and built by individual team members to meet their needs. At least one common package was included as control in each of these test vehicles in order to be able to compare the environmental test results and understand the effects of PWB build and manufacturing variables.

One test vehicle, herein refers to TV-H, was designed and assembled by Hughes Network System using their internal resources. This paper presents the thermal cycling test results to 1,000 cycles (-55 to 125°C) for a variety of CSPs used on the TV-H assembly. CTF test results are compared to those performed under this temperature range, but with a more severe near thermal shock condition to 400 cycles.

TEST MATRIX

Test Vehicle Package I/O /PWB

The TV-H had eight packages with I/Os ranging from 48 to 280 and pitches of 0.8 mm to 1mm. The PWB had four layers with the two resin coated copper (RCC) layers and an FR-4 core (1+2+1) having a total thickness of 0.43 mm. Microvia technology was used. The pad had a 0.1 mm (4 mil) microvia hole at the center of pad. A non-solder-mask-design (NSMD) pad with a diameter of 0.3 mm and 0.05 mm clearance was used. The surface finish of the PWB was Ni/Au immersion with about 2-8 micro inch of gold over 100-200 micro inch Ni. No clean solder paste was applied for assembly using a 5 mm laser-cut stencil thickness. The test vehicle was 11.9 cm by 4.6 cm (4.75″ by 1.85″) with a connector interface for continuous monitoring of daisy chains during thermal cycling.

Test Vehicle Features/Daisy Chain Patterns

A full populated test vehicle (TV-H) with two sites for the 280 I/O fine pitch ball grid array (U4 and U2 sites) was shown in the January 2001 issue of EEE Links. All packages were daisy-chained, and they were divided into several internal chain patterns. The daisy chain pattern on the PWB completes the chain loop into the package through solder joints. Several probing pads connected to daisy chain loops were added for failure site diagnostic testing. All packages were prebaked at 125°C for 2 ½ hours prior to assembly.

TEST CONDITIONS

Thermal Cycling test

Thermal cycling was performed in the range of -55°C to 125°C under two different conditions. Chamber setting and thermal couple readings for conditions A and B are shown in Figure 1 and 2, respectively. For condition A, the heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes and a shorter dwell time duration at the minimum temperature. Each cycle lasted 159 minutes.

The near thermal shock cycle, condition B, had the same temperature range performed in a chamber with three regions of hot, ambient, and cold. Heating and cooling rates were nonlinear and varied averaging between 10 to 15 °C/min. with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.

Monitoring

The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 7.8, were used as guidelines to interpret electrical interruptions. In general, it is expected that once the first interruption is observed, there will be a large number of additional interruptions within the 10% of the cycle life. This was not the case especially for the wafer level package assemblies. Failures detected by continuous monitoring were verified manually at room temperature after weekly removal from the chamber.

THERMAL CYCLING RESULTS

Figure 3 shows the test results for the 180 I/O FPBGA with a die size of 6.3 mm and the 208 I/O with the die sizes of 11.4 and 9.5 under the same thermal cycling range (-55°C/125°C), but with two different ramp rates, A and B conditions. It is apparent that under the near thermal shock cycle, the CTFs for the 208 I/O package with 11.4 and 9.5 mm dies were within the data scatter. This is not the case for those under thermal cycle A condition where the effect of die size clearly demonstrated. The CTFs for the 180 I/O package with a 6.3mm die size are also differed significantly under two cycling conditions. The CTFs were in the range of 145 to 389 cycles for the near thermal shock whereas the first failure was observed at 778 cycles for the thermal cycle condition.

CONCLUSIONS

These conclusions are based on the results limited to assembly failures to 1,000 thermal and 400 near shock cycles in the range of -55°C to 125°C. Addition thermal and mechanical cycling data with their failure analyses are being gathered to further define the effects of various parameters on assembly reliability.

- Cycles-to-failures for the fine pitch ball grid arrays (FPBGAs) with 0.8 mm pitch were in the range of 300 to 800 and 100 to 200 cycles for thermal cycle and near thermal shock conditions, respectively. The CTFs fir both conditions are significantly lower than the ones observed earlier with their 1.27 mm pitch BGA counterparts [1].
- CTFs decreased as package die size increased under thermal cycle condition. The effect of die size decrease from 11.4 mm to 9.5 mm could not be clearly identified by the near thermal shock condition. Additional tests are being performed for further analysis.
- The 208 I/O FPBGA package with the largest relative die size to package dimension (11.4 mm die in 15x15 mm package) showed the lowest CTFs and the 180 I/O package with the lowest relative die size to package (6.3 mm die in 12x12 mm package) showed the highest CTFs under thermal cycle condition.

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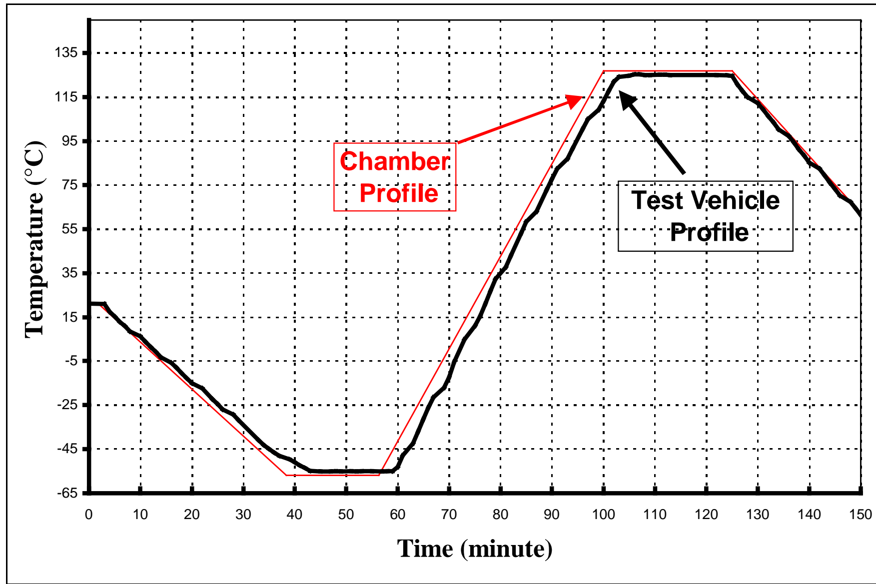

Figure 1 Thermal cycle profile in the range of –55°C to 125°C, condition A, 159 minutes/cycle

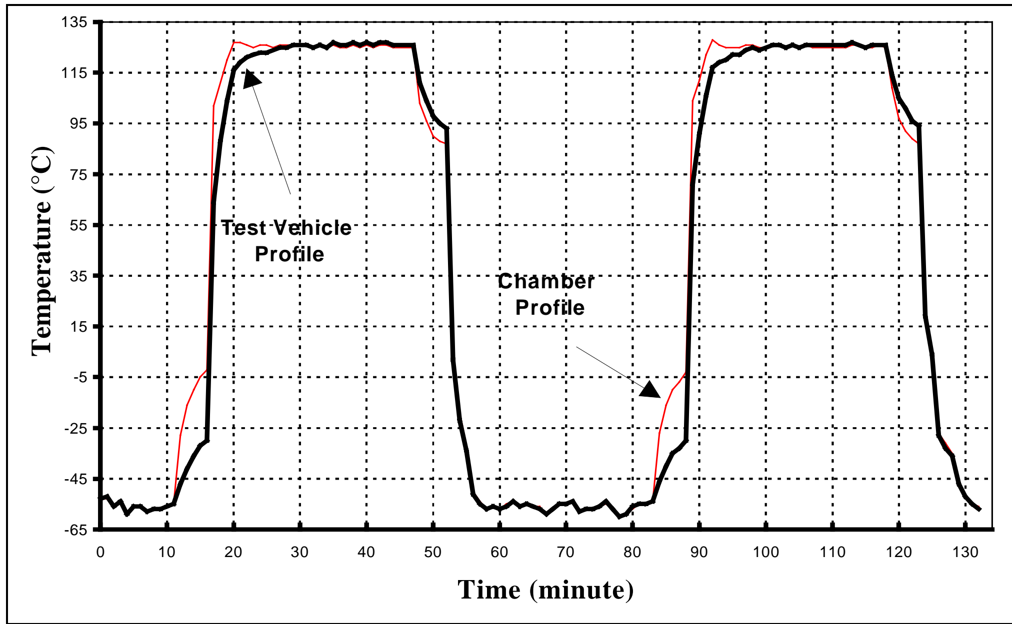

Figure 2 Near thermal shock profile in the range of –55°C to 125°C, condition B, 68 minutes/cycle

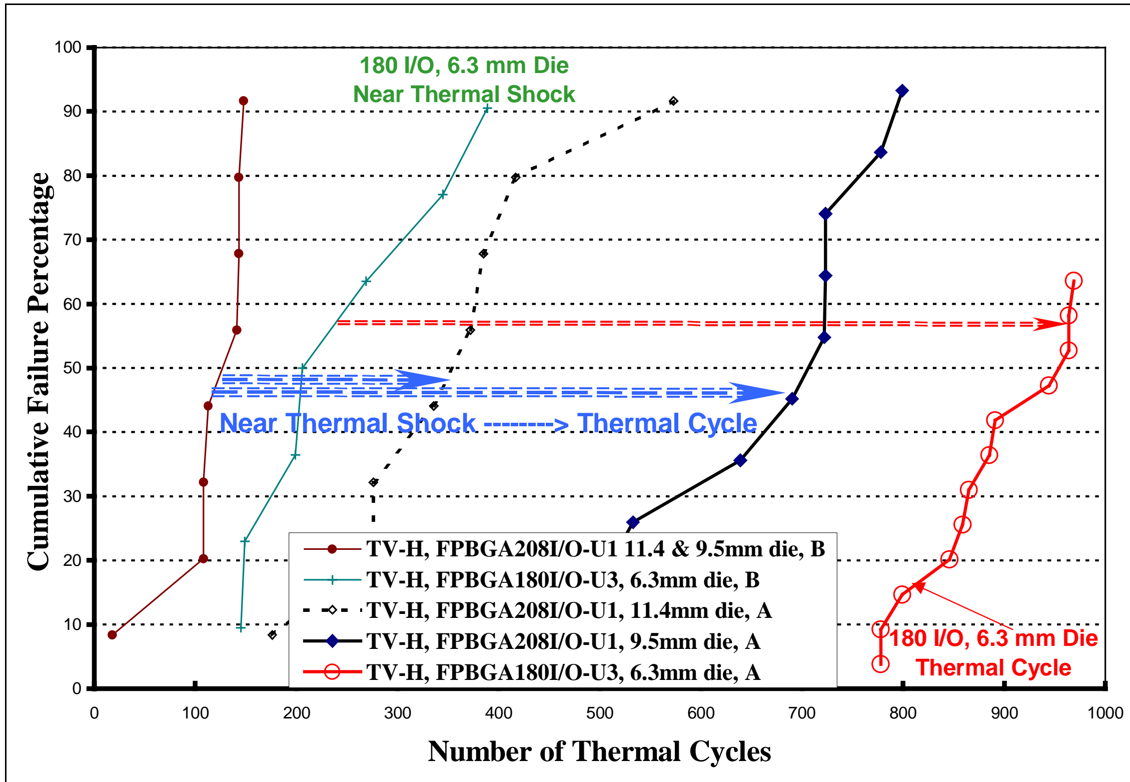

Figure 3 Cumulative Failure Distribution for the Same FPBGA Package and I/Os Under the Same Thermal Cycling Range (-55 ° to 125°C) But Two Different Rates