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National Aeronautics and
Space Administration

Jet Propulsion Laboratory
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Table of Contents

Abstract
This paper describes the design tradeoffs between Actel and Xilinx high-reliability field programmable gate arrays (FPGAs). It has been written in response to recent concerns over failures on Actel RTSX-S (MEC) devices. An industry tiger team has been formed to investigate the issues and provide recommendations for use. A final disposition has not been released.

1. Introduction

The type of FPGA technology and device family used in a design is a key factor for system reliability. There are basically three types of programming technologies currently in existence: antifuse-based, flash-based, and SRAM-based. Each type has advantages and disadvantages associated with its use in flight applications. Some of the characteristics of SRAM- and antifuse-based device technologies are compared in Table 1. At present, there is no flash-based FPGA with acceptable radiation tolerance for space applications. Xilinx total ionizing dose (TID) specifications are detailed in Xilinx's data sheets, and are in compliance with the methodology of method 1019.5.

Table 1: Programming Technology Comparison

	ANTIFUSE	SRAM
Reprogrammable	No	Yes
Nonvolatile	Yes	No
Start-up time	Low (less than 1 ms)	Significantly higher (greater than 100 ms)
Power consumption	Less	Generally more: Xilinx has many power-estimation tools
Architecture	Multiplexers, Registers, C-cells, R-cells	Configuration Logic Blocks (LUT, F/F), BRAM, Multipliers (Virtex-II)

For each type of programming technology there are multiple device families. Table 2 shows the Actel Rad-Hard and Rad-Tolerant and Xilinx Rad-Tolerant 4000XL series, Virtex, and Virtex-II FPGA device families and their operating voltages, system gate complexities, packages, availability, source manufacturing drawing (SMD) numbers and foundries. Table 3 (in Section 2) shows the same devices with their advertised resistance levels to TID and single event upsets (SEU). A designer must weigh the cost, reliability, performance, and functions when choosing the FPGA technology and device family for the required design.

Table 2: Some Attributes for Actel and Xilinx Rad-Tolerant FPGAs

Device	Core Voltage (V)	I/O supply (V)	System Gates (k)	Packages	Availability	SMD#	Foundry
Actel Rad-Hard							
RH1020	5	5	3	CQFP84	now	5962F9096505	BAE
RH1280	5	5	12	CQFP172	now	5962F9215603	BAE
Actel Rad-Tolerant							
RT1020	5	5	6	CQFP84	now	None	BAE
RT1280A	5	5	24	CQFP172	now	5962-92156	MEC
RT1425A	5	5	7.5	CQFP100	now	5962-95520	MEC
RT1460A	5	5	18	CQFP196	now	5962-95508	MEC

Device	Core Voltage (V)	I/O supply (V)	System Gates (k)	Packages	Availability	SMD#	Foundry
RT14100A	5	5	30	CQFP256	now	5962-95521	MEC
RT54SX16	3.3/5	5	24	CQFP256	now	5962-9956901	MEC
RT54SX32SU	2.5	3.3/5	48	CQFP208/ 257	now	5962-0150801	UMC
RT54SX72SU	2.5	3.3/5	108	CQFP208/ 257	now	5962-0151502	UMC
RTAX250SU	1.5	3.3	250	CQFP 208/352	2Q2005	n/a*	UMC
RTAX1000SU	1.5	3.3	1000	CGA624/ CQFP352	2Q2005	n/a*	UMC
RTAX2000SU	1.5	3.3	2000	CGA624/ CQFP352/ CGA1152	2Q2005	n/a*	UMC
XQR 4000XL Series FPGAs							
XQR4013XL	3.3	5	10–30	CB228	now	n/a*	UMC
XQR4036XL	3.3	5	22–65	CB228	now	n/a*	UMC
XQR4062XL	3.3	5	40–130	CB228	now	n/a*	UMC
Virtex 100 krad TID guaranteed							
XQVR300	2.5	3.3	32.3	CB228	now	5962R9957201	UMC
XQVR600	2.5	3.3	66.1	CB228	now	5962R9957301	UMC
XQVR1000	2.5	3.3	112.4	CG560	now	5962R9957401	UMC
Virtex-II 200 krad TID guaranteed							
XQR2V1000	1.5	1.8–3.3	1000	BG575 FG456	now	n/a*	UMC
XQR2V3000	1.5	1.8–3.3	3000	CG717 BG728	now	n/a*	UMC
XQR2V6000	1.5	1.8–3.3	6000	CF1144	now	n/a*	UMC

Note:
* n/a = data not yet available

Below, we discuss some of the major factors to consider in selecting Actel Rad-Tolerant antifuse-based and Xilinx Rad-Tolerant SRAM-based Virtex/Virtex-II FPGAs.

1a. Ideal FPGA for Space Applications

An ideal FPGA for space applications is the qualified manufacturing line (QML) Class V with radiation hardness assurance (RHA) level identified as part of the SMD part number. Only Class V is space quality. All other levels contain uncontrolled processes, which have risk(s) for space flight. The ideal FPGA is a high-density SRAM-based that is not susceptible to SEU. As for TID, 300 krad (Si) is sufficient for the great majority of missions. High SEU tolerance is essential for FPGAs used in critical applications: a threshold of at least 37 MeVcm^2 /mg for upsets in both configuration memory (SRAM-based FPGAs) and user flip-flops and registers. For reprogrammable FPGAs, nonvolatile memory–based devices (if they can meet the radiation requirements) would be preferable to SRAM-based devices. For all types, some dedicated memory to help improve density would be desirable. Although performance is not as critical in space applications, the selected FPGA's performance should be reasonably close to the performance of comparable commercial FPGAs, and full performance should be maintained over the military temperature range. The most important factor is reliability; both the foundry and assembly/test

facility should be Defense Supply Center Columbus (DSCC) certified to QML level V and a full level V flow (without significant "optimizations") should be available.

Anti-fuse FPGAs are used in critical applications where the SEU sensitivity of existing SRAM-based FPGAs and the reconfiguration time for SEU mitigation are issues. In noncritical applications, SRAM-based FPGAs are widely used for density and reprogrammability. Design tools that support design for testability and include (or interface to) tools for test vector generation and fault grading of test vectors are also desirable.

2. FPGA Radiation Considerations

Although results of radiation tests of antifuse-based FPGAs can be compared to results from SRAM-based FPGAs, the two technologies are quite different. Antifuse-based FPGAs are programmed via permanent interconnections, so logic upsets due to radiation effects will not cause programs to be lost. Thus, it is not possible to make assumptions about the radiation tolerance of SRAM-based FPGAs based on test results of antifuse-based devices. Table 3 shows the radiation data on Actel and Xilinx FPGAs. Table 4 shows radiation data on rad-tolerant PROMs from Xilinx. SEL performance is identified for all of the Actel and Xilinx FPGAs discussed in this paper, which meets JPL requirements. The built-in TMR on the Actel RT54SX-S and RTAX-S devices reduces the upset rate well below most projects' requirements. For Xilinx devices, designers must implement recommended SEU mitigation techniques by Xilinx.

These techniques have been detailed in the literature, have been verified by independent testing (including testing by Gary Swift of JPL), and are fully supported by the Xilinx production-released TMR tool.

Table 3: Actel RH and RT FPGA and Xilinx Virtex and Virtex-II FPGA Radiation Comparison

Device	TID (krad (Si)	SEL (LET) (MeV cm^2/mg)	SEU (LET) (MeV cm^2/mg)	SEU rates, interplanetary space, solar minimum		
				Flip-flops	RAM blocks[3]	SEFI
Actel Rad-Hard						
RH1020	300	>84	8	none[4]	none[4]	clock upsets
RH1280	300	>120	4 S-mod 17 C-mod	1 per 150 days	none[4]	clock upsets
Actel Rad-Tolerant						
RT1020	100	>84	8			
RT1280A	7 to 60	>120	5 S-mod 26 C-mod			
RT1425A	20–70	>110	5 S-mod 28 C-mod			
RT1460A	20–70	>110	5 S-mod 28 C-mod			
RT14100A	20–70	>110	5 S-mod 28 C-mod			
RT54SX16	80–135	>120	17			
RT54SX32S	135[1]	>100	>50	1 per 14000 years	none[4]	none[4]
RT54SX72S	135[1]	>100	>50	1 per 6800 years	none[4]	none[4]
RTSX32SU[5]	100	>100		SEU LET th >> 37	none[4]	none[4]
RTSX72SU[5]	100	>100		SEU LET th >> 37	none[4]	none[4]
RTAX250S	200	>100	>50	1 per 19000 yrs	<1E-10 e/b-d	none[4]
RTAX1000S	200	>100	>50	1 per 4500 yrs	<1E-10 e/b-d	n/a[2]

Device	TID (krad (Si)	SEL (LET) (MeV cm^2/mg)	SEU (LET) (MeV cm^2/mg)	SEU rates, interplanetary space, solar minimum		
				Flip-flops	RAM blocks[3]	SEFI
RTAX2000S	200	>100	>50	1 per 2500 yrs	<1E-10 e/b-d	n/a[2]

Xilinx XQR4000 Series						
XQR4013XL	60	>100		1 per 130 days	none[4]	n/a[2]
XQR4036XL	60	>100		1 per 48 days	none[4]	n/a[2]
XQR4062XL	60	>100		1 per 28 days	none[4]	n/a[2]
Xilinx Virtex						
XQVR300	100	>125		1 per 2.5 days	1 per 45 days	1 per 70 years
XQVR600	100	>125		1 per 1.1 days	1 per 30 days	1 per 70 years
XQVR1000	100	>125		1.5 per day	1 per 22 days	1 per 70 years
Xilinx Virtex-II						
XQR2V1000	200	>125		1.8 per day	1 per 1.7 days	1 per 70 years
XQR2V3000	200	>125		4.6 per day	1.4 per day	1 per 70 years
XQR2V6000	200	>125		10.3 per day	2.2 per day	1 per 70 years

Notes:
RTSX-SU radiation results available on Actel web site:

http://www.actel.com/products/aero/RTAX-S radiation results have been posted at MAPLD 2003 and MAPLD 2004

1. Rev 2 only. Rev 0 devices were 50–80 krad (Si), Rev 1 were 100 krad (Si) and were significantly more susceptible to upset, esp. protons.
2. n/a = data not yet available
3. The RAM upset rates are for the underlying memory cells, that is, before any error detection or correction. Similarly, the configuration SRAM rates do not consider the effects of scrubbing or the fact that most (~90%) configuration upsets do not affect even a "full" design's functionality.
4. Based on Actel and Xilinx data sheet; test data not yet available.
5. RTSX-SU radiation results available on Actel web site:
http://www.actel.com/products/aero/RTAX-S radiation results have been posted at MAPLD 2003 and MAPLD 2004

Table 4: PROM Usage for Xilinx FPGAs

Device	Configuration Bits	XQR17V16 PROMs	XQR18V04 PROMs	XQR1701L PROMs
XQVR300	1,751,808	1	1	2
XQVR600	3,607,968	1	1	4
XQVR1000	6,127,744	1	2	6
XQR2V1000	3,752,736	1	1	4
XQR2V3000	9,594,656	1	3	10
XQR2V6000	19,759,904	2	5	20

3. TID Performance

Actel rad-tolerant products have TID performances between 100 and 300 krad (Si), depending on the device family and lot. Xilinx devices offer TID performance (guaranteed by rad-hard assurance testing of every wafer fabrication lot) from 100 to 200 krad (Si). Both companies perform the TID test per method 1019.5. Typically, ACTEL has declined to guarantee TID performance of their parts, and their literature suggests that users verify the TID performance of specific lots in actual applications testing. Only Xilinx guarantees TID performance to specification and conducts hardness assurance testing on every wafer fabrication lot in accordance with the principles of method 1019.5.

4. SEU Performance

High SEU tolerance is essential for FPGAs used in critical applications, including space, with a threshold of at least 37 MeVcm^2/mg for upsets in both configuration memory and user flip-flops and registers. See Table 3 for details.

5. SEU Mitigation Techniques

Xilinx chips are chosen based on the radiation tolerance, high gate density, on-board RAM, and large I/O count offered by the Virtex and Virtex-II family. Onboard reprogrammability of the FPGAs allows for design changes and updates right up to launch time, allowing the design team to meet demanding schedules.

Xilinx SRAM-based devices are SEU soft**;** high SEU tolerance is essential for FPGAs used in `critical applications, with a required threshold of at least 37 MeVcm^2/mg for upsets in both configuration memory and user flip-flops and registers. There are two basic categories of upsets:

a. SEU, which causes bit flip in the affected memory elements

b. Single-effect functional interrupt (SEFI), which applies to control circuits and in turn affects device functionality

These categories are subdivided as follows:

- Configuration bit upset (SEU)
- Block RAM (BRAM) upsets (SEU)
- Power-on-rest (POR) circuit upsets (SEFI)
- Select map port circuit upsets (SEFI)
- JTAG port circuit upsets (SEFI)

Virtex-II can become effectively SEU-immune if designers are informed of the following recommended mitigation techniques: (1) applying the care and discipline required to properly implement the combination of TMR and configuration scrubbing and (2) obtaining additional supporting parts in addition to the FPGA, particularly PROMs and a watchdog timer.

Xilinx parts have a couple of SEFI modes, and any project that uses them must accept the risk they entail. (SEFIs, though rare, require a reconfiguration that is intrusive to device operation for a brief period.) Because any upset mitigation fails if the flux is high enough, a combination of XTMR and a scrubbing technique is applied to lower the likelihood of an upset-induced system error to below that of the SEFI probability. In-beam testing is recommended to verify that this goal is achieved. XTMR's main purpose is NOT to protect the design from upset of its memory elements and flip-flops (although it does have a beneficial effect there); it mainly guarantees functionality in the presence of an error in the configuration.

Another concern regarding Virtex devices is half latches. Half latches are sometimes used within these devices for internal constants, as this is more efficient than using logic. Radiation-induced changes in half latches are not detectable; therefore, if they are being utilized, they should be removed during radiation testing.

5a. User Logic SEU Mitigation Techniques

One method of increasing a design’s resistance to SEU effects is by implementing the design using TMR, which may have up to 3.2× the gate count and a performance cost of approximately 10%.

Xilinx SRAM-based FPGAs require the designer to implement TMR for user logic. Xilinx has recently released their TMR tool (XTMR). Currently, JPL does not have sufficient information about these tools to determine its effectiveness. The Xilinx serial configuration bit-stream must be monitored for flip-flops, which can be done without interfering with normal operation. Upon detection of an error, the configuration can be reloaded. The Virtex-II family can be partially reconfigured, which eliminates downtime.

In Actel's RT54SX-S and RTAX-S family all internal registers are designed with built-in TMR, while the I/O registers are not. However, in RTAX-S devices there are added block RAMs that are not hardened. Actel provides a built-in macro to perform background scrubbing with EDAC. JTAG circuitry is not rad-tolerant, so test logic reset (TRST) must be hardwired to ground to enhance SEU immunity.

5b. Configuration Bits SEU Mitigation (Xilinx only)

In addition to implementing TMR for user logic, the configuration data must be monitored. Upon detection of an error, a reconfiguration of the SRAM memory is initiated. For Virtex and Virtex-II, a time-saving partial reconfiguration is also possible. While detection and correction is a possible solution, scrubbing at 10× the expected upset rate is much more efficient. A scrub function is implemented on the Xilinx chip itself (using TMR) or in the programming environment supporting the Xilinx FPGA's reconfiguration.

Configuration files in the Xilinx Virtex families can be continuously scrubbed in the background, so that user logic is not affected and there is no need to pause the user's application. The scrub function differs from the configuration bit stream program function, though they are very similar. Scrubbing is vital, because even for designs that use TMR, SEUs can be accumulated over time to the point where TMR will no longer be effective. Another alternative for Xilinx is to use TMR at the part level.

6. Architecture

Starting with the Virtex series, Xilinx added BRAMs to their architecture. For the Virtex-II FPGAs, Xilinx also added (among other improvements) blocks of 18×18 multipliers, which are a suitable addition for DSP applications. These added BRAMs and block multipliers make the Xilinx Virtex and Virtex-II series more suitable for computation-intensive applications.

The Actel RT54SX is based on the sea-of-modules architecture, which is denser and more area-efficient than the Virtex series architecture. Actel uses small and simple logic blocks (C-cells and R-cells). However, the computation function is not implemented efficiently in Actel FPGAs, which are more effectively used for controller functions.

7. Fan Out

For the Actel RT54SX-S and RTAX-S families, the internal logic has a fan-out limit of 10 loads. For Xilinx parts, the internal fan-out limit is 100 loads.

8. Operating Temperature

For most of the rad-tolerant FPGAs, the temperature range is –55 to 125 °C for both Actel and Xilinx. The exception is the XQR18V04 PROM, with a range of –55 to 100 °C. Start-up for the XQVR1000 is limited to a lower level of –40 °C. This is detailed in the data sheet for this part.

9. Operating Clock Speed

Specifying an operating clock speed is not really feasible in an FPGA. This is neither an application-specific integrated circuit (ASIC), nor an application-specific standard product (ASSP). The operating clock speed is dependent on the design. A fair comparison would require implementing the same design in both FPGAs to see how they differ, although even this approach is hazardous, as some designs can be implemented more efficiently than others in certain FPGAs.

10. Set-up and Configuration Time Duration

Any FPGA is considered functional once the inputs and outputs behave as expected by the designer.

For Actel FPGAs, the exact moment a device becomes functional is dependent on the FPGA family and the ramp rate of V_{CCA} and V_{CCI} (assuming V_{CCA} is powered up simultaneously). For example, with a ramp rate of 0.25 V/µs at room temperature, it will take 8 µs to power up RTSX32S and 10 µs to power up RTSX72S. With a ramp rate of 0.025 V/ms, it will take 47 ms to power up RTSX32S and 40 ms to power up RTSX72S. It is important to note that Actel does not characterize the worst-case power up time for Actel devices. For further details see the following application note:
http://www.actel.com/documents/HotSwapColdSparing.pdf

For MEC RT54SX32S and RT54SX72S, high in-rush current is observed under certain power-cycling conditions. (See GIDEP [Government and Industry Data Exchange Program] Product Advisory SC7-P-03-04 for specifics.) This in-rush current is eliminated in the UMC RTSX-SU FPGAs.

Volatile SRAM-based FPGAs have to be configured during system power-up, which may last hundreds of milliseconds with a current peaking at over 2 A. In order to configure Xilinx FPGAs, a serial PROM, a microprocessor/microcontroller, or possibly an Actel FPGA (must be alive immediately) can be used on power-up to ensure that the Xilinx FPGA is programmed. Anything controlled by or using the Xilinx FPGA will be in an indeterminate state until the Xilinx is brought up, unless appropriate use of external lock-out/pull-down/etc. circuitry is designed. This configuration time has been improved in the Virtex-II family over the earlier Virtex products.

11. Synthesizable Logic Density

Vendors use different gate-counting methods for synthesizable gate density. This number is very much a marketing specification. If engineers want to compare functionality between devices, they need to look at the features that really count, such as available flip-flops and look-up tables (LUTs). The added functionalities, such as embedded memory, dedicated multipliers, and Xilinx Virtex-II or global clocking resources, provide more meaningful guidelines for comparing FPGAs.

Xilinx and Actel FPGAs have distinct architectural features that are not directly comparable. Table 2 shows the gate complexities in terms of system gates. The actual gate utilization and availability is design dependent.

12. MEC RTSX-S Failures

JPL and several Air Force contractors have reported failures on Actel RTSX-S (MEC) devices. As a result, an industry tiger team has been established (coordinated by the Aerospace Corporation) to determine the causes for these failures. Some of the possibilities are transients on the power supply or I/O rings,

programming algorithm deficiencies, and process variations in the antifuses. Contact the JPL part specialist for current information on the team investigation. Substantial testing is ongoing, and the results of those investigations may change recommendations for screening these devices. See JPL Interoffice Memorandum (IOM) 514-DJS-04-025 for more details.

Actel has released several versions of programming with significant improvements on the reliability of the MEC RTSX-S FPGAs. In addition, Actel has introduced a new version of these parts, RTSX-SU, with a new fuse design. Fabricated at United Microelectronics Corporation (UMC) Wafer Foundry, RTSX-SU has demonstrated no failures in over 1.5M device hours of testing.

JPL has not yet seen any problems due to short-duration transients on Xilinx FPGAs. However, JPL has limited experience using Xilinx FPGAs for flight applications. JPL should investigate the reliability issues of Xilinx devices in light of recent Actel RT54SX-S experiences to determine whether similar transient sensitivities affect the Xilinx parts.

13. FPGA Power Consumption

FPGAs have a unique power profile that varies with different FPGA technology. Actel antifuse-based FPGAs power characteristics are similar to ASICs. When determining the power consumption for different FPGA technologies, three basic power components must be considered. These components are discussed below.

13a. Dynamic Power

Dynamic power is the power consumed when the logic cells are switching. It varies by technology, design, and architecture. This power component is a major contributor to both heat dissipation and operating power consumption. It is more strongly influenced by the design than the device type.

13b. Start-Up Power

FPGAs require a certain amount of supply current during power-on to ensure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. (See the application notes for more details.). A power spike is caused when a system is powered up. Volatile SRAM-based FPGAs (i.e., Virtex FPGAs) have to be configured during system power-up, which may last hundreds of milliseconds, with current averaging over 50 mA and peaking at over 100 mA. To ensure that a Xilinx FPGA is programmed, either a serial PROM for self-boot or possibly an Actel FPGA or a microprocessor (if alive immediately) can be used on power-up.

Note that Xilinx parts do not need an Actel part or any other part to configure or power up. Some Xilinx application notes mention the use of a small Actel part to manage scrubbing, but there are alternatives to that approach, including totally managing the scrubbing function within the Xilinx FPGA itself. Also note that some applications do not use a PROM at all to configure the FPGA; they utilize system storage elsewhere to supply the configuration file. Anything controlled by or using the Xilinx FPGA will be in an indeterminate state until the Xilinx is brought up, unless generous use of external lock-out/pull-down/etc. circuitry is designed. SRAM-based FPGAs consume significantly more power at power-up than Actel RTSX-S devices. For RT54SX32S and RT54SX72S, high in-rush current is observed (see GIDEP Product Advisory SC7-P-03-04 for specifics).

Reconfigurability of SRAM-based FPGAs is a valuable feature to designers, since the design of these devices can be modified post-launch to fix problems or change their functionality. This is critical for “multi-missions” support.

13c. Static Power

Static power is defined as the minimum power required to keep the device ‘powered-up’ with the clock inputs not switching and I/Os drawing minimal power. Note that static power varies with temperature. The static power component for SRAM-based FPGAs is much higher than antifuse FPGAs. As the process scale-down continues (at 90-nm process technology), static power becomes the dominant power factor.

14. Parts Count and Footprint for Circuit Implementation

Implementing designs with Xilinx devices would require more board space if the designer requires in-system reprogrammability. Note that in-system programmability and—more importantly—reconfigurability is impossible with antifuse products. The PROM typically used for configuration of Xilinx FPGAs does not draw significant power, and hence it does not significantly affect the power budget. The added parts count for Xilinx FPGAs for configuration bits also contributes to their possibly lower reliability. In stand-alone applications where the FPGA is effectively the controller, high-density nonvolatile configuration memories (PROMs) are needed. The Xilinx Virtex 1000 requires 6 Mb for configuration memory; the Virtex-II 3000 requires 8.5 Mb. As a result, we need two XQR18V04s for Virtex 1000 and three XQR18V04s for Virtex-II 3000. Xilinx currently, and for the foreseeable future, does not have a solution bigger than 1 Mb. (Xilinx has released a commercial 16-Mb PROM, and work is under way to determine its radiation and temperature range characteristics, with the goal of releasing both military and radiation-tolerant versions of this part.) Table 5 shows the available options for such PROMs. Note that the TID level for configuration memories is significantly lower than the FPGA itself.

With Actel’s “one time programmable” FPGAs, there is no need for extra programming devices, resulting in lower in-system power consumption and a smaller footprint.

Table 5: Rad-Tolerant PROMs for Xilinx FPGAs; one time programmable (OTP), in system - programmable (ISP)

Device	Program-mability	TID (krad)	Configura-tion Bits (kb)	SEL (LET) (MeV cm^2/mg)	SEU	Supply Voltage (V)	Package	Avail.
XQR1701L	OTP One-time prog.	50	1048	No latch up for LET>120	No upset for LET>120	3.3	CC44	Now
XQR17V16	OTP One-time prog.	50	16,000	No latch up for LET>120	No upset for LET>120	3.3	CC44[1] VQ44[1]	Now
XQR18V04	ISP In-system prog.	30; 10 for the ISP Circuitry	4194	No latch up for LET>120	No upset for LET>120	3.3	CC44[1]	For existing designs only[2]

Notes:

1. CC 44: 44-pin ceramic chip carrier http://www.actel.com/products/aero/package, VQ44: 44-pin plastic thin quad flat package
2. Support for existing designs only; Xilinx does not encourage new designs with this part.

15. Package Quality Issues

For package availability, see Table 2. Other package quality issues are discussed below.

15a. Xilinx CGA Package

The issue with the Xilinx CGA 560 package is related to temperature cycling, which causes cracking of the column at around 1000–1500 cycles. The Virtex-II 3000 (XQ2V3000) only comes in 717/728 ball/column packages, which may have to be requalified if a ceramic package is used. Xilinx has released the hermetic CG717 and the flip chip nonhermetic FC1144 ceramic column grid packages, which have notably, better second- (broad) level reliability data, with the first failures occurring after thousands of temperature cycles.

15b. Xilinx Plastic Ball Grid Array (BGA) Package

The Xilinx plastic BGA package is suitable for use only in those applications where the column grid array (CGA) package is not acceptable due to temperature cycling considerations and on-board temperature control is not possible due to power or space limitations. The burn-in time of plastic BGA is a limiting factor. Xilinx recommends only 72 hours burn-in at 125 °C (with 12 hours of re-burn) because of BGA ball separation due to aging, although Xilinx performs accelerated testing (48 hours at 145 °C). Xilinx has subjected a large number of previous versions of BGAs to burn-in at 125 °C on printed wiring boards (PWBs) and have seen no failures. If the BGA package is used, it is necessary to require a long-time burn-in on representative samples from the flight lot in addition to the short burn-in (48 hours) for a 100% screening test and acceptance of flight units.

15c. Xilinx Flip-Chip Package

Xilinx is using a nonhermetic ceramic flip-chip package for the XQR2V6000. This is a new package style for which JPL has no data; it would require a mission risk assessment before being recommended for full or limited flight qualification. This package utilizes IBM technology with modifications, so some reliability data are available. Xilinx has informed JPL that they have just completed qualification of these packages and have demonstrated improved performance for thermal cycle for onboard package. JPL has requested a copy of the report.

15d. Xilinx CQFP Package

At this time, there are no reported issues with the CQFP 228 package used for Virtex 300 and 600.

15e. Actel Packaging Issues

There are four packages available for RTSX-S devices: the 208-pin, the 256-pin CQFP, the 256-pin land grid array/wire bond, and the CCGA624. The parts use gold bond wires. Previous-generation 0.6-µm RTSX parts exhibited bond pull failures in the 1999 time frame due to purple plague. This was first observed in hardware for a NASA Goddard Space Flight Center (GSFC) program, and subsequent detailed investigation by GSFC showed that parts from certain date codes exhibited the problem. (These older 0.6-µm RTSX devices have been discontinued.) Actel made some changes to the wire-bonding process in an attempt to eliminate the problem and have not seen any wire bond issues due to purple plague on the RT54SX-S devices. More recently there has been at least one case (in a destructive physical analysis [DPA] performed for a JPL subcontractor) when the bond pad lifted off the substrate, possibly due to overcompensating for the earlier problems. However, the devices marginally passed the wire pull criteria, and the specific lot passed the DPA criteria. If a program is concerned about the gold bond wires, they should procure the E-Flow screened devices that are intended for flight and provide greater control for wire bond reliability monitoring.

The RTAX1000S and RTAX2000S are available in a ceramic column grid array (CCGA) package similar to the Xilinx CCGA. It is expected that the CCGA would have much lower solder joint reliability compared to plastic and leaded versions. Actel uses aluminum wire bonds on the RTAX-S family, so there should be no wire-bond problems similar to those seen on the older RTSX devices.

16. Screening

The level a project plans to use determines which screens are not performed and the risk level associated with screening deficiencies. Comparatively, Actel E-flow is better than the Xilinx QPro-plus flow because it is closer to QML V-level. Table 6 compares the Actel E- and B-flows and the Xilinx QPro-plus flow. All tests listed are 100% screens unless otherwise noted. SMDs are available for both the rad-hard and military versions of Virtex FPGAs. Virtex-II rad-hard and military SMDs have been submitted to DSCC for approval. Xilinx was previously audited by DSCC and the Defense Threat Reduction Agency (DTRA) for the manufacture and issuance of rad-hard SMDs and found suitable.

Table 6: Xilinx QPro Plus and Actel E-flow Comparison

Operation	Xilinx QPro-Plus	Actel E-Flow
Internal Optical Inspection	per Method 2010 Condition B	Internal Visual per 2010 Condition A
Final Visual/Mech. Inspection	Per 5004	Per 2009
Temperature Cycling	Per Method 1010 condition **C**	Per Method 1010 condition C
Constant Acceleration	Per Method 2001, condition E	Per Method 2001 condition D or E
Radiographic	Per Method 2012	Per 2012
Fine/Gross Leak Test	Per Method 1014	Per Method 1014
Pre Burn-in Electrical Test at 25˚C	Per part drawing	Per specification
Burn-in	Per Method 1015 240 hours equivalent Static /Dynamic BI	Per Method 1015 Dynamic blank Burn-in 240 hours at 125°C
Reverse Bias Burn-In	n/a	72 hours at 150 °C
Electrical Test at Room Temp	Per part drawing Per 5004 or SMD	Per 5004
Percent Defective Allowable	5%	5%
+125˚C Electrical Test	Per part drawing or SMD Per 5004	Per 5004
–55˚C Electrical Test	Per part drawing or SMD	Per 5004
External Visual Inspection	Per Method 2009	Per 2009
QC Sampling Plan	Per 5005;Group A,B,C and D	n/a

16a. Actel Flows

Actel offers two flows for their HiRel FPGA: B-flow (MIL Std-883) and E-flow (Extended flow). The E-flow includes X-ray, serialization, and read-and-record electrical parameters with deltas. The SMDs for RT54SX-S devices include parts that are still technically Class Q, but have additional testing, including Condition-A internal visual, X-ray, and read-and-record electricals with delta calculations.

Actel FPGAs should be procured based on the SMD numbers shown in Table 7. (The complete number depends on package, screening flow, and speed option.)

Table 7: Actel RTSX Product

Device	Foundry	SMD#	Packaging	Screening Flow
RT54SX32S	MEC	5962-01508	CQ208/256	B, E
RT54SX72S	MEC	5962-01515	CQ208/256, CG624	B, E
RTSX32SU	UMC	5962-01508	CQ208/256	B, E
RTSX72SU	UMC	5962-01515	CQ208/256, CG624	B, E

16b. Xilinx Flows

The SMDs currently available for Xilinx Virtex rad-tolerant products are shown in Table 8.

Table 8: Xilinx Rad-Hard Virtex-II Product

Device	Foundry	SMD#	Packaging	Screening Flow
XQVR300	UMC	5962-99572	CB228	QPRO plus
XQVR600	UMC	5962-99573	CB228	QPRO plus
XQVR1000	UMC	5962-99574	CG560	QPRO plus

There are not yet any SMDs for Virtex-II. Xilinx parts should be procured to "QPro-plus" flow (V suffix on Xilinx part number), which includes 100% particle impact noise detection (PIND) and lot sample DPA and radiographic inspection. Plastic packaged parts (see 15b) will require additional screening, and special screening may be recommended for the flip-chip package after review of available data.

17. Actel and Xilinx FPGA Upgrade Screening

Both Actel and Xilinx are against after-market screening for reliability, claiming it is not a good way to weed out infant mortality in faulty products. Both Actel and Xilinx screen their unprogrammed devices with various military and space standard tests throughout the production phase. However, there is evidence that additional screening of Actel devices after programming may detect defects related to the programming process. For Xilinx FPGAs, unlike Actel FPGAs, there is no permanent physical change introduced by programming, so post-programming testing is not necessary. However, the one-time programmable PROMs should be subjected to a three-temperature electrical test after programming.

18. Design Tool Quality

Both Actel and Xilinx have comprehensive design tool systems. Actel offers the Libero Integrated Design Environment (IDE) development tool, which includes a design manager tool that guides the designer through the design process, keeps track of design files, and seamlessly manages file exchanges between the various tools.

Xilinx offers their Integrated Software Environment (ISE), which is easy to use and comes in four configurations offering simplified design flow 2× faster than ASIC flows. They have optional design tools that tackle everything from HDL simulation to embedded systems design. Xilinx also offers a TMR tool (XTMR), which is a fully released and supported software program (see earlier notes on TMR tool). Whether a designer uses Actel's Libero IDE or Xilinx's ISE, both software tools are sufficient to develop a design from beginning to end.

19. Other Available FPGA Options for Space Applications (Aeroflex and Atmel)

Aeroflex Colorado Springs is planning to offer a rad-hard Eclipse FPGA family on 0.25-µm five-layer metal, using the ViaLink™ epitaxial CMOS process with guaranteed radiation performance and embedded rad-hard SRAM (See Table 9). For prototyping, Aeroflex offers the rad-hard Eclipse or QuickLogic commercial devices in plastic packages. Qualification is in progress. Table 10 shows the only rad-hard FPGA offered by Atmel.

Table 9: Aeroflex Rad-Hard FPGAs

Device	Core Voltage (V)	I/O Supply (V)	System Gates	# of SEU Immune Dedicated FFs	Package Availability	SMD#	TID (krad)	Cost ($/100 pcs.)	Available Flow
Eclipse UT6250	2.5	2.5/3	250K	3072	208/288 CQFP and 484 CCGA	5962-04229	300	4,700	Q, V
Eclipse UT6325	2.5	2.5/3	320K	3072	208/288 CQFP and 484 CCGA	5962-04229	300	4,700	Q, V

Table 10: Atmel Rad-Hard FPGAs

Device	Core Voltage (V)	I/O Supply (V)	System Gates	# of SEU-Immune Dedicated FFs	Package Availability	SMD#	TID (krad)	Cost ($/10–24 pcs.)	Available Flow
AT40KEL040	3.3	3.3	50K usable ASIC gates	3048	MQFPF160	5962-0325001	200	7200(Q) 10500(V).	Q, V

20. Technology Evolution in the Near Term

Xilinx future high-reliability Virtex FPGAs include HiRel Virtex-II Pro and Virtex 4, which feature up to four PowerPCs embedded on the FPGA.

The ProASIC PLUS family, Actel's second-generation of flash-based FPGAs, consists of six devices ranging in density from 150,000 to 1,000,000 system gates. The combination of a fine-grained, ASIC-like architecture and nonvolatile flash configuration memory makes Actel's ProASIC PLUS offering a strong ASIC alternative. The devices are live at power up and highly secure, and they require no separate configuration memory—all characteristics shared by ASICs. The ProASIC PLUS architecture and design methodology support popular FPGA and ASIC tool flows, reducing time-to-market and permitting designers to migrate easily between FPGA and ASIC solutions. New features of the ProASIC PLUS family include multiple phase-locked loops (PLLs) supports for up to 198 kb of two-port embedded SRAM and 712 user-configurable I/Os, as well as improved, in-system programmability.

21. Summary

Recommendations for FPGA selection will vary depending on the details of the particular application for which the FPGA is intended. There are many respects in which one of the technologies is superior to the other, but the differences do not point to a single solution. For each application, the designer will need to make a decision based on the various factors discussed in this report and their relative importance for his or her particular needs.

Applications now planning to use the RTSX-S (MEC) parts may wish to switch to the pin-compatible RTSX-SU (UMC) parts. The RTSX-SU devices are form, fit, and functionally compatible with the RTSX-S parts, and meet the same timing limits as the RTSX-S parts.

- RT5SX32S may be replaced by RTSX32SU.
- RTSX72S may be replaced by RTSX72SU.
- Designers considering use of Xilinx parts should note that SEU mitigation is not built in as it is in the RT54SX-SU, so the designer must incorporate it. SEUs can corrupt the configuration and therefore the functionality of the Xilinx parts, not just data, and mitigation strategies need to account for this. The Xilinx parts are not pin compatible with the Actel parts, and designers should also account for additional board space and power consumption needed for configuration memory, and possibly reconfiguration hardware as well. It is still a judgment call on whether the benefits (mostly in number of gates and auxiliary features, like clock managers and hardware multipliers) are worth it in the absence of a pressing need for reconfigurability.

These recommendations will be updated as additional data becomes available. For the latest information, consult the FPGA specialists in the JPL Parts Engineering Group.

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Acronym List and Glossary

ASIC	application-specific integrated circuit
ASSP	application-specific standard product
BGA	ball grid array
BRAM	block RAM
CCGA	ceramic column grid array
CGA	column grid array
CMOS	complementary metal oxide semiconductor
CQFP	ceramic quad flat pack
DPA	destructive physical analysis
DSCC	Defense Supply Center Columbus
DSP	digital signal processing
DTRA	Defense Threat Reduction Agency
EDAC	error detection and correction
FF	flip flop
FPGA	field-programmable gate array
GIDEP	Government and Industry Data Exchange Program
GSFC	NASA Goddard Space Flight Center
HDL	hardware description language
IND	integrated design environment
ISE	integrated software environment
JTAG	A test architecture developed by the Joint Test Action Group and later adopted by IEEE as the IEEE Standard Test Access Port and Boundary-Scan Architecture (also referred to as IEEE Std. 1149.1)

LET	linear energy transfer
LUT	look-up table
MEC	Matsushita Electronics Corporation
Method 1019.5	Ionizing Radiation (Total Dose) Test Procedure (MIL-STD-883)
POR	power on rest
PROM	programmable read-only memory
purple plague	A brittle gold aluminum compound formed when bonding gold to aluminum. The growth of such a compound can cause failure in microelectronic interconnection bonds.
PWB	printed wiring board
QML	qualified manufacturing line
RHA	radiation hardness assurance
RH	radiation hardened
RT	radiation tolerant
SEFI	single-effect functional interrupt
SEL	single-event latchup
SEU	single-event upset
SMD	source manufacturing drawing
SRAM	static random access memory
TID	total ionizing dose
TMR	triple module redundancy
TRST	test logic reset
UMC	United Microelectronics Corporation
PWB	printed wiring board
PIND	particle impact noise detection
PLL	phase-locked loops
XTMR	Xilinx triple module redundancy