Technology Readiness Overview: Ball Grid Array and Chip Scale Packaging

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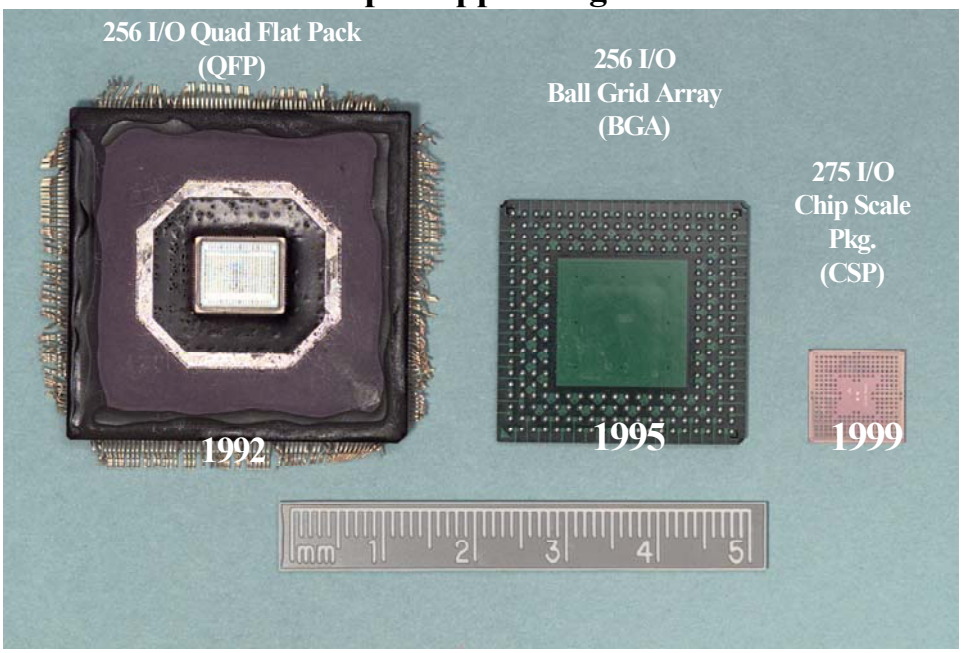

January 2003

Overview of BGA and CSP Packaging Technology for Spaceflight Missions

This document provides an overview for designing, manufacturing, and testing printed wiring assemblies populated with ball grid arrays (BGA) and chip scale packages (CSPs). NASA Headquarters, Code AE and Code Q, has funded numerous tasks for the last several years to investigate the use of BGAs and CSPs for potential spaceflight missions.

The objectives of the NEPP (NASA Electronic Parts and Packaging) Program area array (BGA and CSP) projects were to evaluate the quality and reliability of these technologies and to assist in the development of the rapidly growing associated industrial infrastructure. This was successfully accomplished by organizing industry-wide consortia, led by the NEPP Program to address many issues with this technology. The principal investigator, as chairperson and in collaboration with industry, released findings in 2002 as industry qualification specification, IPC 9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments". This was published by IPC, Association Connecting Electronics Industries.

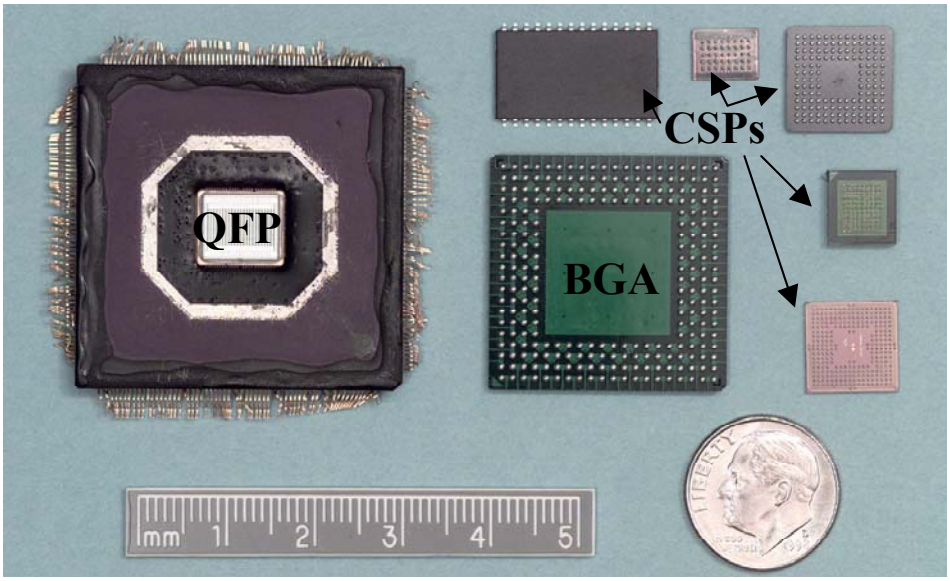

Figure 1 Miniaturization trends in surface mount electronics packaging, from quad flat pack (QFP) to ball grid array (BGA) and chip scale package (CSP)

Figure 1 compares a conventional leaded package with BGA and smaller configuration CSPs. BGAs with 1.27 mm pitch (distance between adjacent ball centers) are the only choice for packages with higher than 300 I/Os (input/output) count, replacing leaded packages such as the quad flat pack (QFP) even for lower I/Os. The area array packages also provide improved electrical and thermal performance, more effective manufacturing (improved manufacturability), and ease-of-handling compared to the conventional surface mount (SMT) leaded parts.

CSPs (a.k.a fine pitch BGAs, FPBGAs) are further miniaturized versions of BGAs, leaded, and leadless packages with pitches less than 1.27 mm. These electronic packages have low mass and small chip sizes, and are generally used for low I/Os (<100) for memory and have the potential

for use for higher (>300) I/Os. They also provide improved electrical and thermal performance, more effective manufacturing, and ease-of-handling compared to the conventional surface mount leaded parts such as thin small outline packages (TSOPs). However, there are some issues (mainly inspection and reliability) with the implementation of the new area array packages for high reliability applications.

Advantages of BGA

BGAs offer several distinct advantages over fine pitch surface mount components having gull wing leads, including:

- High I/O capability, 100s to 1000s balls can be build and manufactured, but gull-wing leads are limited to less than 300 I/Os
- Larger lead pitches, which significantly reduces the manufacturing complexities for high I/O parts
- Higher packaging densities are achievable since the lead envelope for the gull wing leads is not applicable in the case of BGAs; hence, it is possible to mount more packages per board, i.e., higher packaging density
- Faster circuitry speed than gull wing SMCs (surface mount components) because the terminations are much shorter and therefore less inductive and resistive
- Better heat dissipation
- Conventional SMT production technologies such as stencil printing and component mounting can be employed

The BGAs are also robust in processing. This stems from their higher pitch (1.27 mm , 0.050", typical), better lead rigidity, and self-alignment characteristics during reflow processing. This latter feature, self-alignment during reflow (attachment by heat), is very beneficial and considerably opens the process window.

Disadvantages of BGAs

BGAs, however, are not compatible with multiple solder processing methods, and individual solder joints cannot be inspected and reworked using conventional methods. In ultra low volume SMT assembly applications, the ability to inspect the solder joints visually has been a standard inspection requirement and is a key factor for providing confidence in the solder joint reliability. Advanced inspection techniques including X-ray need to be developed to provide such confidence for BGA and FPBGAs.

The four chief drawbacks of both BGAs and FPBGAs are similar. These are:

- Lack of direct visual inspectability
- Lack of individual solder joint reworkability
- Interconnect routing between the chip and the PWB necessitates a multilayer PWB

- Reduced resistance to thermal cycling due to use of rigid balls/columns

BGA Types

Examples of typical BGA packages are shown in Figure 2. These include plastic ball grid array with ball composition of eutectic 63Sn/37Pb alloy or slight variation. The ceramic BGA package uses a higher melting ball (90Pb/10Sn) with eutectic attachment to the die and board. Column grid array (CGA or CCGA) is similar to BGA except it uses column interconnects instead of balls. Flip chip BGA (FCBGA) is similar to BGA, except it is internal to the package and flip chip die is used.

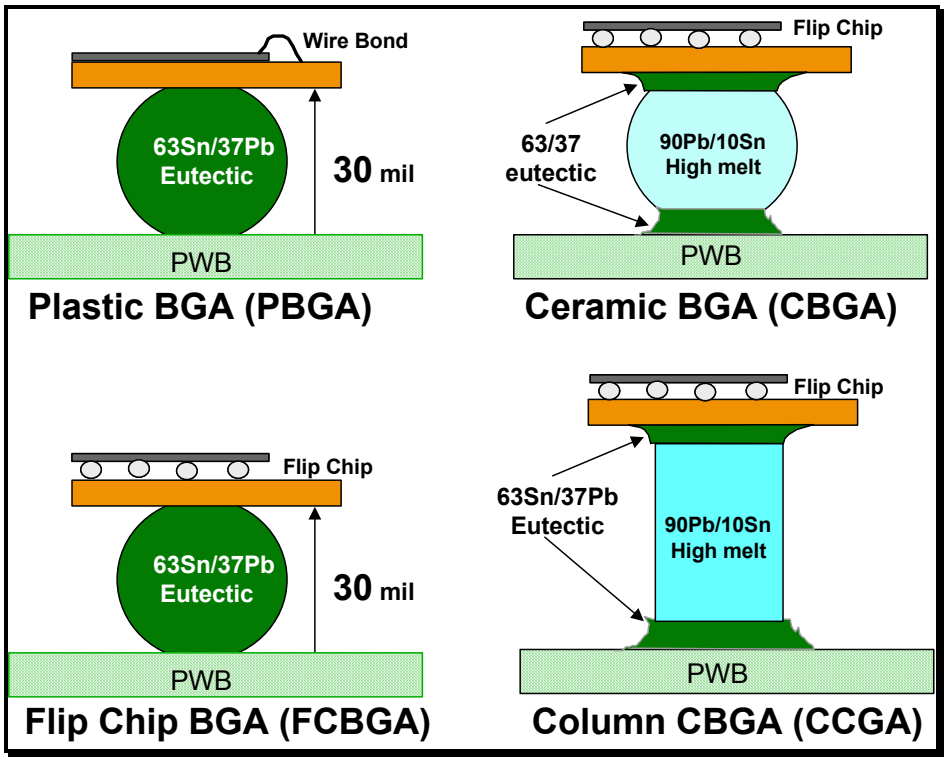

Figure 2 Plastic and ceramic package configurations

Key Recommendations for BGA Qualification/Implementation

The key disadvantages of BGAs remain the same, i.e., inspectability for interconnection cracks and individual ball reworkability. Only peripheral balls/columns can be inspected easily. Even though progress has been made in improving resolution of X-ray for better inspection, the issue of inspection remains partially unresolved. The interconnections of plastic BGA mounted to polymeric circuit boards are generally more reliable under thermal cycling when compared to ceramic BGA packages mounted to polymeric circuit boards. This is due to a closer match in the materials' coefficient of thermal expansion (CTE). For long missions with high reliability requirements such as Mars 05 and Mars Smart Lander, plastic packages may be the only choice for good resistance to thermal cycling.

All BGAs and almost all CGAs are commercial-off-the-shelf (COTS) packages. The issues with COTS for BGAs are the same as other COTS issues and include: package die source and materials variations from lot-to-lot, availability of packages with radiation hard die, moisture effect and popcorning for PBGAs, outgassing for materials, etc. Assembly related issues of BGAs have not been a problem.

Review of Chip Scale Package (CSP)

As mentioned previously, the trend is towards ever increasing I/Os on packages, and so this is driving the packaging element of semiconductors. Already chip scale packages (CSPs) are making their appearance. Unlike conventional BGA technology at typically 1.27 mm (0.050'') pitch, CSPs utilize lower pitches, e.g. currently 0.8 to 0.4 mm, and hence, will have smaller sizes and their own challenges.

CSPs are competing with bare die assemblies. CSPs provide the benefits of small size and performance of the bare die or flip-chip, with the advantage of standard die packages. Key advantages/disadvantages compared to bare die are listed in Figure 3. A photo comparing a wafer level CSP to QFP with the same I/O count, is shown in Figure 4. The tiny CSP is located at the center of the QFP, the CSP's bottom side with solder balls is apparent in photo.

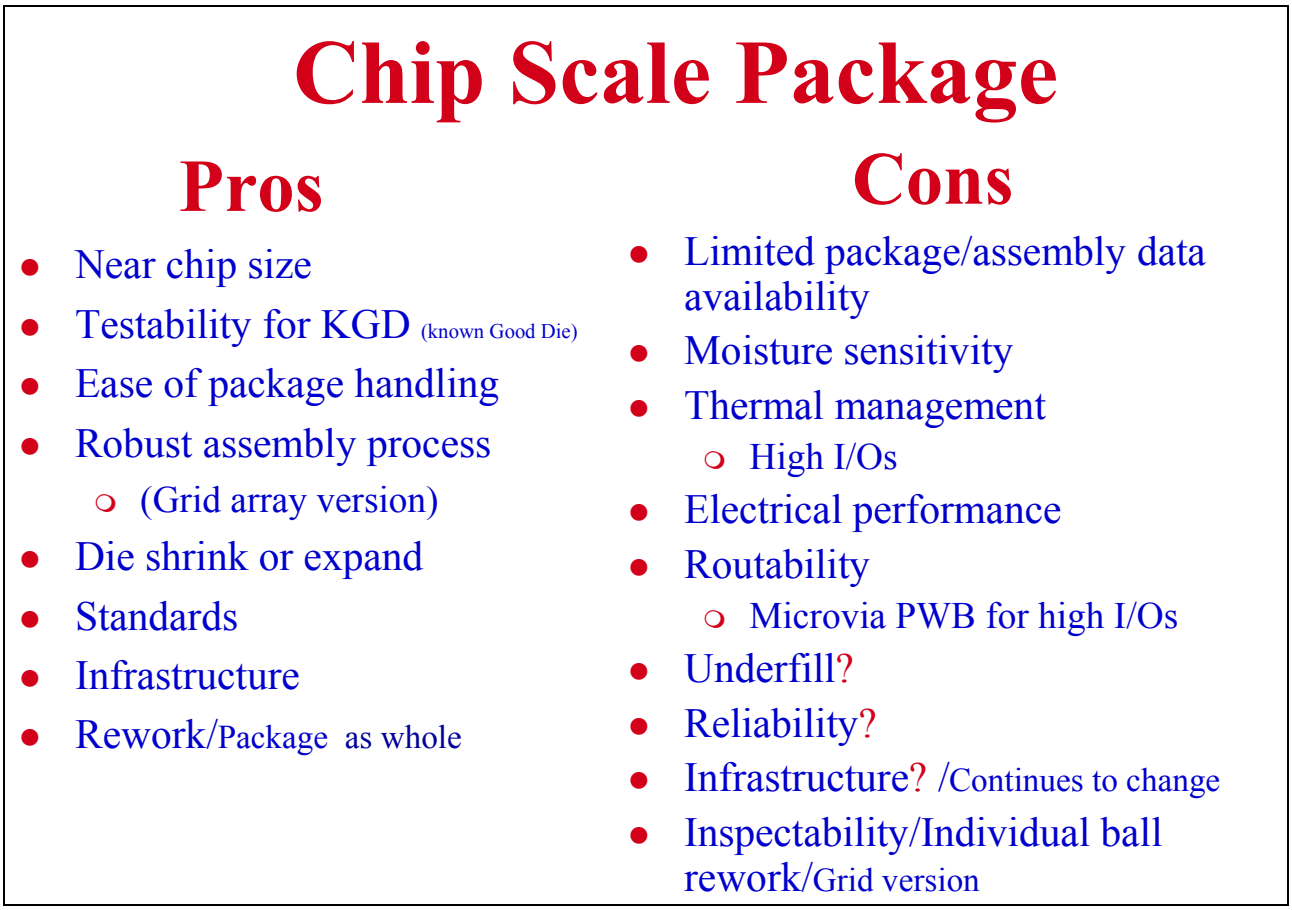

Figure 3 Pros and cons of chip scale package (CSP)

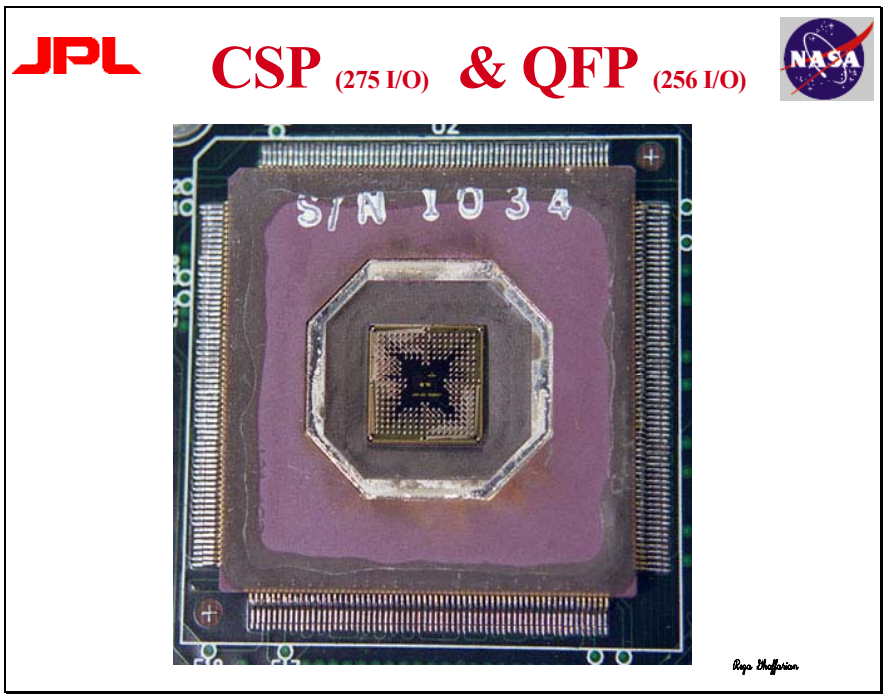

Figure 4 Size comparison of QFP with a wafer level CSP- same I/O

CSPs especially their area array versions, a.k.a FPBGAs, are now widely used for many electronic applications including portable and telecommunication products. The BGA version of the area array package, introduced in the late '80's and implemented with great caution in early '90's, was further evolved in the mid '90's to the CSP having a much finer pitch. Distinguishing between size and pitches has become difficult for the various array package versions. These are now categorized as area array packages in order to be able to distinguish them from the flip chip, bare die category. The bare dies have been around for a longer time, but their associated issues, including known good die and difficulty in direct attachment to printed wiring boards (PWBs), have limited their wide implementation.

The definition of CSP has evolved as the technology has matured and now refers to a package with 0.8 mm and less pitch. Current packages have as low as 0.4 mm pitch. Packages with fine pitches, especially those with less than 0.8 mm and high I/Os, may require the use of microvia PWBs are costly and may perform poorly when assembled onto these boards. One approach has been to increase function through systems-in-a-package technology, i.e., stacking die/packages while keeping the pitch within the limitation of current board technology.

CSP Implementation-Lessons Learned

This technology continues to emerge with new packages and smaller pitch. Thus it is more challenging for use in high reliability space applications. Each individual package needs to be evaluated for design, construction, materials, ball shear, moisture, etc. prior to acceptance and

evaluation for 2nd level assemblies, IPC 9701 should be used as a guideline for solder joint qualification.

Lessons learned from NEPP Program and Code Q task activities on CSPs are as follows:

- CSPs continue to be developed by industry. Many issues including detailed design information on the packages may not be available.
- Standardize on metric units for BGA, especially for CSP. Significant error information is introduced when converting from one unit of measurement to the other if sufficient digit accuracy is not considered.
- Use a non-solder mask defined (NSMD) pad configuration, i.e. allowing a gap between the pad and solder mask, since it has been shown that when the mask contacts solder, it could initiate solder joint cracking and therefore degrade BGA assembly reliability. This is now included in IPC 9701.
- The assembly process is very insensitive to solder paste volume. There was no obvious difference on the ease-of-assembly for 4 mil, 6 mil and 7 mil thick stencils.
- Use different aperture sizes, rather than a step-down stencil, if there is a requirement for solder volume variation. It has been demonstrated that using a step-down stencil can introduce other operation-related variables into the soldering process
- BGAs and FPBGAs align themselves during the reflow process and therefore are more robust than fine pitch leaded packages.
- Mixed technology assembly may not easily permit the use of optimum solder volume to achieve the highest reliability. This is also true for a surface mount mixture of fine pitch and leadless packages. Assembly becomes more challenging with the addition of leadless CSPs.
- Traditionally, solder joint failure was considered to be the weakest link of microelectronics attachment reliability. This may not be true for CSPs with innovative designs and use of new materials and processes. For example, an internal package TAB (tape automated bond) lead bond failure was considered to be the possible cause of a CSP failure after cycling. Therefore, understanding the overall philosophy of testing to meet system requirements, as well as detecting new failure mechanisms associated with the miniaturized CSPs is a key to collecting meaningful test results.
- Literature data indicate that a shift in failure from the solder joint to the package may occur more often with miniaturized CSP packages. A projection, based on the wrong failure mode may result in a wrong forecast of life.
- Literature data indicate that the board level cycles-to-failure of most CSPs, with less than 50 I/Os, are comparable to or better than LCCCs (Leadless Ceramic Chip Carriers) with a similar I/O count. CSPs, however, are not as robust in board level reliability as conventional SM leaded packages, including gull wing and J-lead packages. In a few cases, they might have comparable board reliability to their TSOP counterparts.
- The best CSP package assembly had cycles-to-failure reliability of 30% or less than plastic ball grid arrays. Ceramic CSP assemblies had similar or higher reliability compared to their ceramic ball grid array versions.

- Visual inspection has been the most common method to characterize solder quality and reject nonconformance to specification for space missions. Inspection for acceptance is still a challenge for BGAs. The challenges are further magnified for the inspection of CSPs with small features and hidden solder joints. Stringent process controls in conjunction with non-destructive characterization tools such as micro focus x-ray must be used to mitigate risk for space applications.
- The effects of underfill on cycles-to-failure may be positive, neutral, or negative depending on package types. It improved the reliability of leadless package, was neutral for chip-on-flex, and had negative effects on the TAB CSP reliability.
- Failure mechanisms may shift to the weakest package assembly sites (PWB/solder/package internal) when solder failure is prevented by underfilling. The TAB CSP failure shifted to the internal package and TSOP and Leadless package assemblies failed at in-pad microvias, filled or unfilled with solder.

Recommendations for BGA/CSP Qualification and Flight Implementation

Qualification and verification steps for BGA and CSP packages for various NASA missions are summarized below. Prior to design, it is recommended to review industry standards on this subject including IPC 7095, "design and assembly process implementation for BGA", and IPC 9701 (for a copy, please order through IPC, http://www.IPC.Org). If you need additional assistance or have specific questions, please contact this author.

Recommendations for NASA mission implementation are as follows:

- Define the overall NASA mission environmental requirements including radiation, mechanical, thermal, life cycle, etc.
- Define appropriate potential package technology and types including BGA, CGA, CSP, I/O, build up, materials, solder geometry and materials, heat distribution, etc.
- Determine if package properties are within the envelope of mission environmental requirements in order to avoid early overstress failures. Examples are: radiation capability of die, temperature limits of package materials including softening temperature (glass transition temperature, Tg) and junction temperature.
- For life thermal cycle qualification, determine life cycle requirements for mission. The life cycle requirement shall be three (3) times the realistic worst-case life consumption including ground test.
- For the purpose of further narrowing package selection, consider the following four categories of NASA missions.
    - A: Benign thermal cycle exposure with short mission duration
    - B: Benign thermal cycles with long mission duration
    - C: Extreme thermal cycles with short mission duration
    - D: Extreme temperature cycle exposure with long mission duration
- If details on life cycle requirements are not available, then use the following rules-of-thumb to estimate the number of accelerated thermal cycles for the NASA missions.
    - For the A and B missions, thermal life cycle requirements are estimated to vary from 100 to 500 NASA accelerated cycles (-55°C/100°C).
    - For the C and D missions, estimate the flight allowable temperature ranges plus the ground exposure and multiply mission life cycles by 3.
- Review heritage/vendor data for BGA/CSP packages. Use the following generic guidelines for meeting the requirements.
    - Most plastic BGAs on polymeric circuit boards have sufficient life cycles to meet the A and B NASA mission categories. Plastic packages with very large die may be required to be

qualified for use under the B category. Low I/O ceramic packages (<400 I/Os) may have sufficient life for the A, but should be verified for the B category missions. High I/O ceramic packages (>500 I/Os) may not meet either A or B mission categories.

- Most BGA packages may be required to be qualified when they are considered for the C and D mission categories.
- Most ceramic and plastic CSPs may meet the A mission category requirements. CSPs may be required to be qualified for the B, C, and D mission categories.

- Use the following guidelines when review of heritage data indicates that package qualification and verification is required.
  - Use a daisy chain package as the test article for accelerated thermal cycle tests. Daisy chain packages are generally built using similar materials and layup as the functional package with the exception of using a dummy die with even/odd pad connections. Die size affects solder joint reliability and therefore should be the same size or larger than the flight-like package.
  - PWB design considerations:
    - Design in local fiducials, especially for CSPs. Use NSMD for pad design. Include microvia and buried build-up technology if they are used in the flight PWB design. Note that PWB thickness affects solder joint reliability. Balance the board to avoid PWB warpage. Control warpage by specification and verify by measurement.
    - Design double-sided assembly if it mimics flight configuration. Double-sided, mirror image, assemblies show major reduction in solder joint reliability.
    - Use hot air solder leveling (HASL) surface finish and avoid immersion gold on Ni or other exotic finishes.
    - For inspection/rework purposes, allow enough clearance (0.15 inch) for optical inspection/rework.
  - Package assembly considerations:
    - Follow the guideline documents for package/PWB preparation, e.g., assure that BGA/CSP balls have sufficient package attachment shear strength, perform wettability test for ball/PWB, bake PWB and packages prior to assembly, etc.
    - BGAs and most CSPs are robust in assembly and will self-align during reflow.
    - Optimize your reflow thermal profile, especially for a mixed technology assembly. Remember that process optimization and process control are key parameters that control solder attachment integrity, not optical/visual inspection, as commonly used for most other electronic packages at NASA. Use of an RMA (rosin mildly activated) flux is recommended, measure paste release consistency, and clean after assembly.
    - Perform real time X-ray and optical inspection if possible. Use of an X-ray machine with laminography capability is recommended.
  - For environmental test, use a continuous monitoring system to detect electrical interruptions as detailed in IPC9701. Remove at specified intervals for optical/visual inspection to

document damage progress. Use non-destructive and destructive techniques to confirm early failures or non-failures at the end of qualification.

- Use of underfill is not recommended for BGAs, but may be required for CSPs. Select an underfill that has a close CTE match to the PWB. If no heritage data is available, then the underfilled packages must be qualified since their effects on reliability cannot be extrapolated from one package to another. Do not consider underfilling packages with large gaps such as CGA or very fine gaps such as thin and ultrathin CSPs.
- For those mission environments where the part may be exposed to heavy ions resulting in single event effects (SEE) such as upset and latchup, note that these advanced packages may make it difficult to perform SEE testing at accelerators. Special steps may have to be taken in order to accomplish these tests. This is primarily due to the effects of packaging materials on the ion beam that the beam must go through in order to reach the part.

Summary

The key issues for BGAs and CSPs are:

1- There is no flight heritage data available yet.

2- BGAs and CSPs withstand fewer 2nd level (assembly) thermal cycles than their leaded counterparts. CSPs have lower life than BGAs.

3- Need to perform testing on dummy daisy chain package/board if in doubt about reliability, or if application requires ability to withstand significant thermal cycling.

4- A non-destructive inspection technique for interconnection cracks is not yet developed. Also, individual balls cannot be reworked.

5- Most packages are built for commercial applications and many issues with COTS BGAs/CSPs are similar to those encountered with conventional COTS microcircuits and their packages.

The interconnections of plastic BGAs mounted to polymeric circuit boards are generally more reliable under thermal cycling when compared to ceramic BGA packages mounted to polymeric circuit boards. This is due to a closer match in the materials' coefficient of thermal expansion (CTE). For NASA missions with relatively benign environments, most ceramic packages may be appropriate. For longer NASA missions, plastic packages better meet thermal cycle reliability requirements. Note, however, that COTS plastic encapsulated microcircuits may exhibit other reliability problems.

List of Acronyms

ACTS Advanced Communication Technology Satellite
BGA Ball Grid Array
CBGA Ceramic Ball Grid Array
CCGA Ceramic Column Grid Array
CGA Column Grid Array
COTS Commercial-off-the-shelf
CSPChip Scale (Size) Package
CTE Coefficient of Thermal Expansion
FCBGA Flip Chip Ball Grid Array
FPBGA Fine Pitch BGA, a.k.a. Chip Scale Package (CSP)
GALEX Galaxy Evolution Explorer
I/O Input/Output
IPC Association Connection Electronics Industries
KGD Known Good Die
LCCC Leadless Ceramic Chip Carrier
MER Mars Exploration Rover
MGS Mars Global Surveyor
MLS Microwave Limb Sounder
MSL Mars Smart Lander
NEPP NASA Electronic Parts and Packaging
NGST Next Generation Space Telescope
PBGA Plastic Ball Grid Array
PWB Printed Wiring Board
QFP Quad Flat Pack
SATS Small Aircraft Transportation System
SATS Small Aircraft Transportation System
SMT Surface Mount Technology
SORCE Solar Radiation and Climate Experiment
TAB Tape Automated Bond
TSOP Thin Small Outline Package