

Heavy-ion Single Event Effects Test of LSI Logic 0.18 μ m G12 process SRAM Test Vehicle

Test Report

NASA-GSFC, Radiation Effects and Analysis Group (REAG), Code 561

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1 Introduction

This report presents the heavy-ion SEE test results obtained on the SRAM test vehicles of the LSI-Logic 0.18 μm G12 processes (bulk and CMOS). These tests were performed in the frame of NASA Electronics Parts and Packaging (NEPP) program.

2 Tested devices

The device tested is a memory test chip (LXA0387). The memory test chip is a 512Kbit SRAM organized externally as 64K words of 8 bits. The minimum cycle time is about 50 ns, and the power supply voltage is 1.8V. A picture of the SRAM test chip is shown in Figure 1. A zoom of one corner of one of the two memory arrays is shown in Figure 2. The memory test chip is packaged in a 64 pin ceramic PGA package.

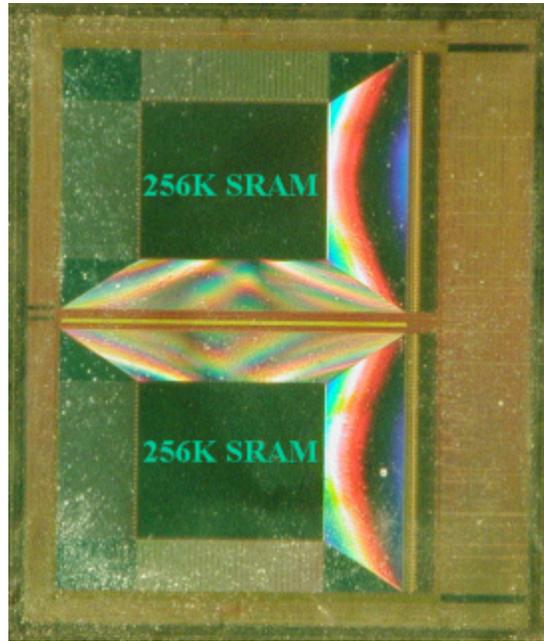


Fig 1: Picture of the SRAM die

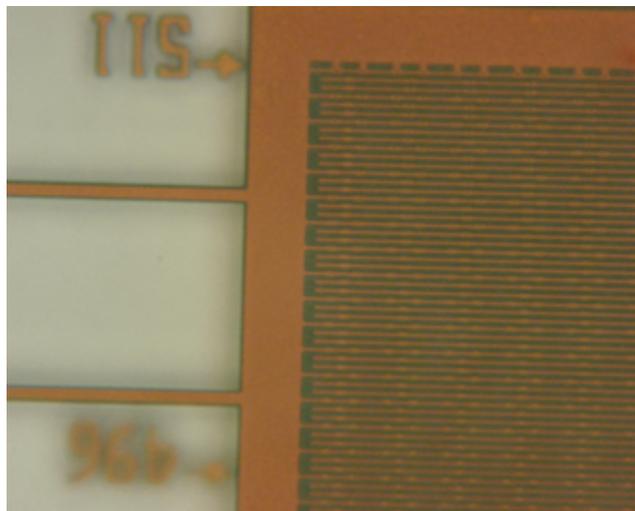


Fig 2: high magnification (x160) view of one corner of one memory array

Table 1 gives the information on the test sample provided by LSI-Logic. All test samples have been tested, read and record, by the manufacturer before shipping. Four parts from each process (SN1 to 4) have been delidded for Single Event Effect Testing.

Table 1: Test samples information

Process		Package	Package Marking	Sample Size
G12	Bulk	FA28 (ceramic PGA 64)	LSI Logic LXA0387 GAF49909.7 T036SEE4 EZG13002.1 ENGR SAMPLE G0414 ? Philippines	SN1to4 (delidded)
	SOI	FA28 (ceramic PGA 64)	LSI Logic LXA0387 GAF33921.2 A027WSD6 EZG13003.1 SOI ENG SAMPLE G0414 ? Philippines	SN1to4 (delidded)

3 Test Description

3.1 Irradiation Facility

The tests have been performed at the Texas A&M particle accelerator on June 3, 2004. Irradiation has been performed in Air. The distance of Air between the ion beam output and the Device Under Test (DUT) was 6 cm. The characteristics of beams used are given in Table 2. The LET and ranges values given in Table 2 are the LET and range on the DUT, the target, after 6cm of Air and the 25.4 μ m Aramica window.

Table 2: Characteristics of ions used at TEXAS A&M

Ion	Energy (MeV/u)	Energy at target (MeV)	LET at target (MeVcm ² /mg)	Range at target (? m)
Xe	15	1291	53.9	102
Kr	15	912	29.3	116
Ar	15	496	8.7	174
Ne	15	266	2.8	261

3.2 Test set-up and bias conditions

The SRAM test vehicles were tested with a specific test set-up developed at NASA-GSFC. Two different test modes were investigated:

- static test: a test pattern is loaded in the DUT before irradiation, and then checked after the irradiation.
- dynamic test: a test pattern is loaded in the DUT before irradiation. During irradiation the DUT is continuously read.

For both test modes the detected errors were recorded for further analysis. Four different test patterns were tested: all 0, all 1, checkerboard, and reverse checkerboard.

The Power supply currents of the DUT were monitored and charted during irradiation to detect the occurrence of SEL or other anomalous condition. In case of SEL, the set-up shutdown the DUT power supply. The SEL detection threshold was set to 1 mA for the memory core power supply and to 20 mA for the I/O and periphery power supplies.

During irradiation the DUT was biased at the nominal power supply of 1.8V (Vdd2) and operated at the frequency of 1 MHz. The total nominal current was lower than 1 mA.

4 Test Results

The test results are shown in Table 3.

Table 3: Test Results

Run #	Type	SN #	Pattern	Test Mode	Ion	Tilt	eff LET (MeVcm ² /mg)	eff. Fluence (#/cm ²)	SEU #	Xsection SEU (cm ² /bit)	SEL #	Xsection SEL (cm ² /device)	Comment
2	SOI	1	check	read dynamic	Xe	0	53.9	3.37E+04	335	1.90E-08	0	0.00E+00	
3	SOI	1	check	static	Xe	0	53.9	6.39E+04	696	2.08E-08	0	0.00E+00	
4	SOI	1	/check	read dynamic	Xe	0	53.9	2.96E+04	290	1.87E-08	0	0.00E+00	
5	SOI	1	/check	static	Xe	0	53.9	6.08E+04	626	1.96E-08	0	0.00E+00	
8	SOI	1	all1	read dynamic	Xe	0	53.9	3.60E+04	375	1.99E-08	0	0.00E+00	
9	SOI	1	all1	static	Xe	0	53.9	6.50E+04	700	2.05E-08	0	0.00E+00	
10	SOI	1	all0	read dynamic	Xe	0	53.9	6.14E+04	652	2.03E-08	0	0.00E+00	
11	SOI	1	all1	read dynamic	Xe	45	76.2	4.71E+04	599	2.43E-08	0	0.00E+00	
12	SOI	1	all1	static	Xe	45	76.2	8.20E+04	816	1.90E-08	0	0.00E+00	
13	SOI	1	check	read dynamic	Xe	45	76.2	5.69E+04	499	1.67E-08	0	0.00E+00	
14	SOI	1	check	static	Xe	45	76.2	4.91E+04	443	1.72E-08	0	0.00E+00	
15	SOI	2	all1	dynamic	Xe	0	53.9	7.39E+04	767	1.98E-08	0	0.00E+00	
16	SOI	2	all1	static	Xe	0	53.9	5.64E+04	683	2.31E-08	0	0.00E+00	
17	SOI	2	all1	dynamic	Xe	45	76.2	4.69E+04	658	2.68E-08	0	0.00E+00	
18	SOI	2	all1	static	Xe	45	76.2	4.05E+04	570	2.68E-08	0	0.00E+00	
19	bulk	1	all1	static	Xe	0	53.9	2.25E+03			1	4.44E-04	I _{SEL} =160mA, I/O supply
20	bulk	1	all1	static	Xe	0	53.9	1.28E+03			1	7.81E-04	I _{SEL} =94 mA, I/O supply
21	bulk	1	all1	static	Ne	0	2.8	5.00E+05	2529	9.65E-09	0	0.00E+00	
22	bulk	1	all0	static	Ne	0	2.8	2.31E+05	1111	9.17E-09	0	0.00E+00	
23	bulk	1	all1	dynamic	Ne	0	2.8	1.98E+05	933	8.99E-09	0	0.00E+00	
24	bulk	1	all1	dynamic	Ne	50	4.3	1.04E+05	853	1.56E-08	0	0.00E+00	
25	bulk	2	all1	dynamic	Ne	0	2.8	1.12E+05	559	9.52E-09	0	0.00E+00	
26	bulk	2	all1	dynamic	Ne	50	4.3	5.28E+04	419	1.51E-08	0	0.00E+00	
27	SOI	1	all1	dynamic	Ne	0	2.8	5.27E+05	1926	6.97E-09	0	0.00E+00	
28	SOI	1	all1	static	Ne	0	2.8	1.27E+05	516	7.75E-09	0	0.00E+00	
29	SOI	1	all0	static	Ne	0	2.8	1.05E+05	414	7.52E-09	0	0.00E+00	
30	SOI	1	all1	dynamic	Ne	50	4.3	6.84E+04	374	1.04E-08	0	0.00E+00	
31	SOI	2	all1	dynamic	Ne	0	2.8	1.51E+05	623	7.87E-09	0	0.00E+00	
32	SOI	2	all1	dynamic	Ne	50	4.3	7.16E+04	440	1.17E-08	0	0.00E+00	
33	SOI	2	all1	dynamic	Ar	50	13.5	1.30E+06	7827	1.15E-08	0	0.00E+00	
34	SOI	2	all1	dynamic	Ar	50	13.5	6.49E+04	423	1.24E-08	0	0.00E+00	
35	bulk	1	all1	static	Ar	50	13.5	1.62E+06			0	0.00E+00	SEL test only
36	bulk	1	all1	dynamic	Ar	50	13.5	7.86E+04	787	1.91E-08	0	0.00E+00	
37	bulk	1	all1	dynamic	Ar	0	8.7	6.63E+04	482	1.39E-08	0	0.00E+00	
38	bulk	1	all1	static	Kr	0	29.3	5.64E+04			1	1.77E-05	I _{SEL} =80 mA, I/O supply
39	bulk	1	all1	static	Kr	0	29.3	3.44E+03			1	2.91E-04	I _{SEL} =93 mA, I/O supply
40	bulk	1	all1	static	Kr	0	29.3	1.11E+04			1	9.01E-05	I _{SEL} =83 mA, I/O supply
41	SOI	1	all1	dynamic	Kr	0	29.3	4.23E+04	300	1.35E-08	0	0.00E+00	
42	SOI	1	all0	dynamic	Kr	0	29.3	5.01E+04	385	1.47E-08	0	0.00E+00	
43	SOI	1	all1	dynamic	Kr	40	38.2	5.17E+04	471	1.74E-08	0	0.00E+00	
44	SOI	1	all1	dynamic	Kr	50	45.6	5.00E+04	498	1.90E-08	0	0.00E+00	
46	SOI	2	all1	dynamic	Kr	0	29.3	5.00E+04	324	1.24E-08	0	0.00E+00	
47	SOI	2	all0	dynamic	Kr	0	29.3	6.47E+04	416	1.23E-08	0	0.00E+00	
48	SOI	2	all1	dynamic	Kr	40	38.2	4.22E+04	371	1.68E-08	0	0.00E+00	
49	SOI	2	all1	dynamic	Kr	50	45.6	3.98E+04	334	1.60E-08	0	0.00E+00	

Fig 1 shows the SEU cross-sections. The bulk devices were sensitive to Single Event Latchup (SEL) at a LET of 29.3 MeVcm²/mg; therefore, no SEU characterization was possible on bulk devices for LET higher than 29.3 MeVcm²/mg.

The maximum SEU cross-section for the SOI devices is about 3E-08 cm²/bit. At low LET, bulk devices have a similar sensitivity as the SOI devices. For both SOI and bulk devices, there is no significant effect of the test method or the test pattern on the SEU sensitivity.

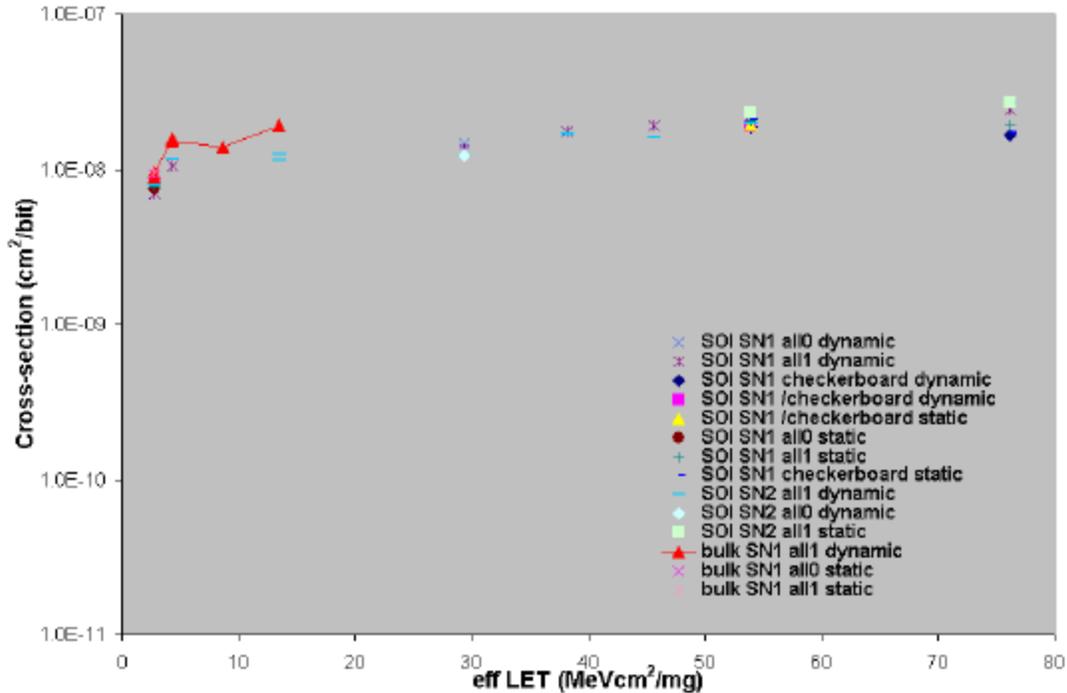


Fig 1: SEU cross-section

The SOI devices are not sensitive to SEL up to the maximum tested LET of 76 MeVcm²/mg. Fig 2 shows the SEL and SEU cross-section curves of the bulk devices. The bulk devices are sensitive to SEL at a LET of 29.3 MeVcm²/mg. No SEL was observed at the LET of 13.5 MeVcm²/mg. The SEL was only observed on the I/O and periphery power supplies. The maximum measured SEL current is 160 mA.

Because of the memory physical organization, no multiple errors within a data byte were observed. However, at high LET, Multiple Event Upsets (MEU) were observed. In most cases, a MEU only affects 2 neighboring memory cells. Fig 3 shows the physical locations of the upsets observed at the highest tested LET of 76 MeVcm²/mg. We can see that the errors are randomly distributed in the memory array. Only one triple error was observed, and the double errors represent about 16% of the total number of errors.

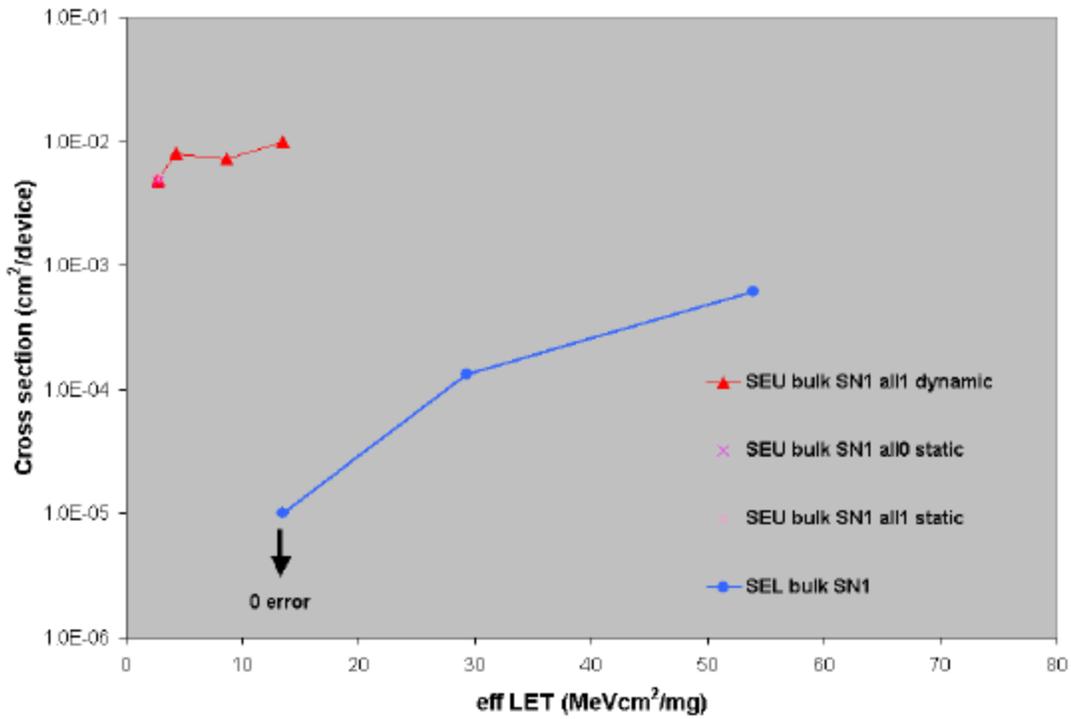


Fig 2: SEL and SEU cross-sections of the bulk devices.

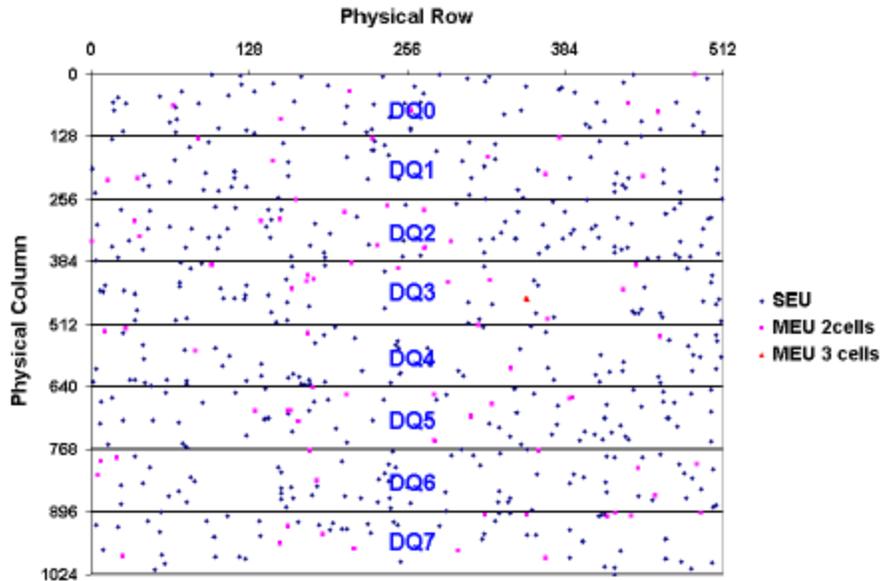


Fig 3: Physical mapping of the errors, SOI device irradiated at a LET of 76 MeVcm²/mg, run 17.

Table 4 shows the number of MEUs in function of LET for SOI devices. We can see that the number of MEU decreases quickly with the LET. At a LET below 29 MeVcm²/mg, the number of MEUs is negligible. On bulk devices, the number of MEUs is also negligible at low LET. We do not have data at high LET on bulk devices.

Table 4: Number of MEUs versus the number of SEUs
in function of LET, SOI devices

Run #	eff LET (MeVcm ² /mg)	SEU	MEU		Ratio MEU/SEU
			2 cells	3 cells	
31	2.8	619	3	0	0.5%
34	13.5	426	0	0	0.0%
46	29.3	304	10	0	3.3%
48	38.2	322	26	0	8.1%
49	45.6	283	26	0	9.2%
15	53.9	595	88	0	14.8%
17	76.2	495	81	1	16.4%

5 High energy beam testing at Michigan State University (MSU)

5.1 Introduction

A complementary heavy ion test was performed at MSU on September 2, 2004. The objective of this test was to study effect of high angles of incidence on SEU sensitivity. This test also gave more information on the bulk devices.

5.2 Irradiation Facility

The tests have been performed at the MSU particle accelerator on September 2, 2004. MSU facility provides very high-energy ion beams. The characteristics of beam used are given in Table 5. Irradiation has been performed in Air.

Table 5: Characteristics of ions used at MSU

Ion	Energy at target (MeV)	LET at target (MeVcm ² /mg)	Range at target (? m)
Xe-124	17360	14.1	~3300

5.3 Test set-up and bias conditions

The SRAM were tested with the same test set-up and under the same conditions than those used at TEXAS A&M. In addition to the two test modes investigated at TAMU, another test mode was used:

- dynamic write: During irradiation the DUT is continuously written and read. This mode leads to a lower cross section than the other modes, because the memory content is refreshed during irradiation.

5.4 Test results

Test results are shown in Table 6.

Table 6: Test results

Run #	Type	DUT #	Pattern	Test Mode	Tilt (°)	eff LET (MeVcm ² /mg)	eff Fluence (#/cm ²)	SEU #	Xsection SEU (cm ² /bit)	SEL #	Xsection SEL (cm ² /device)
1	SOI	1	all0	dynamic write	0	14.10	1.77E+04	21	2.26E-09	0	0.00E+00
2	SOI	1	all0	dynamic write	0	14.10	4.04E+04	28	1.32E-09	0	0.00E+00
3	SOI	1	all0	dynamic write	0	14.10	4.10E+04	22	1.02E-09	0	0.00E+00
4	SOI	1	all1	dynamic write	0	14.10	4.20E+04	24	1.09E-09	0	0.00E+00
5	SOI	1	all1	static	0	14.10	4.08E+04	202	9.44E-09	0	0.00E+00
6	SOI	1	all1	static	70	41.23	1.40E+04	129	1.76E-08	0	0.00E+00
7	SOI	1	all0	static	70	41.23	1.39E+04	156	2.14E-08	0	0.00E+00
8	SOI	1	all0	static	0	14.10	4.20E+04	239	1.09E-08	0	0.00E+00
9	SOI	1	all0	dynamic write	0	14.10	2.67E+04	20	1.43E-09	0	0.00E+00
10	SOI	1	all1	static	0	14.10	4.14E+04	180	8.29E-09	0	0.00E+00
11	SOI	2	all0	static	0	14.10	4.10E+04	192	8.93E-09	0	0.00E+00
12	SOI	2	all0	static	70	41.23	1.40E+04	142	1.93E-08	0	0.00E+00
13	SOI	2	all1	static	70	41.23	1.40E+04	137	1.87E-08	0	0.00E+00
14	Bulk	1	all0	static	0	14.10	4.04E+04	211	9.95E-09	0	0.00E+00
18	Bulk	1	all1	static	70	41.23	1.49E+04	266	3.40E-08	0	0.00E+00
19	Bulk	1	all0	static	70	41.23	1.45E+04	197	2.59E-08	0	0.00E+00
22	Bulk	2	all0	static	70	41.23	4.93E+05			1	2.03E-06
23	Bulk	2	all0	static	70	41.23	4.13E+05			1	2.42E-06

Fig 4 shows the SEU cross-sections. The measured cross sections are in agreement with those measured at TEXAS A&M. We can see that, as expected, the dynamic write mode results in lower cross-sections. It was possible to measure the SEU cross section of bulk devices at the maximum LET of 41.2 MeVcm²/mg. If we do not see any difference between bulk and SOI devices at the lowest LET obtained with a normal incidence beam, we can see that the cross-sections at the highest LET obtained with the same beam at a 70 degrees incidence, are higher for the bulk devices.

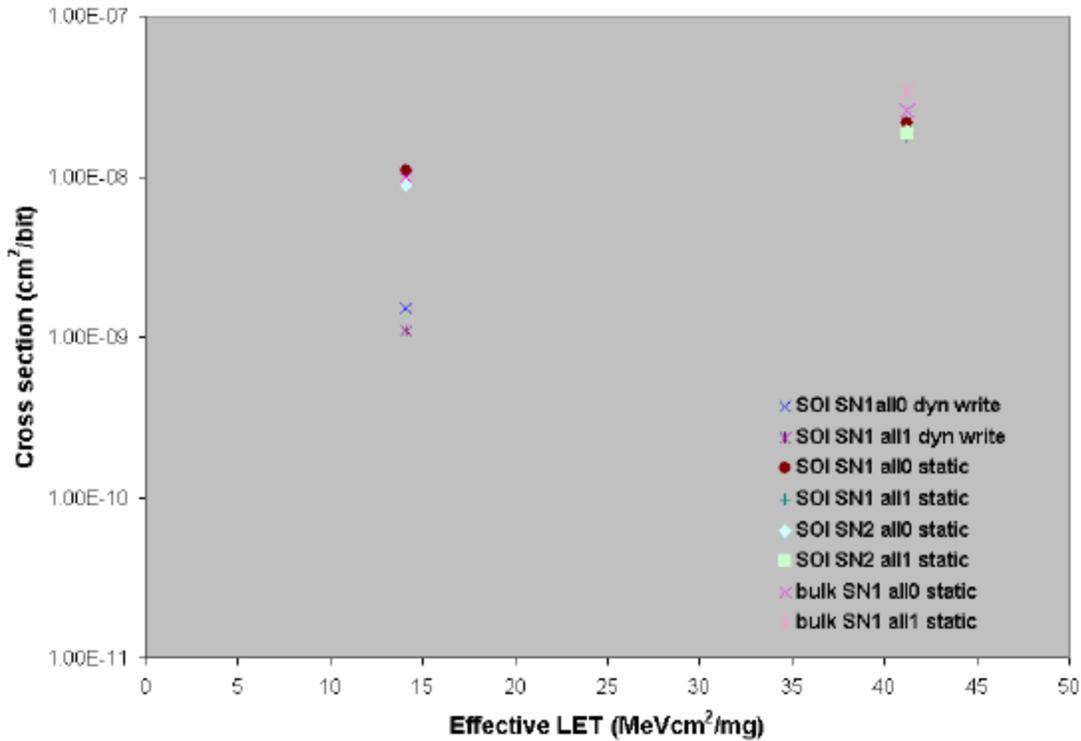


Fig 4: SEU cross section

Table 4 shows the number of MEU in function of LET. We can see that both for SOI and bulk devices for the LET of 14 MeVcm²/mg the number of MEU is negligible. At the LET of 41 MeVcm²/mg, the double errors represent about 4% of the total number of errors in SOI devices. For a LET of 38.2 MeVcm²/mg at TAMU the ratio was 8%. For bulk devices at the LET of 41 MeVcm²/mg, the double errors represent up to 40% of the total number of errors. This explains the higher cross section of bulk devices at this LET.

Table 7: Number of MEUs versus the number of SEUs in function of LET

Run #	Type	Pattern	Tilt	eff LET (MeVcm ² /mg)	SEU	MEU		Ratio MEU/SEU
						2 cells	3 cells	
5	SOI	all1	0	14.10	220	2		0.9%
8	SOI	all0	0	14.10	239	0		0.0%
6	SOI	all1	70	41.23	119	5		4.2%
7	SOI	all0	70	41.23	142	5		3.5%
14	Bulk	all0	0	14.10	211	0		0.0%
18	Bulk	all1	70	41.23	178	44		24.7%
19	Bulk	all0	70	41.23	105	46		43.8%

6 Laser Testing

6.1 Introduction

A laser test was performed at Naval Research Laboratory (NRL) on September 17, 2004. The objective of this test was to identify the SEL sensitive areas on bulk devices.

6.2 Irradiation Facility

The NRL laser is a pulsed laser with a 590nm wavelength resulting in a penetration depth of about 2 ? m. The laser spot size is about 1 ? m in diameter.

6.3 Test set-up and bias conditions

- The SRAM were tested with the same test set-up and under the same conditions than those used heavy ions broad beam tests.

6.4 Results

As observed during the heavy ion tests, no SEL was observed in the memory arrays. Fig 5 shows the SEL sensitive area in the periphery. We can see that a large part of the periphery circuitry is sensitive to SEL.

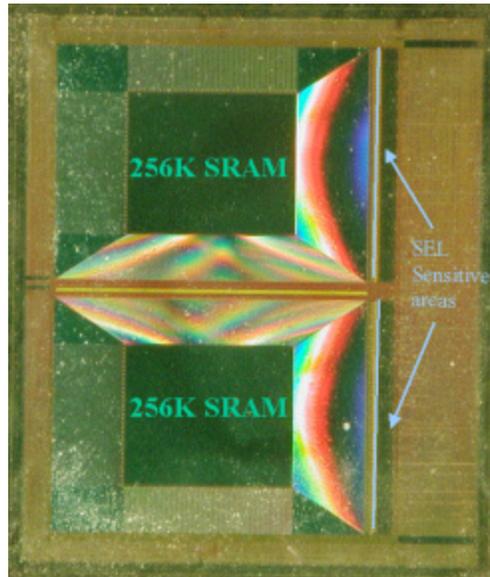


Fig 5: bulk devices, SEL sensitive area.

7 Conclusion

Test results show that:

- Bulk devices are sensitive to SEL from a LET between 14 and 29 MeVcm^2/mg . Laser tests have identified the SEL sensitive area in the device periphery. The maximum measured SEL current is 160 mA
- SOI devices not sensitive to SEL up to the maximum tested LET of 76.2 MeVcm^2/mg
- The bulk devices have a SEU LET threshold lower than 2.8 MeVcm^2/mg and a cross section of $3.5\text{E-}8 \text{ cm}^2/\text{bit}$ at the LET of 41 MeVcm^2/mg . A full SEU characterization of bulk devices was not possible because of the devices SEL sensitivity.
- The SOI devices have a SEU LET threshold lower than 2.8 MeVcm^2/mg and a maximum cross section of $3\text{E-}8 \text{ cm}^2/\text{bit}$.
- Small numbers of MEUs were observed on SOI devices. The numbers of MEUs increase with LET. They are negligible at low LET and represent about 16% of the events at high LET.
- The sensitivity of bulk devices is similar to the one of SOI devices at low LET. At higher LET the sensitivity of bulk devices is slightly higher. This can be explained by the large numbers of MEUs, up to 40% of the total numbers of events, observed on bulk devices at high LET.
- For both bulk and SOI devices, the test pattern does not have any effect on the SEU sensitivity.