Heavy Ion Testing of Freescale Nano-Crystal Nonvolatile Memory*

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Outline

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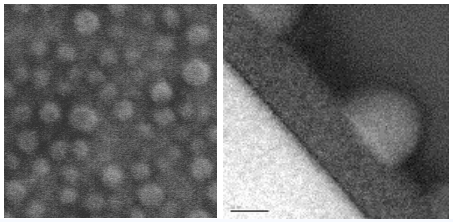
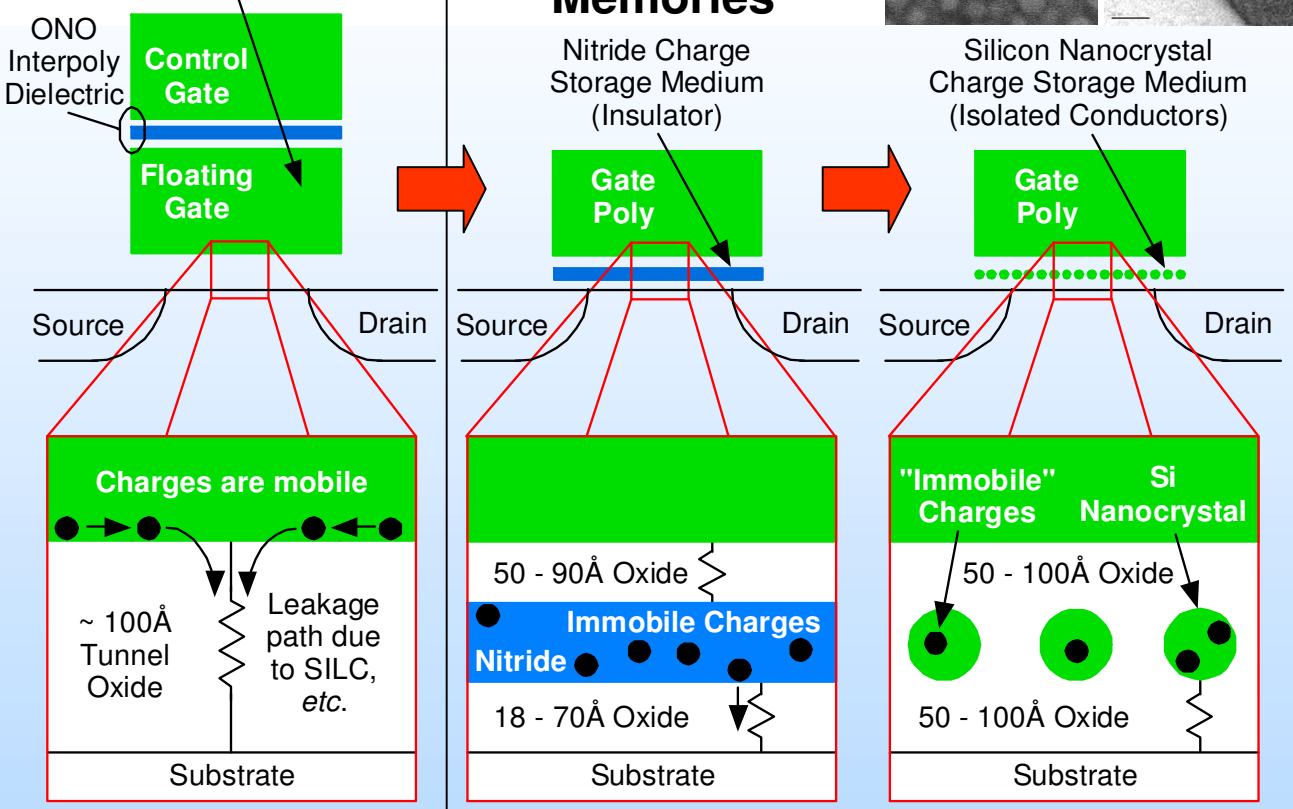
- Description of Devices
- Test Procedure
- Experimental Results
- Analysis and Discussion
- Conclusions

Introduction

- Floating Gate (FG) non-volatile memories (NVM) are widely used in space systems
  - Commercially available
- However,
  - FG has been shown to be sensitive to ionizing radiation
  - Concern that FG cannot be scaled below 100 nm for reliability issues
- Nanocrystal (NC) memory has the potential to
  - Scale <<100 nm with increased reliability at 90 nm and below, as well as,
  - Increase radiation resistance

Thin Film Storage Nonvolatile Memories



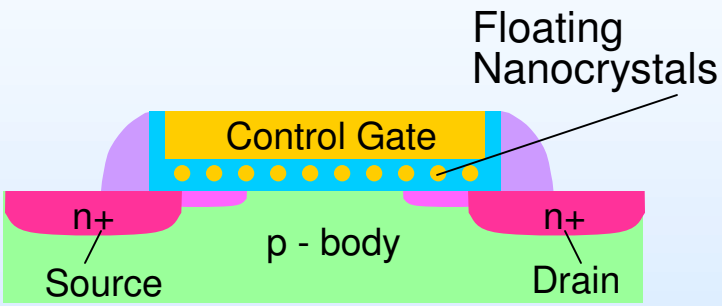


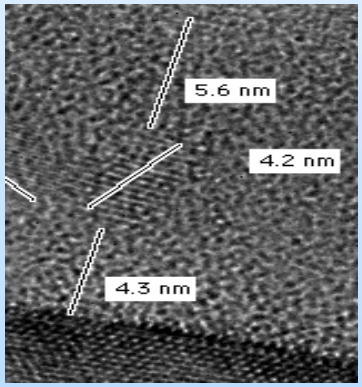
Floating Gate | **SONOS (oxide/nitride/oxide)** | **Nanocrystal**

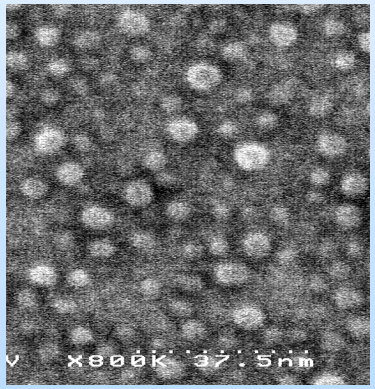
Nanocrystal Storage for Embedded NVM

- **Write/Erase Voltage Reduction**
  - **±6...±7V write/erase voltages instead of ±9V**
  - **50% periphery area reduction**
- **No SILC (stress induced leakage current)-related extrinsic reliability issue**
- **No gate or drain coupling effect**
- **Process Simplicity**
  - **Floating gate: adds 6-11 masking steps**
  - **Nanocrystal: adds 4 masking steps**

Description of Devices

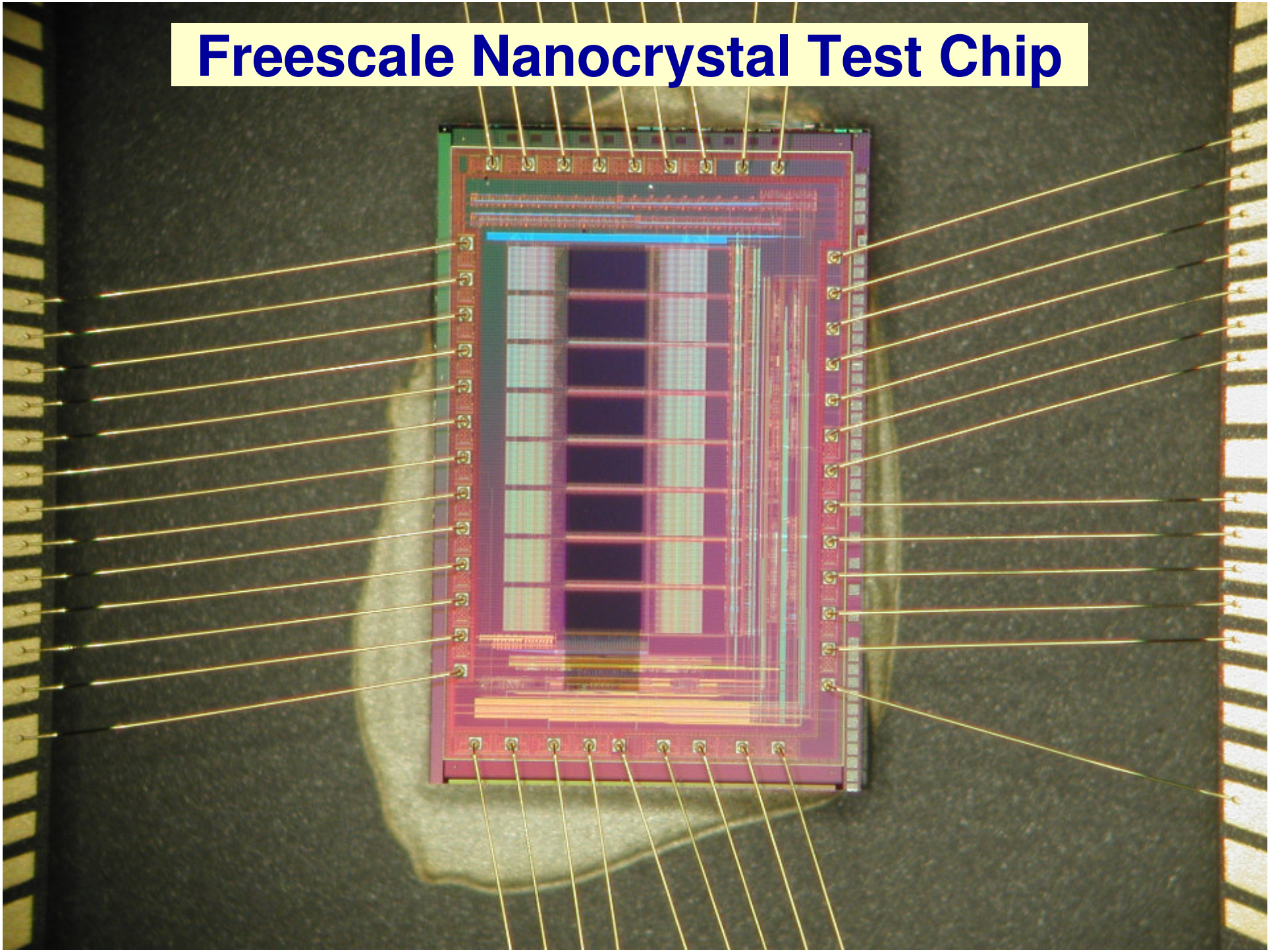






- **Write by CHE (channel hot electron) injection**
- **FN (Fowler-Nordheim) Erase**
- **Read by detecting V_T (threshold voltage) difference (zero V_T is about 2V greater than one V_T)**
- **Nominal 6V supply**

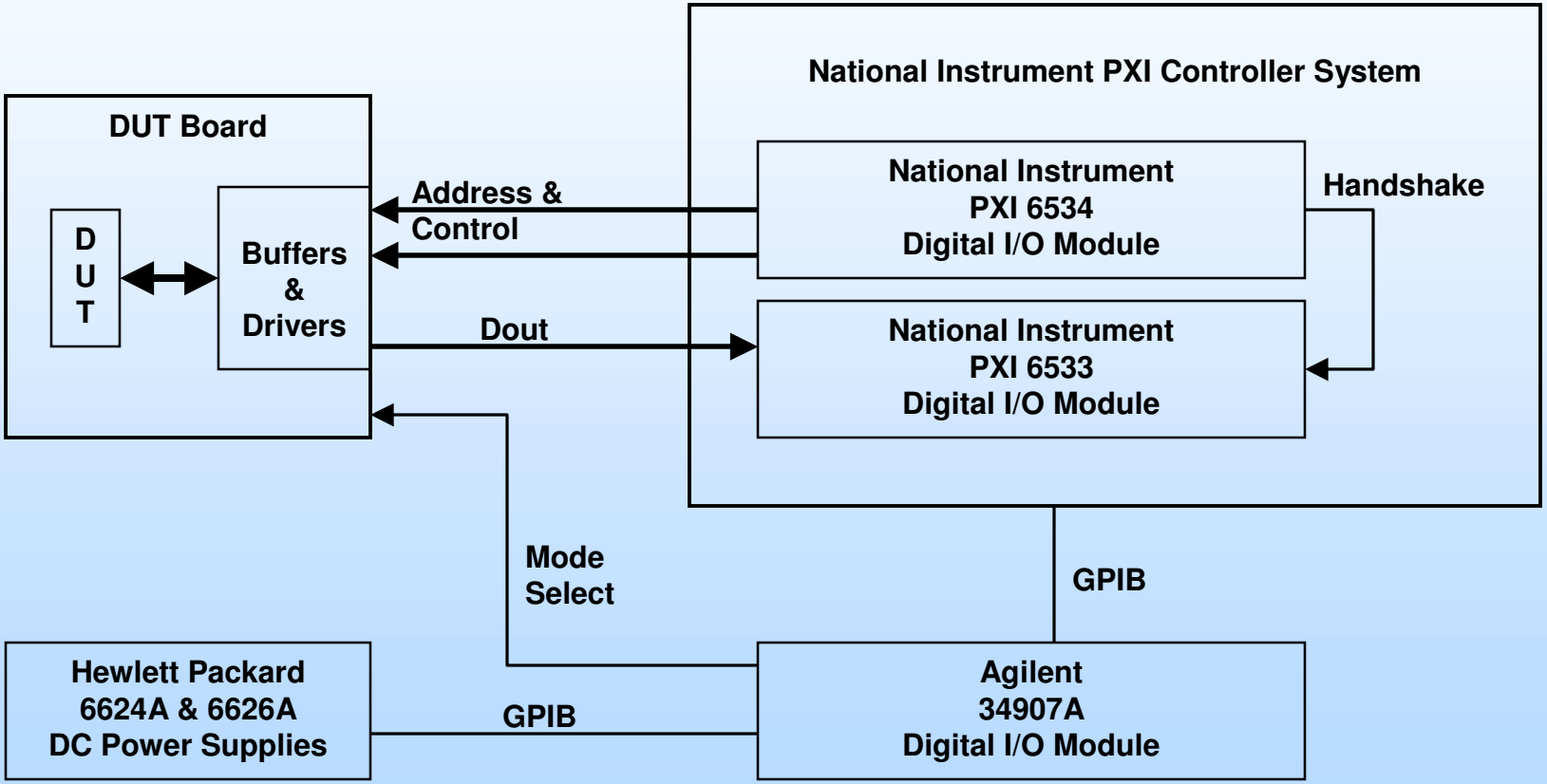
Freescale Nanocrystal Test Chip



Experimental Procedure

- Devices under test (DUTs)
  - 130 nm CMOS, part of 90 nm development process
    - Nanocrystal
      - 6V Vdd
      - 0.1V Vt margin
    - FG
      - (9V Vdd)
      - ~2V Vt margin
- Exposures
  - Heavy ion at Texas A&M University (TAMU) Cyclotron
    - 15 MeV/nucleon cocktail
  - Naval Research Laboratories' Pulsed laser
- Test modes
  - Static, dynamic read, dynamic write, dynamic erase tests
- All tests performed at room temperature and nominal Vdd, frequency ~25 kHz

Experimental Apparatus



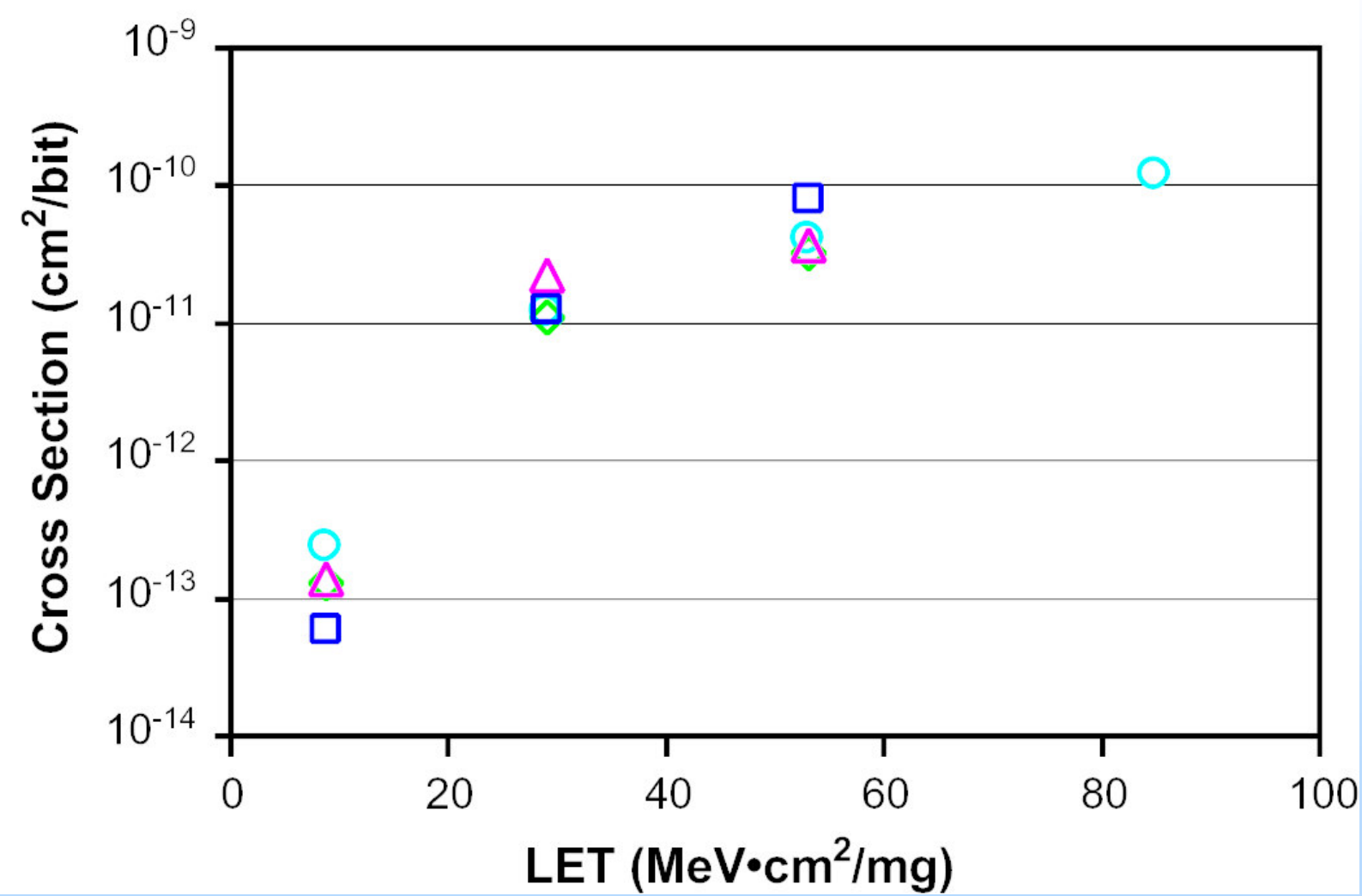
Heavy Ions Used at TAMU

Ion	E (MeV)	LET (MeV/mg/cm^2)	Range (μm)
Ar	497	8.7	175
Kr	916	29.3	117
Xe	1299	53.8	102
Au	2247	85.0	118

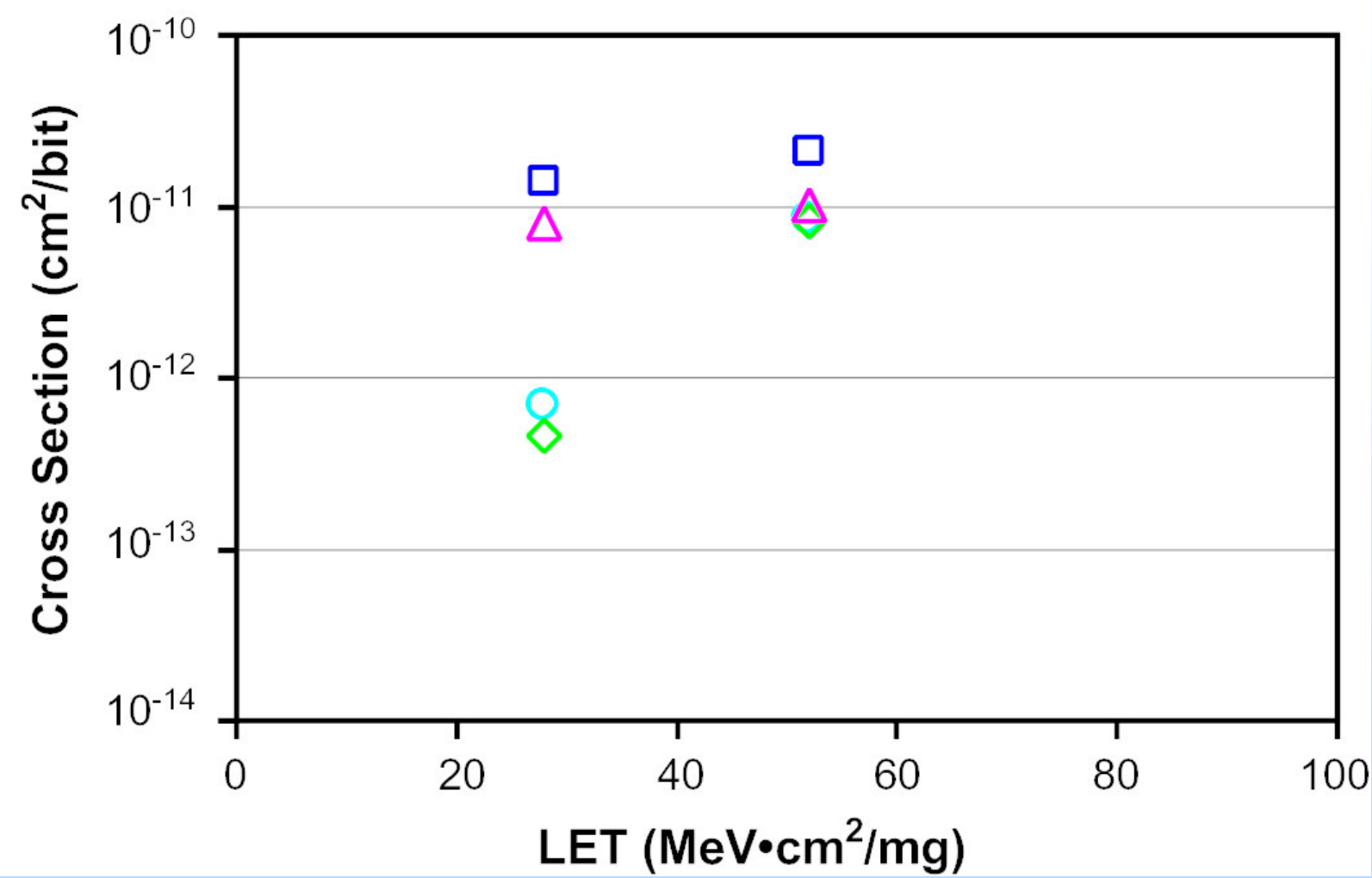
Heavy Ion Results - Nanocrystal

- Errors observed in all test modes
  - All errors appear to be static errors, even in dynamic tests
    - Cell values changed and remained at values until re-written
- Fewer errors observed in write and erase tests
  - Errors are being overwritten during exposures
- All errors are zeroes turned into ones (loss of stored electrons)
- Error rate depends on voltage margin
  - 0.1 V used for this test
    - Production chip would have >> margin
- High current state observed, suggestive of latchup, but parts remained fully functional
- No single event functional interrupts (SEFIs) noted
- Limited test on FG
  - Linear Energy Transfer (LET) of 29 Mev*cm^2/mg: no Single Event Effects (SEE) observed

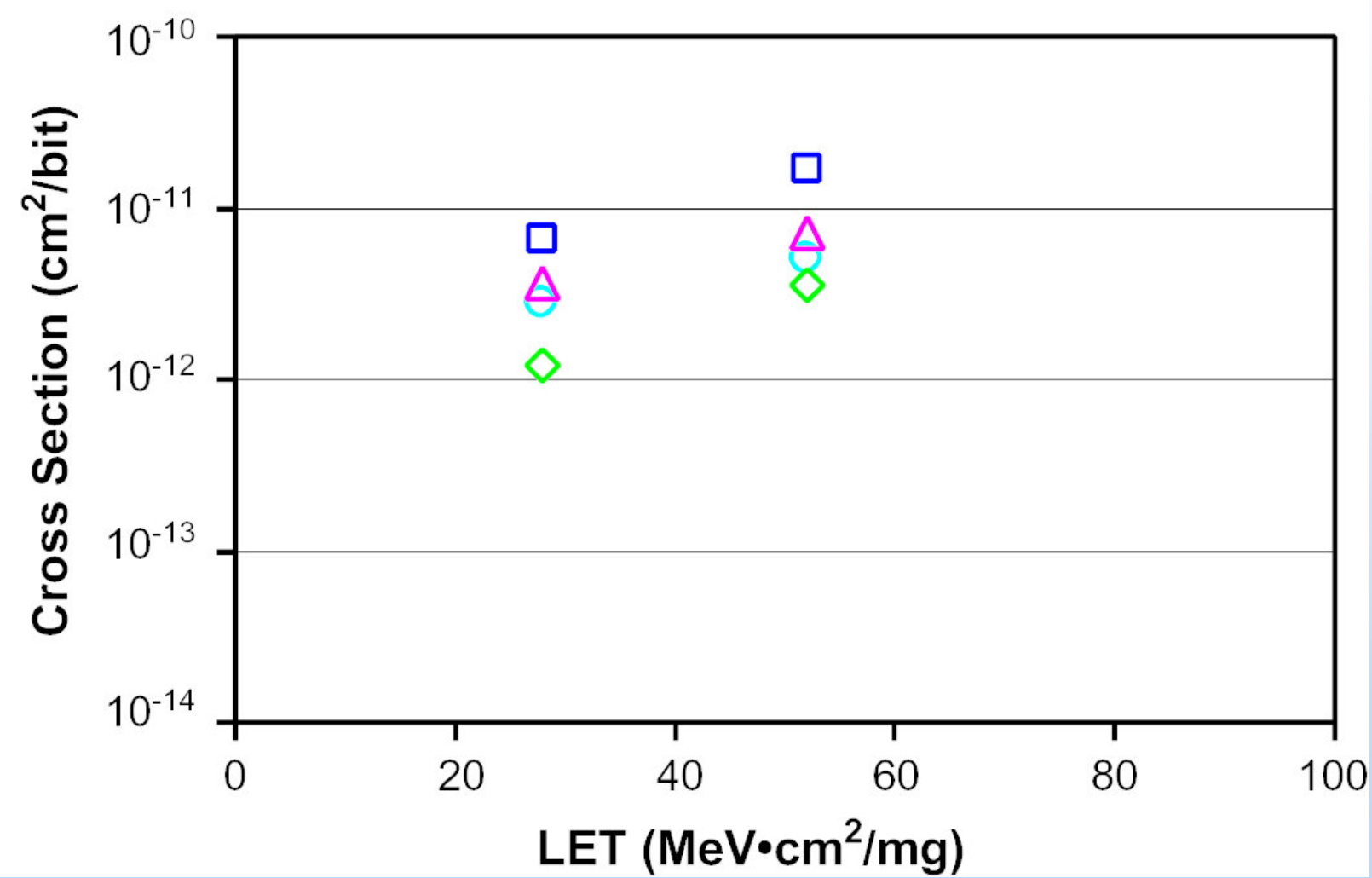
Read Errors – Nanocrystal Heavy Ion



Write/Read Errors – Nanocrystal Heavy Ion



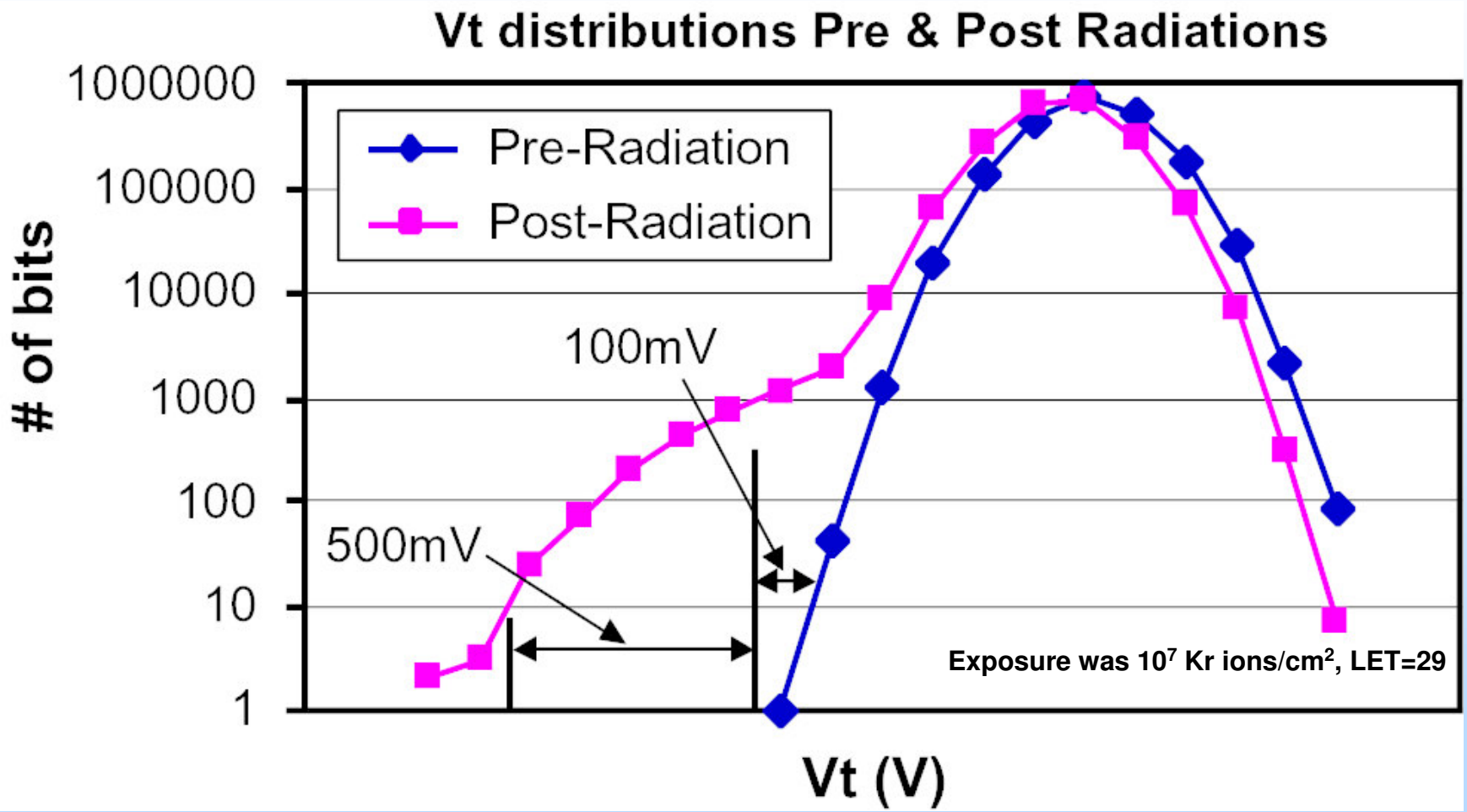
Write/Erase/Read Errors – Nanocrystal Heavy Ion



Laser Test Results – Nanocrystal and FG

- **No bit errors observed**
  - **Laser will not produce ionization in SiO_2**
- **No errors observed in control circuits on NC parts**
- **Apparent latchup in FG parts**
  - **Possibly due to higher voltages applied**
    - **Devices could not be erased after exposure, including ultraviolet (UV) erase**

Threshold Voltage Distribution



Discussion

- Charge loss, from observed V_T shifts, is 1-2 orders of magnitude greater than positive charge deposited by ion
  - Micro-dose (alone) not sufficient to explain observed charge loss
- Cellere et al. (IEEE TNS Dec 2002) reported similar results for FG cells—presented three possible models, but found problems with all three
  - Models should not apply to NC arrays, even if problems were resolved for FG—single conducting defect should not drain charge from whole array
- Underlying mechanisms not yet explained

Conclusions

- Nanocrystal memories are promising for space applications
- Bit error rate is generally better than previous reports for FG flash NVM
- Only static errors (loss of electrons) observed
- No SEFI
- No unambiguous evidence for latchup