Heavy-ion Single Event Effects Test of LSI Logic 0.18 μm G12 process Logic chip Test Vehicle

Test Report

NASA-GSFC, Radiation Effects and Analysis Group (REAG), Code 561

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1 Introduction

This report presents the heavy-ion SEE test results obtained on the Logic chip test vehicles of the LSI-Logic 0.18 µm G12 processes (CMOS bulk and CMOS SOI). These tests were performed in the frame of NASA Electronics Parts and Packaging (NEPP) program.

2 Tested devices

The device tested is a logic test chip (LXA0381). The logic test chip contains 64, 64-bit ALUs. It has been designed with full scan methodology. There are 4 scan chains with a length of 3072 flip-flops each. This design was synthesized to operate at a maximum speed of 20 MHz. The I/O buffers used in this design consist of 3 voltage types 1.8V, 2.5V, and 3.3V. A picture of the logic test chip is shown in Figure 1. The logic test chip is packaged in a 313 pin plastic EPBGA package.

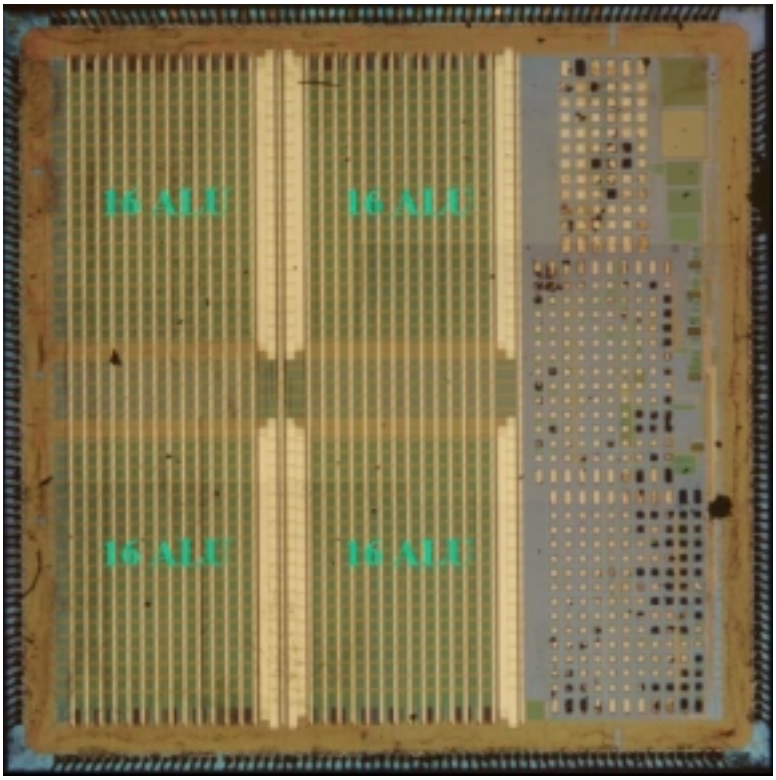


Fig 1: Picture of the Logic test vehicle die

Table 1 gives the information on the test sample provided by LSI-Logic. Four parts from each process (SN1 to 4) have been delidded for Single Event Effect Testing.

Table 1: Test samples information

Process		Package	Package Marking	Sample Size
G12	Bulk	IR52 (plastic EPBGA 313)	LSI Logic LXA0381 GAF49909.7 8603T036SEE4 EEG11008.1 ENGR SAMPLE G0412 Δ Korea	SN1to4 (delidded),
	SOI	IR52 (plastic EPBGA 313)	LSI Logic LXA0381 GAF33921.2 A3R5A027WSD6 EEG11009.1 SOI ENG SAMPLE G0412 Δ Korea	SN1to4 (delidded)

3 Test Description

3.1 Irradiation Facility

The tests have been performed at the Texas A&M particle accelerator on August 14 and 15, 2004. Irradiation has been performed in Air. The distance of Air between the ion beam output and the Device Under Test (DUT) was 6 cm. The characteristics of beams used are given in Table 2. The LET and ranges values given in Table 2 are the LET and range on the DUT, the target, after 6cm of Air and the 25.4 μm Aramica window.

Table 2: Characteristics of ions used at TEXAS A&M

Ion	Energy (MeV/u)	Energy at target (MeV)	LET at target ($MeVcm^2/mg$)	Range at target (μm)
Xe	15	1291	53.9	102
Kr	15	912	29.3	116
Ar	15	496	8.7	174
Ne	15	266	2.8	261

3.2 Test set-up and bias conditions

NASA-GSFC has developed a specific test set-up. Two different test modes have been checked:

- **ALU mode**: In this mode 48 of the device 64 ALUs are operated in sequence one after each other. A static input is applied, and each ALU tested performs in sequence all 16 binary and 16 logical arithmetic operations. The test principle is the golden chip test method. The outputs of the Device Under Test (DUT) during irradiation are compared to those of a reference device operated under the same conditions. In this mode, only one ALU is tested at a time. The number of tested bits is 128 bits (input flip-flops) 25%of the time and 64 bits (output flip-flops) 25% of the time.
- **Scan chain mode**: In this mode we use the device scan chain capability. All flip-flops of each of the four 16 ALUs blocks are chained to form a 3072 bits shift register. We have connected three 3072 bits shift registers to form a 9216 bits shift register. The input signal alternates 1 and 0 at each clock cycle. The number of tested bits in this mode is 9216.

During irradiation the DUT was biased at the nominal power supply of 3.3V (Vdd33), 2.5V (Vdd4), and 1.8V (Vdd, Vdd2). In the ALU mode the device was operated at a 1.25 Mhz clock frequency. In the scan test mode, the device has been operated at three test frequencies, 1, 2.5, and 5 MHz.

The Power supply current of the DUT was monitored and charted during irradiation to detect the occurrence of SEL or other anomalous condition. In case of SEL, the set-up shuts down the DUT power

supply. The SEL detection threshold was set to 200 mA for the Vdd and Vdd2 power supplies, 20 mA for the Vdd33 power supply, and 20 mA for the Vdd4 power supply.

4 Test Results

The test results are shown in Table 3.

Table 3: Test Results (1/2)

Run #	Type	SN #	function	frequency (MHz)	tilt	eff LET (MeVccm2/mg)	eff. Fluence (#/cm2)	SEU #	X SEU (cm2/bit)	SEL #	Comment
79	SOI	3	ALU dynamic	1.25	0	29.3	2.52E+06	5	4.13E-08	0	
80	SOI	3	ALU dynamic	1.25	0	29.3	2.12E+06	7	6.88E-08	0	
81	SOI	3	ALU dynamic	1.25	0	29.3	2.31E+06	6	5.41E-08	0	
82	SOI	3	shift register	5	0	29.3	7.07E+05	1047	1.61E-07	0	
83	SOI	3	shift register	5	0	29.3	8.36E+05	1138	1.48E-07	0	
84	SOI	3	shift register	2.5	0	29.3	7.94E+05	818	1.12E-07	0	
85	SOI	3	ALU dynamic		0	8.7	9.93E+06	2	4.20E-09	0	
86	SOI	3	ALU dynamic		0	8.7	9.86E+06	3	6.34E-09	0	
87	SOI	3	ALU dynamic		0	8.7	1.01E+07	3	6.19E-09	0	
88	SOI	3	shift register	2.5	0	8.7	1.00E+07	1176	1.28E-08	0	
89	SOI	3	shift register	5	0	8.7	1.00E+07	1704	1.85E-08	0	
92	SOI	3	shift register	1	0	8.7	9.95E+06	1234	1.35E-08	0	
94	SOI	30	ALU dynamic		0	8.7	1.02E+07	7	1.43E-08	0	
96	SOI	30	ALU dynamic		0	8.7	1.00E+07	6	1.25E-08	0	
97	SOI	30	shift register	1	0	8.7	1.00E+07	1554	1.69E-08	0	
99	SOI	30	shift register	5	0	8.7	9.99E+06	2113	2.30E-08	0	
102	bulk	32	ALU dynamic		0	8.7	9.91E+06	burst		0	
103	bulk	32	ALU dynamic		0	8.7	5.08E+06	burst		0	needs a power cycle to recover
104	bulk	32	shift register	2.5	0	8.7	2.47E+06	burst		0	
105	bulk	32	shift register	1	0	8.7	5.66E+05	burst		0	
106	bulk	31	shift register	1	0	8.7	2.37E+06	burst		0	
107	bulk	31	ALU dynamic		0	8.7	2.02E+06	burst		0	
108	bulk	31	ALU dynamic		0	8.7	1.59E+05	burst		0	needs a power cycle to recover
109	SOI	3	ALU dynamic		0	8.7	1.00E+07	3	6.25E-09	0	
110	SOI	3	shift register	2.5	0	8.7	1.00E+07	1251	1.36E-08	0	
111	SOI	3	shift register	2.5	0	2.8	1.02E+07	6	6.38E-11	0	
112	SOI	3	shift register	5	0	2.8	9.88E+06	10	1.10E-10	0	
114	SOI	3	shift register	1	0	2.8	9.91E+06	8	8.76E-11	0	
115	SOI	3	ALU dynamic		0	2.8	9.71E+06	0	0.00E+00	0	
116	SOI	30	ALU dynamic		0	2.8	9.80E+06	0	0.00E+00	0	
117	SOI	30	shift register	1	0	2.8	9.89E+06	20	2.19E-10	0	
118	SOI	30	shift register	2.5	0	2.8	1.00E+07	8	8.68E-11	0	
119	SOI	30	shift register	1	0	2.8	9.92E+06	10	1.09E-10	0	
121	SOI	30	shift register	5	0	2.8	1.02E+07	33	3.51E-10	0	
122	SOI	30	shift register	5	0	2.8	1.02E+07	17	1.81E-10	0	
123	bulk	31	ALU dynamic		0	2.8	9.99E+06	0	0.00E+00	0	
124	bulk	31	shift register	1	0	2.8	1.01E+07	112	1.20E-09	0	
125	bulk	31	shift register	1	0	2.8	8.49E+06	burst		0	
126	bulk	31	shift register	1	0	2.8	9.97E+06	96	1.04E-09	0	
127	bulk	31	shift register	2.5	0	2.8	1.01E+07	118	1.27E-09	0	
128	bulk	31	shift register	5	0	2.8	9.96E+06	150	1.63E-09	0	
131	SOI	34	ALU dynamic		0	29.3	5.11E+06	9	3.67E-08	0	

Table 3: test results (2/2)

Run #	Type	SN #	function	frequency (MHz)	tilt	eff LET (MeVccm2/mg)	eff. Fluence (#/cm2)	SEU #	X SEU (cm2/bit)	SEL #	Comment
133	SOI	34	ALU dynamic		0	29.3	5.00E+06	10	4.17E-08	0	
134	SOI	3	shift register	1	0	29.3	1.14E+06	1094	1.04E-07	0	
135	SOI	3	shift register	2.5	0	29.3	1.03E+06	1036	1.09E-07	0	
136	SOI	3	shift register	5	0	29.3	6.91E+05	1086	1.71E-07	0	
137	SOI	3	ALU dynamic		0	53.9	1.00E+07	44	9.17E-08	0	
139	SOI	3	shift register	2.5	0	53.9	6.74E+05	1076	1.73E-07	0	
140	SOI	3	shift register	5	0	53.9	4.84E+05	1188	2.66E-07	0	
141	SOI	3	shift register	1	0	53.9	6.57E+05	1032	1.70E-07	0	
142	SOI	3	ALU dynamic		35	65.8	3.01E+06	11	7.61E-08	0	
143	SOI	3	shift register	1	35	65.8	5.08E+05	1026	2.19E-07	0	
144	SOI	3	shift register	2.5	35	65.8	4.79E+05	1032	2.34E-07	0	
145	SOI	3	shift register	5	35	65.8	4.04E+05	1092	2.93E-07	0	
146	SOI	35	ALU dynamic		0	53.9	2.26E+06	11	1.01E-07	0	
147	SOI	35	shift register	1	0	53.9	6.26E+05	1086	1.88E-07	0	
148	SOI	35	shift register	2.5	0	53.9	5.64E+05	1044	2.01E-07	0	
149	SOI	35	shift register	5	0	53.9	3.88E+05	1076	3.01E-07	0	
150	SOI	35	shift register	5	35	65.8	3.64E+05	1067	3.18E-07	0	
151	SOI	35	shift register	2.5	35	65.8	4.60E+05	1056	2.49E-07	0	
152	SOI	35	shift register	1	35	65.8	4.89E+05	1032	2.29E-07	0	
154	SOI	35	ALU dynamic		35	65.8	3.92E+06	burst		0	
155	SOI	35	ALU dynamic		35	65.8	8.18E+05	10	2.55E-07	0	
156	SOI	35	ALU dynamic		35	65.8	8.67E+05	burst		0	

Fig 1 shows the SEU cross-sections. The LET threshold of SOI devices is lower than 2.8 MeVcm^2/mg maximum measured SEU cross-section is about 3.8E-07 cm^2/bit.

At the LET of 2.8 MeVcm^2/mg, the measured cross section for the bulk devices is about 1.12E-09 cm^2/bit. It is significantly higher than the cross-section measured on SOI devices at the same LET. It has not been possible to measure the SEE sensitivity of bulk devices for LET higher than 2.8 MeVcm^2/mg. For higher LET, large bursts of errors are observed because the device stops functioning. Analysis of the 1.8V power supply current files showed high current anomalies (HCA): the current jumps of 10 to 60 mA from its nominal value and stays at this high value. As soon as the HCA occurs, the device stops functioning. A power cycle is necessary to recover functionality. There are two possible causes of HCAs in CMOS devices:

- Micro latch-up: A latch-up path is triggered by one heavy ion, but the latch-up current is limited by the device internal circuitry. As the current is limited, the micro latch-up is not destructive, but it affects the device functionality.
- Single Event Snapback (SES): SES occurs in N channel MOSFET structures. It is caused by parasitic action of the bipolar transistor formed by the source, well (or substrate), and drain within an individual MOSFET, which affects the avalanche breakdown characteristics and causes a high current condition.

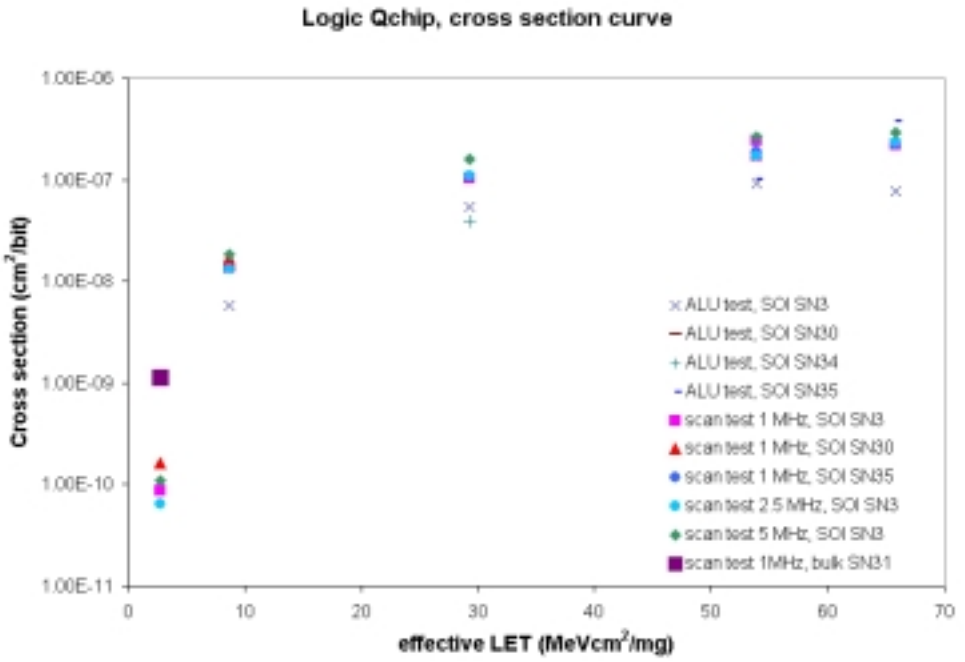


Fig 1: SEU cross-section

Fig 2 shows the measured cross-sections in the scan chain mode in function of the clock speed. The measured cross-section increases only slightly, about 30%, when the test frequency increases from 1 to 5 MHz. We may expect higher cross-sections at higher frequencies.

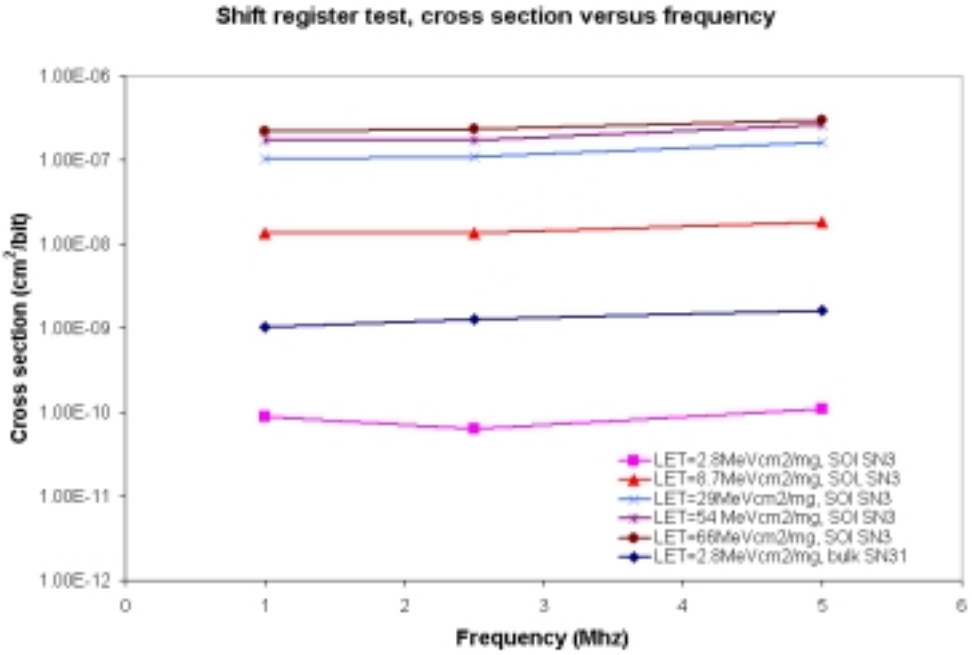


Fig 2: SEU cross-sections versus clock speed in the scan chain mode.

5 Laser Testing

5.1 Introduction

A laser test was performed at Naval Research Laboratory (NRL) on September 17, 2004. The objective of this test was to identify the HCA sensitive areas on bulk devices.

5.2 Irradiation Facility

The NRL laser is a pulsed laser with a 590nm wavelength resulting in a penetration depth of about 2 µm. The laser spot size is about 1 µm in diameter.

5.3 Test set-up and bias conditions

- The Logic chip test vehicles were tested with the same test set-up and under the same conditions than those used heavy ions broad beam tests.

5.4 Results

Laser experiments showed a very high HCA sensitivity of bulk devices. Sensitive areas are spread all over the die. Fig 3 shows the die picture and 3 successive locations that have been hit with the laser. Fig 4 shows the evolution of 1.8V supply current. At the location 1 the current jumped from its nominal value of 16 mA to 66 mA. At the last location, the current has reached 106 mA.

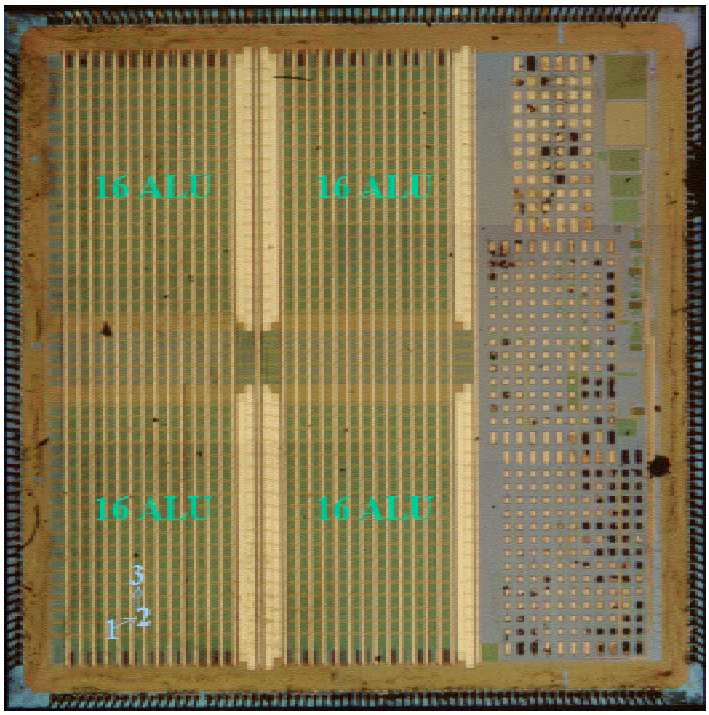


Fig 3: Location of 3 sensitive areas

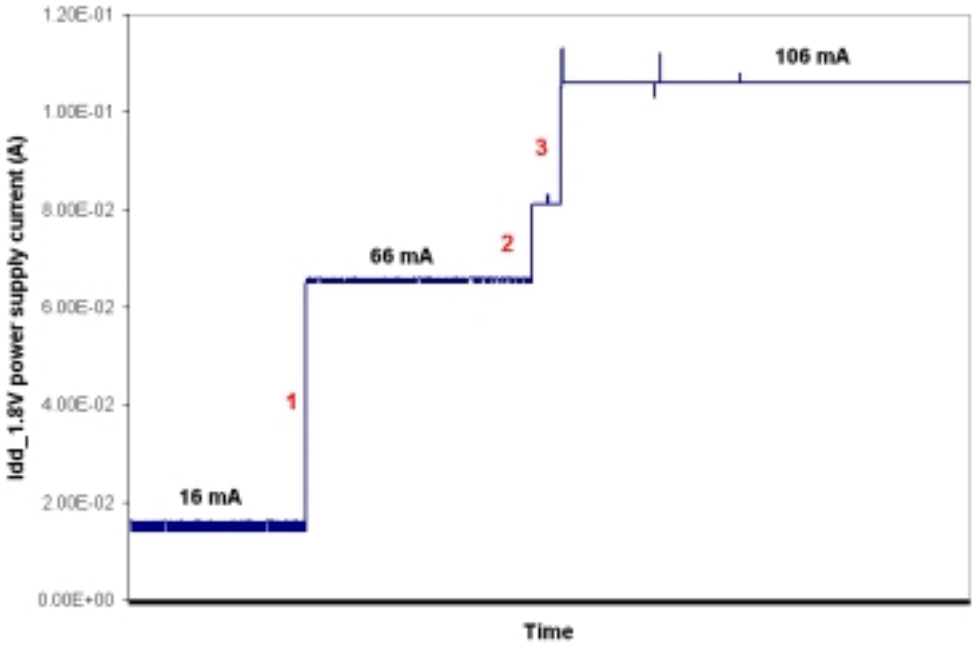


Fig 4: 1.8V supply current evolution when the 3 sensitive areas identified in Fig 3 are hit successively with the laser.

6 Conclusion

Test results show that the bulk process is highly sensitive to heavy ions induced HCA events. When a HCA occurs, the device stops functioning, and a power cycle is necessary to recover functionality. These events were observed for a LET as low as 8.7 MeVcm^2/mg. The measured SEU cross section at the LET of 2.8 MeVcm2/mg is 1.12E-09 cm2/bit.

The SOI process is not sensitive to HCA or SEL up to the maximum tested LET of 68 MeVcm^2/mg. The SEU LET threshold is lower than 2.8 MeVcm^2/mg and the maximum measured cross section of 3.8E-7 cm^2/bit. In the frequency range investigated, from 1 to 5 Mhz, the effect of clock frequency on SEU sensitivity is not very large. It is expected that the increase of SEU sensitivity will be significant at higher test frequencies.