Demonstration of 500°C AC Amplifier Based on SiC MESFET and Ceramic Packaging

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Abstract

Silicon carbide (SiC) metal-semiconductor-field-effect transistors (MESFETs) and ceramic packaging systems have been previously reported for operation in 500°C air ambient for extended periods of time. In this paper, we report successful demonstration of a 500°C low frequency AC voltage amplifier based on SiC devices and ceramic packaging in air ambient for over 430 hrs. Four common-source amplifier circuits were integrated on an Al_2O_3 printed circuit board (PCB). Each amplifier circuit was composed of a SiC MESFET, two SiC on-chip resistors, and an aluminum oxide (96%Al_2O_3) chip-level package. The amplifier was thermally soaked in a bench-top oven, and periodically tested with electrical bias. The high temperature amplifier demonstrated a voltage gain of 15 at room temperature, and a gain of 7 at 100Hz at 500°C, and was stable during 430 hours of heat soak testing. The demonstration of durable and stable operation of a functional 500°C amplifier with packaging is a further step towards useful 500°C extreme environment electronics and packaging technology.

Key wards: High temperature, amplifier, SiC, MESFET, passives, packaging, integration.

I. Introduction

NASA space and aeronautical missions require 500°C operable electronics for probing Venus' surface, as well as for *in situ* monitoring and control of next generation aeronautical engines [1]. 500°C electronics can also find many applications in military, and energy and automobile industries. As very basic elements of high temperature electronics, SiC transistors (MESFETs) [2] and prototype ceramic chip-level (level 1) packages [3] for 500°C operation have been reported in recent years. However, demonstration of high temperature functional circuits based on SiC transistors and ceramic packages still requires high temperature passives and multi-component integration at PCB level (level 2 packaging). Therefore, demonstration of a 500°C functional circuit would be a significant step towards implementation of high temperature electronics. In this paper, we report a 500°C low frequency AC voltage amplifier circuit based on a SiC MESFET, high temperature passives, and a ceramic packaging system. The AC voltage amplifier is one of most commonly required functional circuit units for signal conditioning.

II. Experimental Details

II.I SiC Device Fabrication and Characterization

High temperature n-channel MESFETs and resistors were fabricated on a commercially purchased off-axis 6H p-type SiC epitaxial wafer [4]. The schematic cross-section of the device is shown in Fig. 1. The transistor device used in this paper was from the same wafer we reported earlier [2]. The n-channel of 1 X 10^{17} cm^{-3} doping is 0.2-0.4 μm thick, the underlying p-type layer of doping less than 2 X $10^{15}$$cm^{-3}$ is 7 μm thick. The n-channel epitaxial layer was also used for implementation of resistors on the chip. The transistors originally had been intended to be junction field effect transistors (JFET), but the top p-layer epitaxial layer (not described above) was inadvertently removed during device processing. The SiC MESFETs and resistors were patterned using an inductively coupled plasma (ICP) reactive ion etcher (RIE) in order to isolate the various epitaxial layers. A box-like profile ion implantation with nitrogen dosages of ~10^{14} cm^{-2} was used for the source/drain contacts. The first dielectric layer was a wet thermal oxidation of about 600 Å. The subsequent dielectric layers were 4000 Å of Si_3N_4 (Fig. 1). The contact metal for both p- and n- layers and all interconnect layers was a triple stack of Ti/$TaSi_2$/Pt which has

been shown to have excellent high temperature stability [5]. All vias and metal patterning were accomplished with a parallel plate RIE except for the oxide via which was wet etched in BOE (buffered oxide etch). A photograph of the completed prepackaged transistors and resistors can be seen in Fig. 2. On-chip capacitors were fabricated using Si_3N_4 dielectric between the top two metal layers, but did not function acceptably.

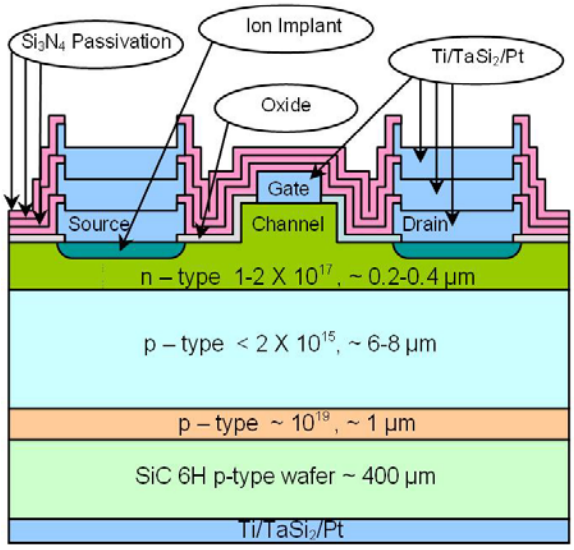

Fig. 1: Schematic drawing of the structure of the MESFET.

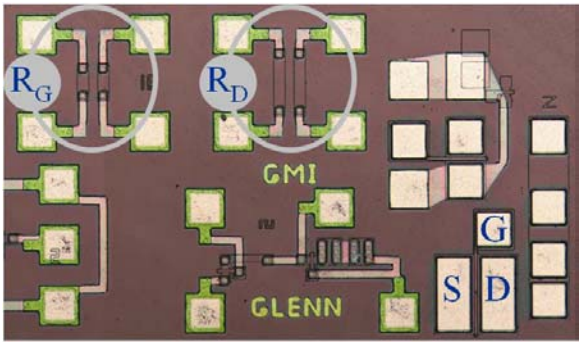

Fig. 2: An optical micrograph of the MESFET, R_G, and R_D prior to packaging. The source, gate, and drain on the MESFET is labeled as S, G, and D.

Electrical characterization of the MESFETs and SiC resistors began with room temperature characterization using a digitizing curve tracer [6]. The first 500 ºC testing commenced following an unbiased overnight heat soak at 500 ºC. All transistor and resistor characterization tests were carried out in air atmosphere, in darkness, with the curve tracer continuously sweeping families of drain current (I_D) versus drain voltage (V_D) curves at a drain sweep frequency of 60 Hz. The V_D was swept from 0 to ~ 50 V and then back for each gate voltage (V_G) step of -2 V. The substrate bias voltage (V_{sub}) was -20 V throughout all reported tests. The resistor I-V curves display the same bias quadrant as the resistors were biased in the circuits. Device characteristics were tested periodically at 500 ºC (during the periods of time the devices were not electrically tested the devices were not electrically biased).

II.II Ceramic Capacitors

96%Al_2O_3 substrates were used as the dielectric material for high temperature ceramic capacitors [7]. Both sides of a 2.5 in. x 2.5 in. x 15 mil 96%Al_2O_3 substrate were metallized with pure Au thick-film. The metallized Al_2O_3 substrate was diced into 36 pieces, each with dimensions of 0.4 in. x 0.4 in.. Au wires were bonded on both sides of these diced substrates. Then, nine of these substrates were stacked layer by layer, and electrically connected together in parallel forming a single capacitor with Au wires for electrical connection. The ceramic capacitor was characterized at both room temperature and 500°C using an LC impedance meter. The optical picture of these ceramic capacitors will be shown later.

II.III Packaging

The ceramic chip-level packages used for this investigation have been reported previously [3]. This chip-level package was designed for low power small scale circuits. The substrate material was aluminum oxide (96% Al_2O_3), and Au thick-film (processed at 850°C) was used for substrate metallization [8]. The package had 8 I/Os. A picture of an unsealed package is shown in Fig. 3. The detailed electrical specifications of this chip-level package at various temperatures have been reported previously [3]. Table 1 shows the parasitic capacitance and dielectric loss, between 100 Hz and 1 MHz, between room temperature and 550°C.

The ceramic PCB used for this testing was also based on a 96% Al_2O_3 substrate and Au thick-film metallization so that the PCB material was compatible to the chip-level packages. The PCB was specifically designed for the 8-pin low power, high temperature chip-level packages. Each PCB could hold up to four chip-level packages (packaged devices) and eight 2-terminal passive components. The PCB was metallized on both sides, and had 48 vias. The PCB provided 14 I/Os for each circuit unit, and had a total of 56 I/Os for flexible testing. Fig. 4 shows the PCB with components. The SiC die

Table 1a: The distributed capacitance and AC conductance between I/O1 (ground) and the nearest neighbor I/O (I/O2) on the prototype Al_2O_3 package. The upper number in each table entry is capacitance in units of pF, unless otherwise specified. The lower number is conductance in units of μS [2].

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00	5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	1.5	1	1	1	1.5	2	2.0	2.0	2.5	4	4
	0.000	0.000	0.000	0.000	0.00	0.00	0.000	0.000	0.0015	0.002	0.0025
1K	1.5	1.3	1.3	1.4	1.35	1.5	1.6	1.75	1.85	2.15	2.35
	0.001	0.000	0.00	0.000	0.000	0.001	0.001	0.002	0.0025	0.004	0.0055
10K	1.36	1.33	1.3	1.36	1.35	1.46	1.43	1.56	1.54	1.63	1.74
	0.003	0.000	0.000	0.001	0.001	0.002	0.004	0.006	0.010	0.015	0.020
100K	1.33	1.38	1.28	1.36	1.36	1.44	1.36	1.427	1.42	1.53	1.47
	0.015	0.006	0.006	0.007	0.009	0.0135	0.018	0.0255	0.036	0.052	0.071
1M	1.29	1.30	1.29	1.40	1.35	1.45	1.33	1.39	1.42	1.45	1.47
	-	-	-	-	-	-	-	-	-	0.043	0.12

Table 1b: The distributed capacitance and AC conductance between two neighbor I/Os (I/O2 and I/O3) on the prototype Al_2O_3 package. The upper number is capacitance in units of pF, unless otherwise specified. The lower number is conductance in units of μS [2].

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	< 5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	0.5	0.5	0.5	1	1	1	1.5	1.5	1.5	1.5	2
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.0005	0.001	0.001
1K	0.5	0.5	0.5	0.5	0.5	0.5	0.6	0.7	0.7	0.8	0.95
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.001	0.002	0.0025
10K	0.49	0.50	0.50	0.490	0.49	0.52	0.53	0.58	0.59	0.65	0.69
	0.001	0.000	0.000	0.000	0.000	0.001	0.002	0.003	0.004	0.006	0.008
100K	0.492	0.486	0.497	0.493	0.487	0.517	0.539	0.535	0.563	0.585	0.57
	0.005	0.006	0.0015	0.002	0.003	0.005	0.007	0.011	0.015	0.022	0.030
1M	0.501	0.497	0.485	0.506	0.499	0.529	0.533	0.55	0.556	0.544	0.55
	-	-	-	-	-	-	-	-	-	-	-

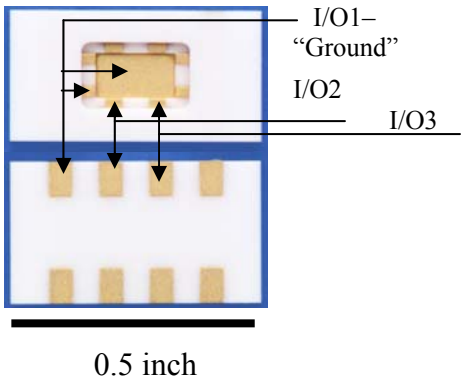

Figure 3: Top and bottom views of 96% Al_2O_3 8-pin chip-level package and I/O numbers used in Table 1.

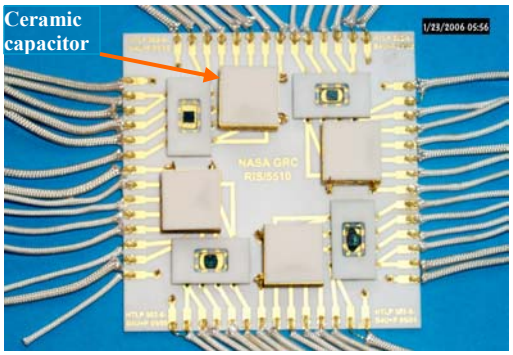

Figure 4: The assembly with four testing circuit units. The prototype ceramic capacitors are illustrated

was attached to the 96% Al_2O_3 chip level package using a low (electrical) resistance material developed in house (more detailed knowledge will be released later). This die-attach material was compatible with the Pt thin-film capped triple-layer-metallization ohmic contact designed for high temperature SiC devices [5]. The die-attach process was performed at 500°C. The SiC devices were connected to the package I/Os with 98% Au alloy wires. A thermal sonic ball/wedge bonder was used for wire bonding. The impurities of the Au alloy wire segregate to the wire surface and form an oxide layer at high temperature. The surface oxide layer was intended to reduce electromigration at the surface of the Au wires under DC current conditions. In order to perform degradation and failure analysis after testing, the packaged SiC devices were not sealed with lids. Packaged SiC devices were connected to the ceramic PCB with an in-house developed conductive material which was cured at 500°C (more detailed knowledge will be released later). 10 mil diameter Au wires were used to electrically connect the PCB with the test instruments located outside of the oven [6]. During 500°C testing, the test assembly (PCB with attached devices) was completely thermally soaked in a bench-top oven with a temperature programming function. In order to reduce low frequency noise, the test assembly was surrounded with aluminum foil to provide electromagnetic shielding from the filaments inside the oven.

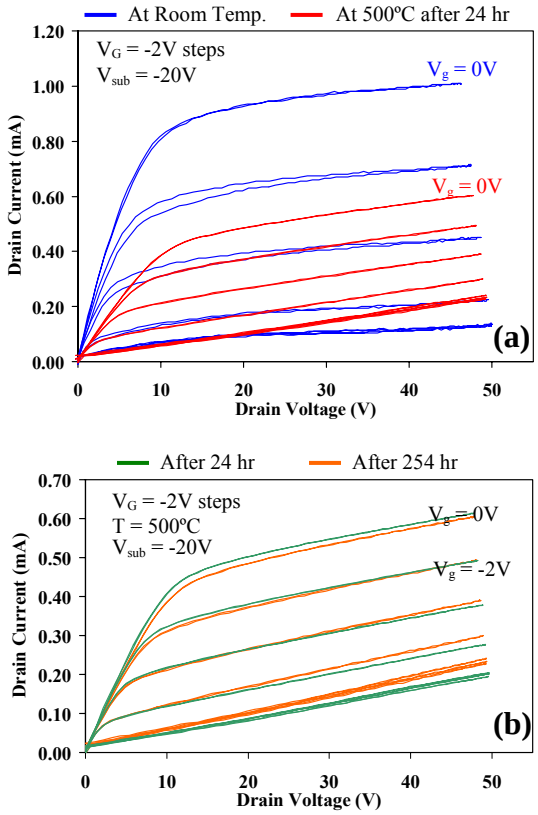

Figure 5: (a) Room temperature compared with 500 ºC and (b) comparison of the MESFET drain characteristics measured before and after 254 hours of temperature stress.

III. Component and Amplifiers

III.I Characterization of Transistors and Resistors

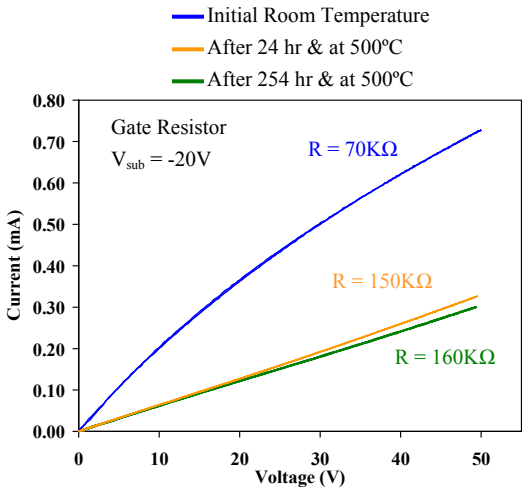

Figure 6: Positive quadrant of IV curve of gate resistor (R_G).

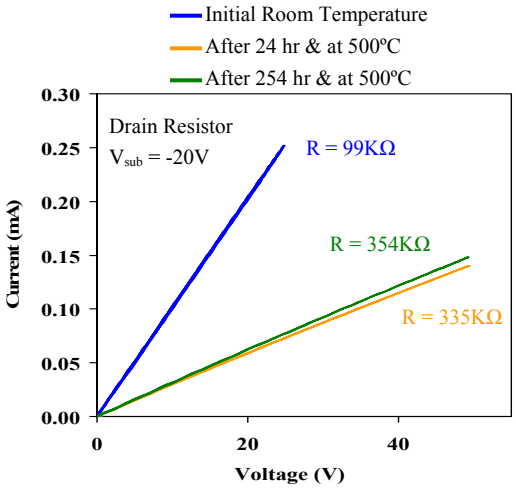

Figure 7: Positive quadrant of IV curve of drain resistor (R_D).

Fig. 5a compares room temperature and 500ºC I-V curves of a MESFET measured near the beginning of the test. Initial room temperature tests had a hysteresis (i.e. looping) which disappeared when the device was heated to 500 ºC but reappeared after cooling. Fig. 5b compares the transistor

performance from 24 hours after commencement of the test to the performance of the device after 254 hours at 500 ºC. Although gate leakage increased due to the gradual degradation of the MESFET's Schottky barrier, the overall characteristics remain stable after 254 hours. The initial gate leakage was due to a leakage path around the metal gate and was an artifact of the loss of the top p-layer.

The I-V curves for the drain and gate bias resistors at initial room temperature, after 24 hours at 500ºC, and after 254 hour at 500 ºC are displayed in fig. 6 and 7. The resistance of the gate bias resistor decreased slightly after 254 hours whereas the resistance of the drain resistor increased slightly over the same 254 hours at 500ºC.

III.II Ceramic Capacitors

The frequency dependent capacitance and dielectric loss of the ceramic capacitor measured at both room temperature and 500°C are listed in Table 2.

Table 2: Capacitance and conductance of ceramic capacitor at room temperature and 500°C.

f (Hz)	120	1k	10k	100k
T_R	835 pF	835pF	835pF	821pF
	0.03μS	0.18μS	0.83μS	4.1μS
500°C	1250pF	1015pF	920pF	879.2pF
	0.28μS	0.90μS	3.11μS	12.8μS

III.III Common Source Amplifiers

The simple common-source amplifier included a SiC MESFET, a SiC drain resistor, a gate bias resistor, and coupling capacitor(s) as shown in Fig. 8. Three separate DC power supplies were used for V_{DD}, gate bias, and substrate bias, respectively. As discussed in the SiC device section, the metal–semiconductor Schottky interface was reverse biased, so at room temperature, the input impedance is approximately determined by R_G (R_G was 70 kΩ). However, at 500°C the gate impedance of the MESFET decreased so the input impedance of the circuit decreased even though the R_G at 500°C was approximately doubled. For a light load Z_L (Z_L»R_D//r_L, r_L is the equivalent resistance of MESFET drain-source leakage), the AC voltage gain of the amplifier was determined by the trans-conductance (y_{21}) of the MESFET and the drain resistor:

$$A_V = - y_{21} R_D$$

The I-V curves of the MESFET and SiC epilayer based resistors were used to select the candidates of drain and gate bias resistors, as well as to determine the range of power suppliers to be utilized for V_{DD}, gate bias, and substrate bias for the amplifier circuit.

The DC voltage transfer characteristics, V_D vs. V_G, under different substrate bias conditions, were measured to determine the initial gate (DC) and substrate biases for good voltage gain and linear dynamic range (for room temperature). The gate and substrate biases were then optimized using an AC input signal for best gain and linear range. The -3dB frequency of the amplifier with the external capacitor (0.47 μF) was measured. The -3dB frequency of the amplifier with the external capacitor was close to $1/R_{in}C_{in}$, where C_{in} was the capacitance of the high temperature ceramic capacitor and R_{in} was the input impedance of the amplifier (without coupling capacitor). So the external capacitor, C_{ext} was used for most AC tests of the amplifier (the capacitance of the ceramic capacitor was not sufficient). The amplifier circuit was then characterized with a small signal of AC voltage.

At 500°C, the same procedure was followed to determine the circuit parameters (resistors and DC bias conditions). A sine wave signal with 1 V (peak to peak) amplitude was used to measure the frequency response. The voltage gain of the amplifier circuit, in a frequency range from 50 Hz up to 10 kHz, was measured by a digital oscilloscope. Waveforms of input and output signals were also recorded with the oscilloscope when it was necessary. After the characterization at room temperature, the testing assembly was soaked in a bench-top oven, and the temperature was ramped from room temperature to 500°C in a rate of 40°C/min..

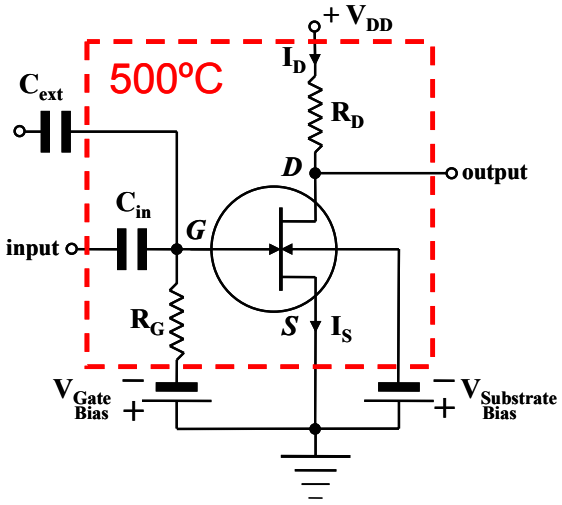

Figure 8: The simple common-source amplifier circuit. The red dash line indicates the components tested at 500°C. In addition to the ceramic high temperature capacitor, an external conventional capacitor (0.47μF) was used for coupling AC signal.

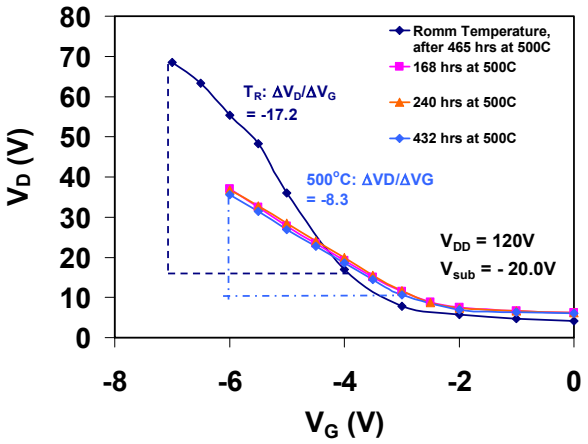

Figure 9: DC transfer characteristics under same V_{DD}, V_G, and V_{Sub} at room temperature, 500°C for 168 hours, 500°C for 240 hours, and 500°C for 432 hours, respectively.

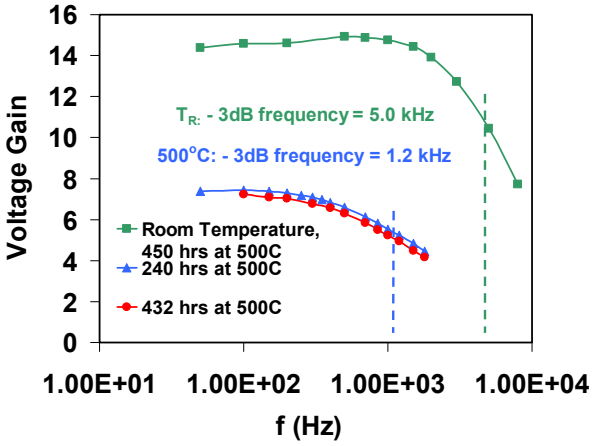

Figure 10: Frequency response of the amplifier with external capacitor at room temperature and 500°C.

For the amplifier circuit with the MESFET (I-V curves at room temperature and 500°C with various testing time are shown in Fig. 5) and resistors (I-V curves at room temperature and 500°C are shown in Fig. 6 and 7) discussed earlier, R_D = 100 kΩ at room temperature (T_R), and 335 kΩ at 500°C, and R_G = 70 kΩ at T_R, and 150 KΩ at 500°C. The DC bias sources were as follows: V_{DD} = 120 V, V_{Sub}= -20 V, and $V_{Gate\ bias}$ = -9 V for both T_R and 500°C.

Fig. 9 shows DC voltage transfer characteristics of the amplifier at T_R (after 465 hours at 500°C), 500°C for 168 hours, 500°C for 240 hours, and 500°C for 432 hours. The ideal V_G for optimized gain and linear dynamic range was -4.5V for both room temperature and 500°C. The room temperature curve shows a slope of – 17.2, and the 500°C data shows a slope of -8. Fig. 10 shows the frequency response of the amplifier circuit under these bias conditions, at room temperature, 500°C for 240 hours, and 500°C for 432 hours. The amplifier was basically a typical low pass amplifier at both room temperature and 500°C. At room temperature, (after 450 hrs at 500°C) the voltage gain of this amplifier (using an external capacitor for coupling AC signal) was between 13.9 and 14.9 (C_{ext}, 47 μF) between 50 Hz and 2 kHz. The -3dB point was 5 kHz. The dynamic linear output range was over 20 V. Fig. 11a shows an image of both input and output signals at 1 kHz. At 500°C (under same bias conditions), after 450 hrs at 500°C (the circuit was not constantly biased), the voltage gain was 7.1 up to 300Hz when tested with the external capacitor. The -3dB frequency was 1200 Hz. The performance of this amplifier was stable in the test time of 340 hours at 500°C. A waveform showing input and output signals at 100Hz is shown in Fig. 11b.

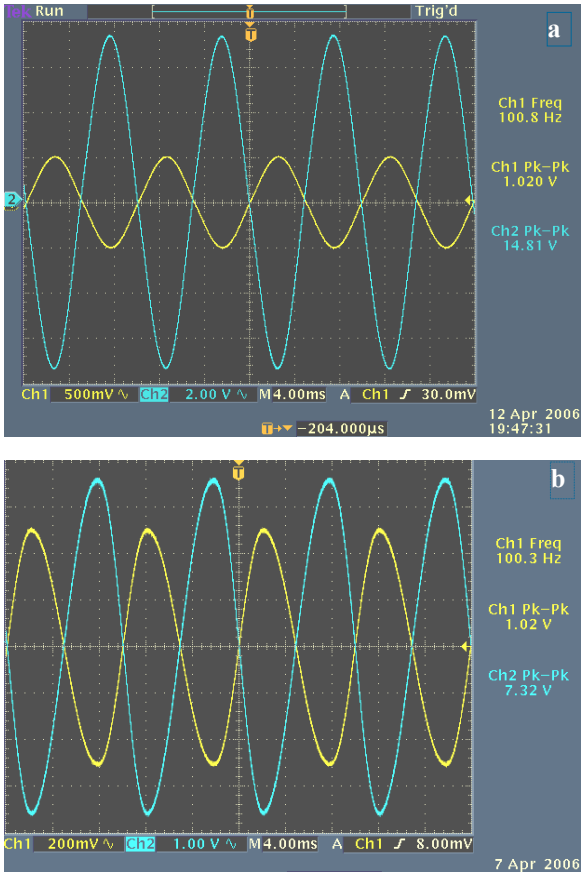

Figure 11: Waveform of input and output signals of amplifier circuit I, (a) at room temperature and 1 kHz, and (b) 500°C at 100 Hz.

As it was discussed earlier, the capacitance of the ceramic capacitor was not sufficient to be used in the frequency range that the amplifier was tested.

In a test with a different amplifier circuit (not discussed), it was found that the signal coupling using the ceramic capacitor was effective at frequencies above 4 kHz. A voltage gain of 2.2 for that amplifier circuit with the ceramic capacitor, at 4.6 kHz, was recorded.

Conclusions

High temperature, low frequency common-source voltage amplifier based on a SiC MESFET, SiC resistors, and high temperature ceramic packaging was successfully demonstrated at 500°C. Both voltage gain and frequency response were reasonably stable during the entire testing period of 430 hours at 500°C. Prototype ceramic capacitors based on 96% Al_2O_3 dielectric and Au thick-film metallization have been demonstrated for 500°C operation. In addition to the SiC MESFET and ceramic chip-level packages reported earlier, the demonstration of a functional 500°C amplifier indicates the most recent progresses in PCB-level packaging and passives for 500°C and is a significant step towards 500°C extreme environment applications.

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