NASA Electronic Parts and Packaging (NEPP) Program

Task: Hybrid

Subtask: Tantalum Capacitors

Effect of Temperature Cycling and Exposure to Extreme Temperatures on Reliability of Solid Tantalum Capacitors

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Abstract

Tantalum capacitors are widely used in hybrid microcircuits and in DC-DC converters in particular. During operation of power hybrids, all internal elements are typically heating up to relatively high temperatures, and power on/off cycles of the hybrids result in temperature cycling of the internal components. This means that all components used in high-reliability power hybrids should be capable of demonstrating the necessary robustness under multiple temperature cycling conditions.

Military-grade and commercial solid tantalum capacitors are typically rated to the same temperature range, from -55 °C to +125 °C, and during qualification testing per MIL-PRF-55365 they are subjected to a few thermal shocks only within these relatively narrow temperature limits. This means that no testing guarantees that these parts can withstand multiple cycling between -65 °C and +150 °C, as is required for hybrid microcircuits per MIL-PRF-38535, and military-grade tantalum capacitors cannot be used in space-qualified hybrids without additional testing.

Space exploration programs often require devices to be exposed to extreme environments, including cryogenic temperatures. Alternatively, the reflow soldering process can be considered as an ultimate high-temperature stress. However, the effects of exposure to extreme temperatures on reliability of tantalum capacitors have not been analyzed yet.

In this work, different types of solid tantalum capacitors were subjected to multiple temperature cycles (up to 1,000 cycles) and variations of capacitance, effective series resistance (ESR), leakage currents, and the probability of scintillations and surge current failures caused by the cycling were examined. Deformations of chip tantalum capacitors during reflow soldering simulation were investigated to evaluate the possibility of the pop-corning effect. Several part types were subjected to multiple (up to 100) fast cycles between room temperature and 240 °C with periodical measurements of characteristics to evaluate the effect of exposures to solder reflow temperatures. To assess thermo-mechanical robustness of the parts caused by extremely low temperatures, several groups of capacitors were subjected to multiple (up to 500) temperature cycles between room temperature and 77 K.

This report contains four parts. In the first three parts the effects of temperature cycling, multiple exposures to extremely high temperatures, reflow soldering temperatures, and cryogenic temperatures are discussed. The fourth part analyzes effects of mechanical stresses on performance and reliability of chip tantalum capacitors.

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Part I. Effect of Temperature Cycling in the Military Range of Temperatures on Reliability of Solid Tantalum Capacitors

I.1. Introduction

Commercial solid chip tantalum capacitors are typically rated to a temperature range from -55 °C to +125 °C, for both operational and storage conditions. For most electronic components, the storage temperature range is wider than the operational one, and the reason for the relatively narrow range of storage temperatures for tantalum capacitors is not clear. Discussions with manufacturers suggest that this situation probably is due to the lack of requirements regarding the storage conditions from the industry. Parts manufactured for the automotive industry, for example THJ capacitors available from AVX, have a continuous operating temperature of 150 °C and are tested by temperature cycling between -55 °C and +150 °C (however, five cycles only).

Military-grade tantalum capacitors manufactured according to MIL-PRF-55365 are rated to the same temperature range as commercial parts. During manufacturing, unmounted parts are subjected to five thermal shocks (TS) between -55 °C and +125 °C as a part of conformance inspection and to 10 TS as a part of qualification inspection (mounted). This means that no testing guarantees that these parts can withstand multiple cycling even within the operating temperature range.

Contrary to tantalum capacitors, military-grade ceramic chip capacitors manufactured per MIL-PRF-123 and microcircuits manufactured per MIL-PRF-38535 have much more stringent requirements for temperature cycling (TC). Ceramic capacitors should demonstrate the capability to withstand 100 TS between -55 °C and +125 °C, and the microcircuits during qualification testing are stressed with 100 TC between -65 °C and +150 °C. Note also that considering the required transfer times (t_t) during cycling, TS conditions for ceramic and tantalum capacitors (t_t ~5 min.) are closer to TC conditions for microcircuits (t_t ~15 min.), while thermal shock conditions for microcircuits are much more severe and require much faster temperature changes (t_t ~10 s).

The existing requirements for tantalum capacitors intended for space applications (NASA GSFC EEE-INST-002) are similar to the military standard, and no additional TC or TS testing is required during reliability qualification of these parts. However, MIL-PRF-38534 for hybrid microcircuits requires TC between -65 °C and +150 °C: 10 cycles during screening and 100 cycles during qualification testing. This means that military-grade tantalum capacitors cannot be used in space-qualified hybrids, and DC-DC converters in particular, without additional testing. Note that the same is true for ceramic capacitors, which are tested between -55 °C and +125 °C only. However, contrary to ceramic capacitors, where mechanical stresses are changing substantially after soldering onto a board, in tantalum capacitors, due to the presence of molding compound and metal frame, which might provide some stress relief, the stresses developed during TC are probably similar for loose and soldered parts. This makes TC testing of loose tantalum capacitors more effective and important compared to the ceramic parts.

A recent history of failures of DC-DC converters used in different space projects [1] indicates a relatively large proportion of cases (eight out of 31 reported) where capacitors were the culprits. Similar information was obtained from manufacturers of DC-DC converters, which indicated that failures of tantalum capacitors are the major reason for failures in DC-DC converters during

testing. G. Ewell and J. Siplon reported on ESR degradation of tantalum capacitors in hermetically sealed hybrids [2], where a significant (~100 times) increase in ESR was possibly related to long-term storage of the parts in dry nitrogen at 125 °C. In our experiments, where 10 DC-DC converters were subjected to multiple TC between -65 °C and +150 °C, one part ceased functioning due to a failed/burnt tantalum capacitor. These data suggest the necessity of a more thorough understanding of the robustness of tantalum chip capacitors and their mechanical and electrical integrity after stresses by multiple TC in a wide range of temperatures. Available literature data on the effect of temperature cycling on tantalum capacitors was scarce. In one of the early works, Franklyn, AVX, noted that the sensitivity to temperature cycling is quite different in various styles of chip tantalum capacitors [3]. Even the effect of soldering, which can be considered as an ultimate temperature cycling stress, is mentioned only in a few papers. The reported data indicate that the thermal stress caused by soldering of tantalum capacitors might increase leakage currents [4] and cause surge current failures [5].

In this work, results of multiple TC testing (up to 1,000 cycles) of different types of solid tantalum capacitors are analyzed and reported. Most testing was focused on variations of the specified characteristics of the devices, such as capacitance (C), effective series resistance (ESR), and DC leakage current (DCL). For some part types, the effect of TC on the probability of scintillations and surge current failures was examined. Recommendations for TC testing of the parts are given.

I.2. Experiment

Temperature cycling in the range from -65 °C to +150 °C was carried out on six groups of commercial chip and leaded tantalum capacitors and in the range from -65 °C to +125 °C on three groups of military-grade devices. Table 1 displays part types and test conditions used in our experiments. The dwell time at the temperature extremes was 15 min., and the transfer time was 10 min.

Table 1. Description of parts and test conditions.

Part	Type	DC	Qty.	TC Range, °C	C Limit, %	ESR Limit, Ohm	DCL Limit, µA	Case
2.2 µF/35 V	T491C225K035AS	DC 0506	10	-65 to +150	± 10	8	0.8	6032
15 µF/50 V Gr. I	T495X156M050AS	DC 0437	10	-65 to +150	± 20	0.3	7.5	7343
15 µF/50 V Gr. II	T495X156M050AS	DC 0405	10	-65 to +150	± 20	0.3	7.5	7343
22 µF/35 V	T491D226M035AS	DC 0408	60	-65 to +150	± 20	0.7	7.7	7343
10 µF/50 V	TAP106K050SCS	DC 0409	10	-65 to +150	± 10	1.6	4	J
10 µF/25 V	TAP106K025SCS	DC 0503	10	-65 to +150	± 10	2.5	2	E
2.2 µF/10 V	CWR09FC225KBA	DC 9732	15	-65 to +125	± 10	8	1	B
10 µF/25 V	CWR09KC106KCA	DC 9733	15	-65 to +125	± 10	1.4	3	G
22 µF/20 V	CWR09JC226KC	DC 0018	15	-65 to +125	± 10	0.9	4	H

Commercial parts were stressed to 500 cycles and military-grade parts to 1,000 cycles with interim measurements of C, ESR, and DCL. The leakage currents were measured at rated voltages while monitoring I(t) characteristics of the parts for 5 minutes and taking the last reading, so DCL = I(5).

Leakage current is the most sensitive indicator of the quality of dielectric in a capacitor compared to the other specified parameters such as C, DF, and ESR. However, DCL has also the largest margin between the real values and the specified limits. As an example, Table 1a shows statistical characteristics of distributions for 200 samples of commercial low-ESR TPSB106K020R1000 parts and 100 samples of TPS337K010R0040 parts. Although the leakage currents do not follow normal distribution, it is possible to estimate the margin (M) between the limit and values for the majority of the parts, as a ratio of the specified limit and the 3-sigma-extended median, M = limit/(median+3σ).

Table 1a. Comparison of characteristics of two types of capacitors with the specified limits.

Part	Param.	Average	St. Dev.	Median	Max.	Limit	Margin, %
TPSB106K020R1000	**C, µF**	9.63	0.12	9.63	9.86	11	110
	DF, %	1.86	0.09	1.86	2.34	6	283
	ESR, mOhm	444.7	42.4	443.6	589.6	1000	175
	DCL, nA	50.8	60.7	27.8	395.6	2000	953
TPS337K010R0040	**C, µF**	324.2	7.42	342.2	338.7	363	105
	DF, %	2.7	0.25	2.67	3.94	8	232
	ESR, mOhm	32.7	3	33.5	38.5	40	96
	DCL, µA	0.61	0.32	0.52	2.15	33	2200

In both cases the margin for DCL far exceeded the margin for other parameters, and the difference between the specified and median leakage currents was about two orders of magnitude. This situation is typical for most tantalum capacitors. For this reason, in our experiments the part was considered as a failure when DCL increased more than three times compared to initial value.

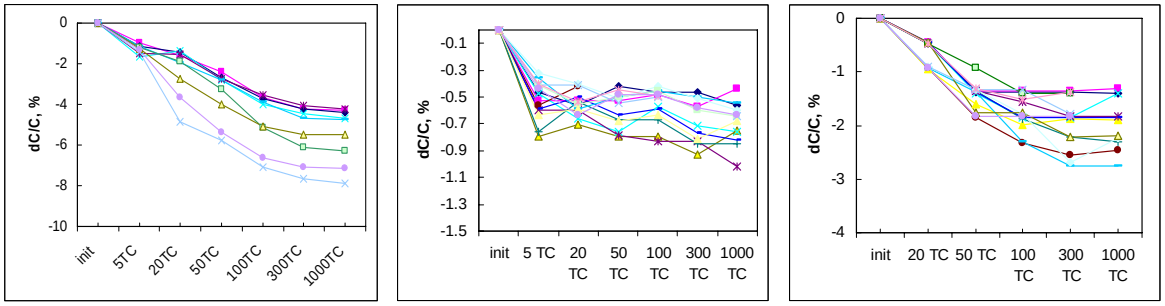
Monitoring of the I(t) characteristics was also used to detect scintillation events in the parts. These events are momentary breakdowns in the tantalum pentoxide, and their observation can be used to characterize quality of the dielectric [6]. Typically, in tantalum capacitors current relaxation after application of forward voltage is due to absorption currents and follows a power law: $I \sim t^{-n}$, where the exponent n is in the range from 0.8 to 1.1 [7]. On the I(t) curves, the scintillations appear as short-duration current spikes, which makes this technique a simple and reliable means for detection of the scintillation events.

The probability of surge current failures was estimated by measurements of the voltage, at which a failure during the step stress surge current testing (3SCT) occurs. During this test, the voltage was increased from the rated voltage in 2 V increments until the part failed. The testing was carried out using a PC-based data-capturing system with a field-effect transistor (FET) switch described in [8]. The current transients were monitored using an oscilloscope, and the failure event was determined when the current after the initial spike increased to more than 10 mA.

I.3. Test results

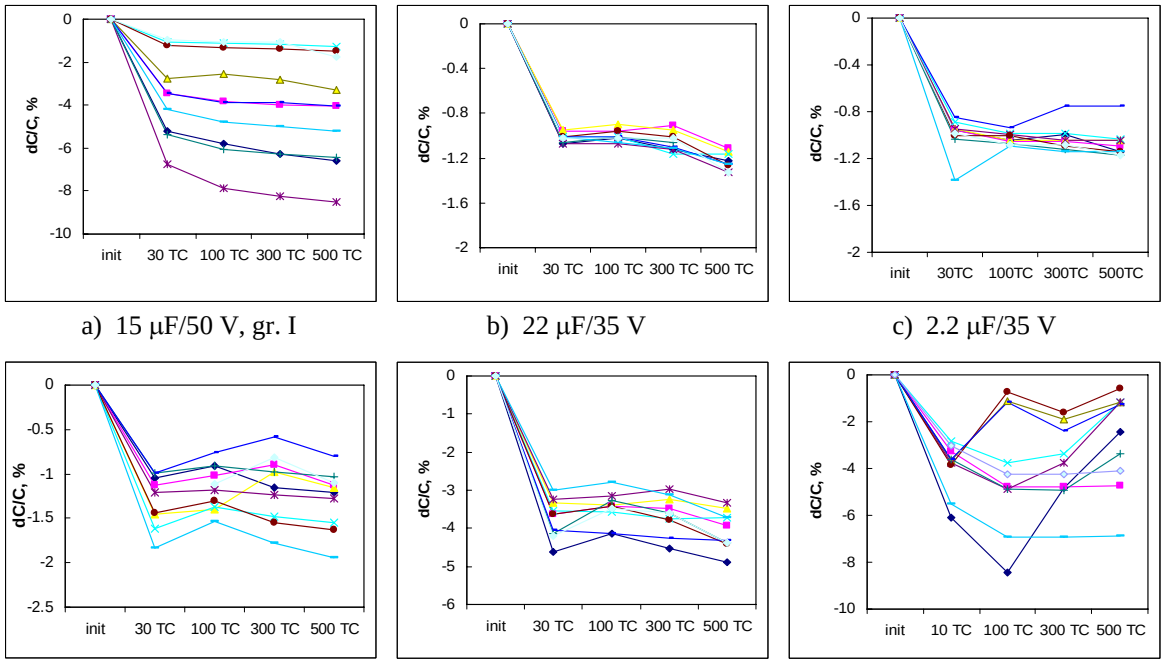
I.3.1 Effect of TC on capacitance

Variations of capacitance during temperature cycle testing are shown in Figures 1 and 2. In all cases, capacitance decreased during the first 10 to 100 cycles and then continued decreasing slowly or stabilized (except for 15 µF/50 V gr. II).



a) 10 µF/25 V b) 2.2 µF/10 V c) 22 µF/20 V

Figure 1. Variation of capacitance in military-grade parts during temperature cycling in the range from -65 °C to +125 °C.



a) 15 µF/50 V, gr. I b) 22 µF/35 V c) 2.2 µF/35 V

d) 10 µF/25 V e) 10 µF/50 V f) 15 µF/50 V, gr. II

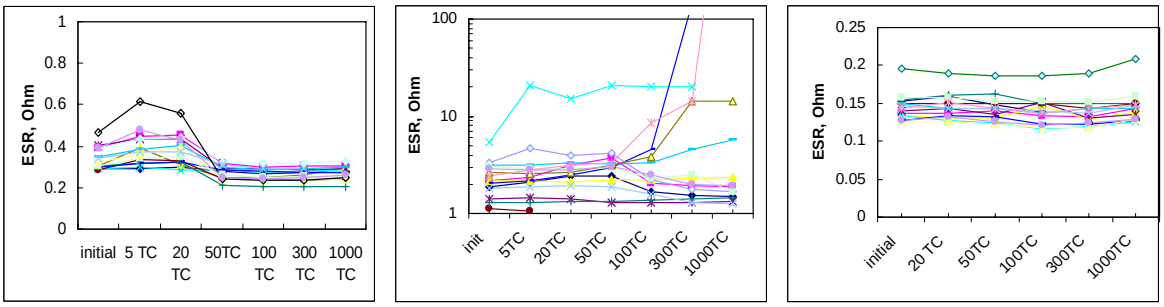
Figure 2. Variation of capacitance in commercial parts during temperature cycling in the range from -65 °C to +150 °C.

The results of cycling between -65 °C and +125 °C show that there is a trend for faster stabilization for smaller-sized capacitors (2.2 µF), where the major drop in C occurs after ~20 cycles. For larger-sized parts, the saturation in C occurs after ~300 cycles. Similar variations in capacitance were observed during cycling of commercial parts up to +150 °C. However, the decrease in C occurs relatively quickly and the capacitance stabilizes mostly after ~30 cycles. The level of the decrease of capacitance varies from ~8% for 15 µF/50 V devices to ~0.7% for 2.2 µF/10 V parts. There is no correlation between the nominal value of the part and its decrease during TC. Note that the behavior of two lots of 15 µF/50 V capacitors was different. Both lots had the most substantial changes during the first 10 to 30 cycles. However, in the first lot capacitance stabilized with the number of cycles, whereas in the second group most of the parts increased C after ~100 TC.

I.3.2 Effect of TC on ESR

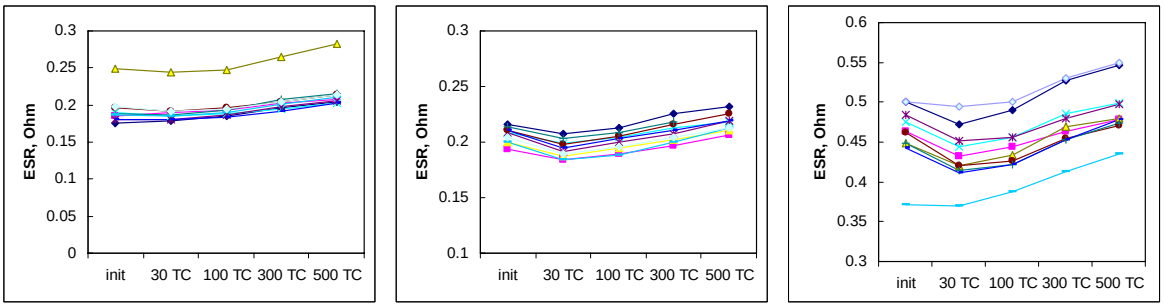
Results of testing the effect of TC on ESR are shown in Figures 3 and 4. Two out of three groups of military-grade capacitors, 10 µF/25 V and 22 µF/20 V, did not change the values of ESR significantly. However, the third group, 2.2 µF/10 V, had three failures, and two more parts had a trend of increasing ESR with the number of cycles.

For commercial leaded parts the ESR values did not change significantly with the number of cycles, whereas all chip capacitors manifested some trend of increasing of the ESR after ~30 to 100 cycles between -65 °C to +150 °C. However, this increase did not exceed ~20%, and all ESR values remained well below the specified limits.

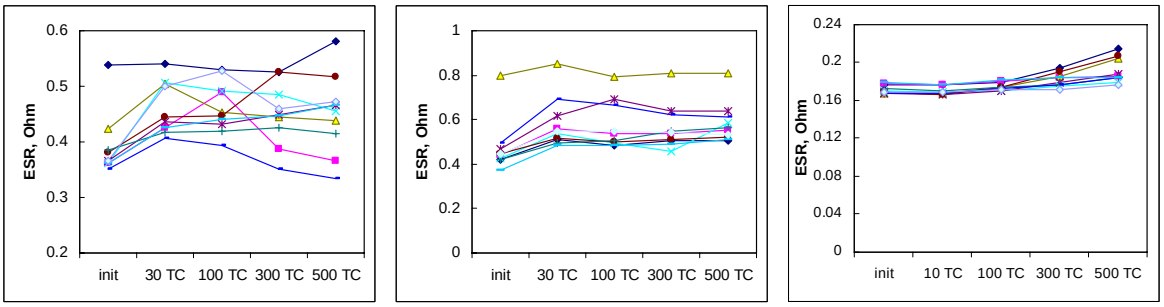


a) 10 µF/25 V, ESR_{max}= 1.4 b) 2.2 µF/10 V, ESR_{max}= 8 c) 22 µF/20 V, ESR_{max}= 0.9

Figure 3. Variation of ESR in military-grade parts during temperature cycling in the range from -65 °C to +125 °C.



a) 15 µF/50 V, gr. I, ESR_{max}= 0.3 b) 22 µF/35 V, ESR_{max}= 0.7 c) 2.2 µF/35 V, ESR_{max}= 4



d) 10 µF/25 V, ESR_{max}= 2.5 e) 10 µF/50 V, ESR_{max}= 1.6 f) 15 µF/50 V, gr. II, ESR_{max}= 0.3

Figure 4. Variation of ESR in commercial parts during temperature cycling in the range from -65 °C to +150 °C.

It was assumed that high initial ESR values might indicate potentially defective parts, which have a higher probability of failure during TC. To check this assumption, statistical characteristics of ESR distributions for the 2.2 μF/10 V lot, as well as several other lots manufactured by the same vendor, were analyzed and compared with the specified limits. Results of this analysis are shown in Table 2.

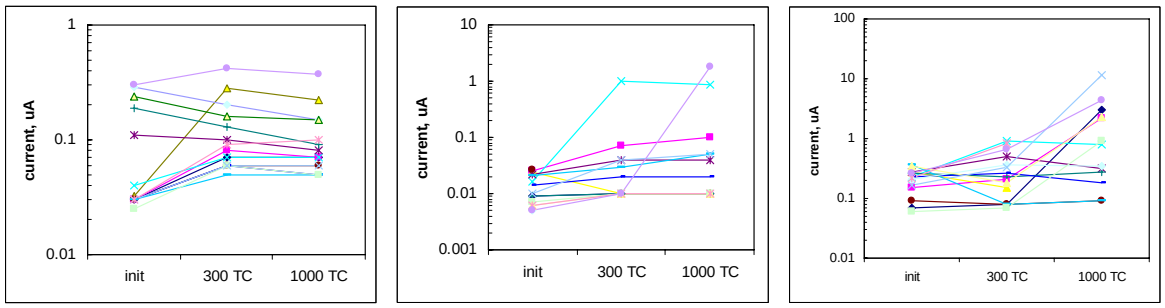
Table 2. Characteristics of ESR, Ohm, distributions for different lots of capacitors.

Capacitor	Capacitor	Qty.	Min.	Max.	Avr.	Std. Dev.	3σ Limit	Spec. Limit
CWR09KC106KC, DC9732	10 μF/25 V	36	0.21	0.46	0.30	0.07	0.51	1.4
CWR09FC225KBA, DC9732	2.2 μF/10 V	40	1.027	5.41	1.82	0.83	4.31	8
CWR09KC106KCA, DC9723	10 μF/25 V	78	0.21	0.44	0.27	0.045	0.405	1.4
CWR09JC226KC, DC 9804	22 μF/20 V	25	0.11	0.15	0.14	0.01	0.17	0.9
CWR09MC685KC, DC 9821	6.8 μF/35 V	27	0.16	0.23	0.19	0.015	0.235	1.3
CWR09NC475KC, DC 9822	4.7 μF/50 V	21	0.47	0.77	0.58	0.068	0.784	1.5

Note that although all 2.2 μF capacitors were within the specification limits, they had the greatest variation of ESR, and one sample exceeded the 3σ limit. The sample, which failed after 5 TC, had also the highest initial level of ESR. Although this value was below the specified limit (8 Ohms), it exceeded the 3-sigma level for this group. This reveals that excessive spreading of the ESR values might indicate the presence of potentially defective parts in the lot. Screening of a lot to pick up capacitors with the lowest ESR values might mitigate the risk and provide additional assurance in the quality of attachment and in mechanical robustness of the parts.

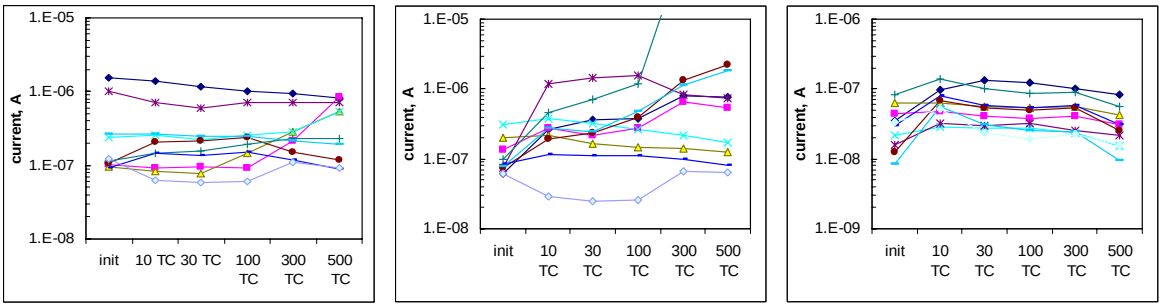
I.3.3 Effect of TC on leakage currents

Variations of leakage currents with the number of cycles for all tested parts are shown in Figures 5 and 6. Table 3 summarizes test results by displaying the proportion of parts with substantially increased leakage currents.



a) 10 μF/25 V, I_{max} = 3 μA b) 2.2 μF/10 V, I_{max} = 1 μA c) 22 μF/20 V, I_{max} = 4 μA

Figure 5. Variations of leakage currents in military-grade parts during temperature cycling in the range from -65 °C to +125 °C.



a) 15 μF/50 V, gr. I, I_{max} = 7.5 μA b) 22 μF/35 V, I_{max} = 7.7 μA c) 2.2 μF/35 V, I_{max} = 0.8 μA

d) 10 μF/25 V, I_{max} = 2 μA e) 10 μF/50 V, I_{max} = 4 μA f) 15 μF/50 V, gr. II, I_{max} = 7.5 μA

Figure 6. Variations of leakage currents in commercial parts during temperature cycling in the range from -65 °C to +150 °C.

Table 3. Failures due to increased leakage currents.

TC	2.2 μF/ 35 V	15 μF/ 50 V Gr. I	15 μF/ 50 V Gr. II	22 μF/ 35 V	10 μF/ 50 V	10 μF/ 25 V	2.2 μF/ 10 V	10 μF/ 25 V	22 μF/ 20 V
0	0	0	0	0	0	0	0	0	0
10	0	0	1/10	4/15	1/10	0			
30	0	0	1/10	5/15	2/10	0			
100	0	0	2/10	5/15	2/10	0			
300	0	1/10	3/10	6/10	2/10	0	1/15	1/15	0
500	0	1/10	3/10	6/10	2/10	0			
1000	-	-	-	-	-	-	2/15	1/15	4/15

The results show that only two lots, 2.2 μF/35 V and 10 μF/25 V, had no substantial variation of leakage currents during the testing, while all other lots had 10% to 60% of parts with increased currents. Note that in most cases the currents remained below the specified limits (except for two parts in the 22 μF/20 V group, one part in the 2.2 μF/10 V group, and one part in the 22 μF/35 V group) even after 500 and 1,000 cycles.

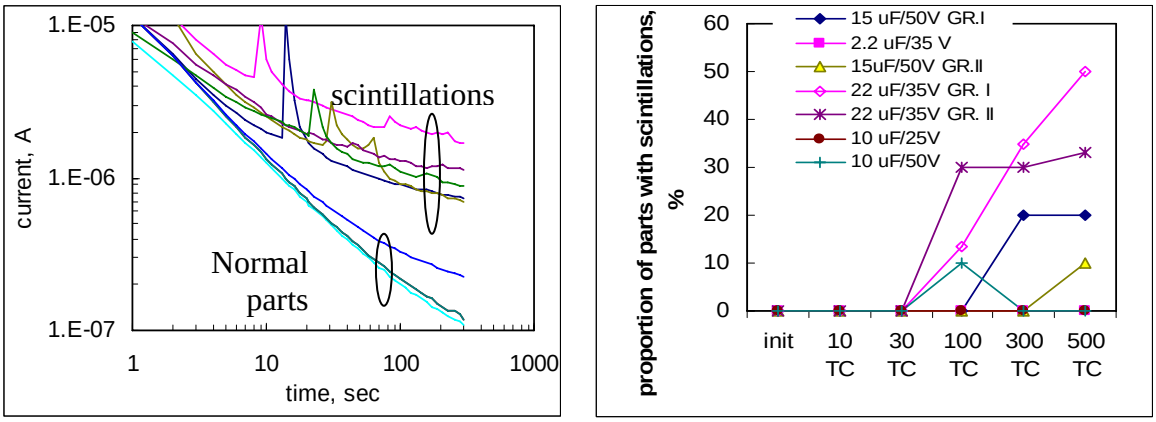
I.3.4 Effect of TC on breakdown voltages

Typical examples of scintillation events observed during I(t) measurements are shown in Figure 7a, where characteristics of the 22 μF/35 V parts tested after 300 temperature cycles are displayed. During these measurements, most of the parts had a relatively smooth decrease of the current after voltage application, and their I(t) characteristics follow the power law, $I \sim t^{-n}$, where $0.75 < n <$

0.95. However, some parts exhibited current spikes due to a short breakdown in the tantalum pentoxide caused by activation of some flaws in the dielectric. Note that all parts, with and without scintillations, have leakage currents below the specified limits, indicating that the compliance with the specified limits of DCL is not sufficient to assure high quality of the parts.

There was a certain correlation between scintillations and DCL; the parts exhibiting scintillations had larger values of DCL. This means that the parts having excessive leakage currents might have greater propensity to scintillations even when they have DCL below the specified limits, and they should not be used for high-reliability applications.

Variations of the proportion of parts with scintillations during TC for different groups of capacitors are shown in Figure 7b. Interestingly, no scintillations were observed in any of the tested parts up to 30 cycles. However, by 500 cycles only two groups, 2.2 μF/35 V and 10 μF/25 V, had no scintillations, whereas the proportion of defective parts in other groups varied from 10% to 50%. There is a clear trend of the probability of scintillations increasing with the number of thermal cycles.



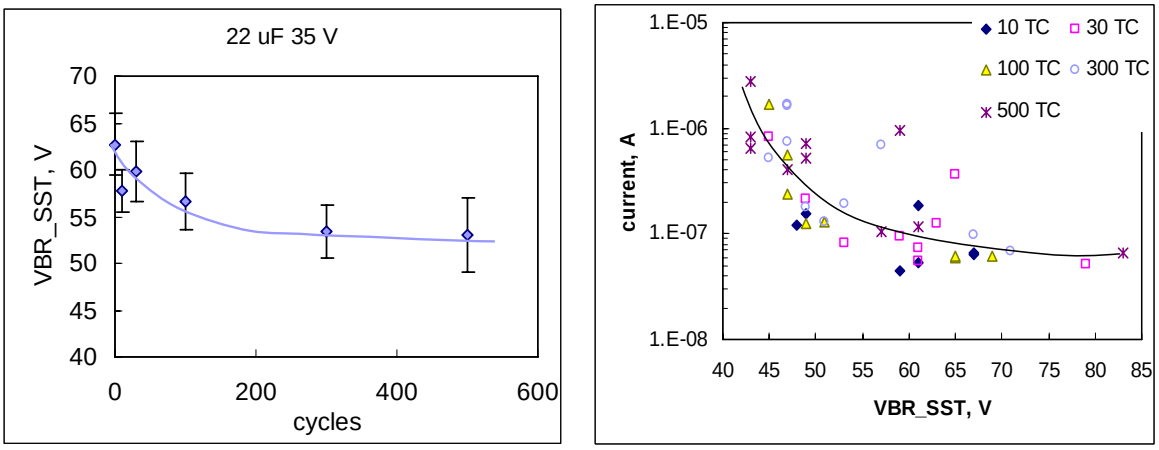
a) b)

Figure 7. I-t characteristics for the 22 μF/35 V capacitors showing normal parts and parts with scintillations (a) and variation of the proportion of devices with scintillations with the number of TC (b).

Step stress surge current breakdown voltages were measured for 22 μF/35 V capacitors periodically during TC. Due to the destructive nature of this test, a group of 60 samples was used for this testing, and each time during the interim measurements 10 parts were destructively tested and removed from the group. Based on results of these tests, average breakdown voltages, VBR_3SCT, and their standard deviations were calculated. Variations of VBR_3SCT with the number of cycles are shown in Figure 8a. It is seen that the breakdown voltage gradually decreased during TC testing and varied from 62.7 V initially to 55.4 V after 500 TC.

Several publications have reported that there is no correlation between the level of leakage current and the probability of surge current stress failures [9, 10]. However, our data (see Figure 8b) accumulated during these experiments indicate that there is a trend of decreasing surge current breakdown voltage for capacitors with greater leakage currents. It is possible, however, that this

trend is a result of two different mechanisms occurring during TC, one of which causes an increase in DCL and another one a decrease in VBR_3SCT.



a) b)

Figure 8. Variation of breakdown voltage during 3SCT with number of cycles (a) and correlation between the VBR_3SCT and leakage current (b).

I.4. Discussion

I.4.1 Capacitance variations

A decrease in capacitance during TC is due most likely to moisture desorption from the part occurring during the high-temperature periods of cycling. As was shown in our previous work [11], in humid environments moisture condenses in gaps between tantalum pentoxide and manganese cathode, thus increasing the effective area of the electrodes. Typical variations of capacitance caused by moisture sorption at room temperature and ~ 50% RH are in the range from 2% to 10%, and the time for capacitance stabilization during baking at 150 °C is less than 24 hours and at 125 °C is less than 72 hours. Considering that the dwell time at high temperatures during TC is 15 min., this corresponds to less than 100 cycles for 150 °C TC and less than 300 cycles for 125 °C TC. These estimations show that both the value of capacitance decrease and the rate of changes agree with the moisture desorption model.

Variations of capacitance during TC are not related to any degradation process in the tantalum pentoxide dielectric and most likely are not a reliability concern. For this reason, the requirement of MIL-PRF-55365 for capacitance to remain within 5% limits after TS is not justified. More than that, according to the sleeping cells model [11], moisture desorption might be beneficial for reliability of the part. However, a decrease of capacitance during TC for the parts, which had initially the value of capacitance close to the lower limit, would move the part out of specification and formally might be considered as a failure. This failure should be taken into account only if a relatively minor decrease of capacitance would cause malfunction in the system where the part is used, which is not the case for many applications.

It is interesting to note that TC does not affect capacitance of ceramic devices. According to [12], there was no significant difference in capacitance values of ceramic capacitors of various sizes before and after thermal shock. Failures of high-voltage Y5U ceramic capacitors subjected to 300

cycles between -40 °C and +120 °C were due to increased IR, whereas capacitance and dissipation factors remained unchanged [13]. However, multiple cryo-cycling of X5R ceramic capacitors between room temperature and 77 K resulted in 10% to 20% decrease in C [14]. The mechanism of this degradation is not clear.

I.4.2 ESR variations

Typically, for devices with good cathode attachment, the resistivity of the manganese layer is considered as a major contributor to the ESR of a tantalum capacitor. However, the resistance of interfaces between different conductive layers of the parts' constitution (manganese, carbon graphite coating, silver paint, silver epoxy, cathode metal) is also critical to assure low ESR values. It was assumed that during TC the mismatch of the coefficient of thermal expansion (CTE) between encapsulating molding compound, metal frame, and silver epoxy would disrupt the interfaces, in particular between the silver epoxy and metal, cause delaminations, increase the resistance of the interface, and thus degrade ESR of the parts.

Out of nine tested lots in our experiments, only one, 2.2 μF/10 V, had ESR failures. Other chip tantalum capacitors manifested only minor (less than 20%) increase in ESR after ~30 cycles. Note that the failed lot was from the same manufacturer that had attachment problems during the period from 1997 to 2000. X-ray images of the part from this lot confirmed poor cathode attachment (see Figure 9).

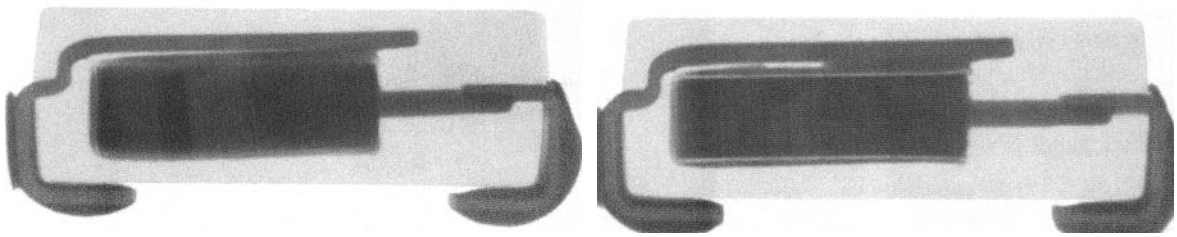


Figure 9. X-ray views of the 2.2 μF/10 V parts indicating a poor cathode attachment.

The results suggest that normally, silver epoxy attachment can provide reliable connection of the slug to the cathode terminal, and chip tantalum capacitors are capable of withstanding multiple TC in the military range of temperatures without significant ESR degradation. Non-adequate attachment is a result of poor manufacturing control over the attachment process or materials used, and degradation of ESR during TC might be used as an indicator of these types of deficiencies. Note that measurements of ESR after TS are optional per MIL-PRF-55365. This, as well as a limited number and temperature range of cycling used in the MIL standard, allows potentially defective parts to pass through the screening and qualification process.

I.4.3 Leakage current variations

Considering the sponge-like structure of a tantalum slug; extremely thin dielectric (Ta_2O_5) used; and significant difference in CTE between polymer encapsulant, manganese oxide filling pores in the slug, and tantalum, one might expect that substantial local mechanical stresses would develop inside the slug during TC, resulting in micro-cracking of the dielectric. It is also reasonable to assume that this micro-cracking might cause an increase in leakage currents and failures of the parts.

Three out of nine lots had DCL failures, which exceeded the specified limits, and in seven lots 10% to 60% of the devices manifested a significant increase in leakage currents. In many cases, increased currents did not deteriorate further with increased numbers of cycles. This can be explained assuming that the fatigue-induced cracking ceases to develop as soon as the mechanical stresses are relieved.

Although cracking-induced leakage currents remain relatively low, cracking of the dielectric might facilitate breakdown phenomena and cause scintillations and surge current failures. Note that the two lots, 2.2 μF/35 V and 10 μF/25 V, which had no DCL failures, had also no scintillation failures. This suggests that degradation of leakage currents during TC can be used as an indicator of the quality of the lot.

I.4.4 Breakdown voltage variations

Cracking in tantalum pentoxide dielectric, which develops during TC, results not only in increased leakage current, but also increases the probability of scintillation breakdowns. A correlation between the proportion of leakage current failures and portion of parts manifesting scintillations after 500 TC (see Figure 10) confirmed this hypothesis. Similar to leakage currents, in some cases the proportion of parts with scintillations does not increase further with the number of cycles.

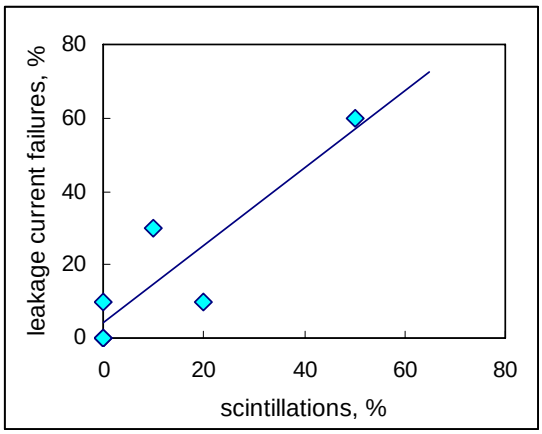


Figure 10. Correlation between leakage current failures and scintillations after 500 TC.

Temperature cycling resulted in a relatively small (~12%) decrease in the step stress surge current test voltage. Although this decrease is not substantial, it might result in a rather significant increase in the probability of failures of the parts. Assume that the distribution of VBR_3SCT follows a simple two-parameter Weibull distribution as shown in Figure 11, where the experimental data are approximated with distributions having slopes β ~6.2. In this case, for a part derated to 20 V, the probability of failure due to a surge current event is ~0.06% initially, and it increases more than two times, up to ~0.15%, after 500 TC. It is quite possible that the distribution of VBR_3SCT is bimodal and the low-voltage group of devices has a much larger beta. In this case, the effect of TC on the probability of breakdown would be much more significant. More data are necessary to accurately estimate the VBR-3SCT distribution and its variation caused by temperature cycling.

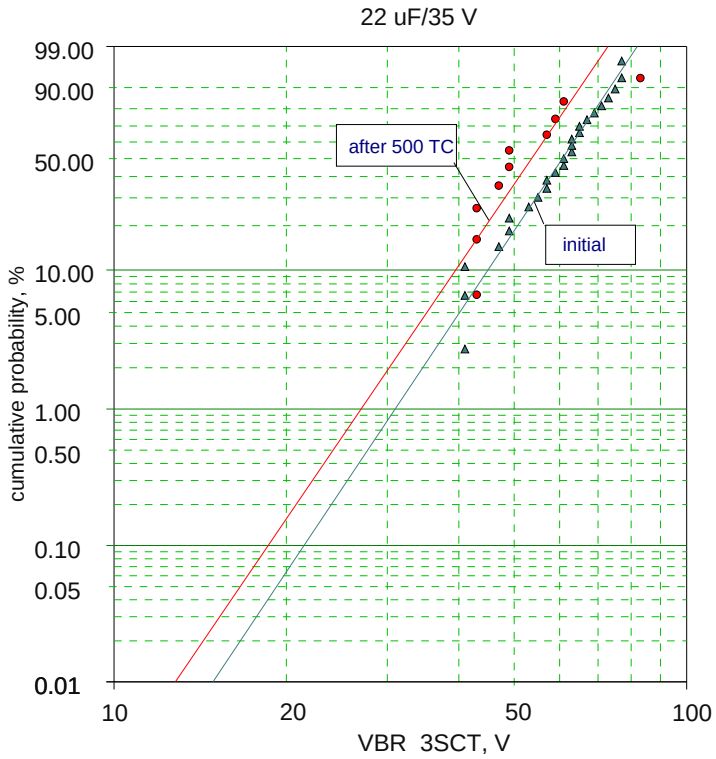


Figure 11. Effect of temperature cycling on distributions of breakdown failures during step stress surge current testing of 22 μF/35 V parts.

Our data indicate an increased probability of failures under surge current conditions after TC for some types of molded chip tantalum capacitors. This is in agreement with the results of R. Franklin [3], who reported that the surge performance of resin-dipped capacitors was also deteriorated by temperature cycling.

I.5. Conclusion

1. Three groups of military-grade capacitors and six groups of commercial tantalum capacitors were subjected to multiple temperature cycling in the range from -65 °C to +125 °C and -65 °C to +150 °C. The results indicate that the parts are capable of withstanding up to 500 TC in the temperature range from -65 °C to +150 °C. However, different lots have different robustness under TC conditions and, although the parts might not fail formally by exceeding the specified limits, a significant degradation in leakage current and breakdown voltages indicates an increased propensity to failure after TC.
2. Temperature cycling up to 150 °C results in decrease in capacitance of 1% to 8%, with most changes occurring after first 10 to 30 cycles. This decrease is most likely due to moisture desorption from the manganese/tantalum pentoxide interface and does not pose a reliability risk.
3. No substantial degradation of ESR was observed in eight out of nine lots even after 1,000 TC. ESR failures in one lot were likely due to poor attachment during manufacturing. This lot had also excessive ESR scattering, which might be used as an indicator of manufacturing

deficiencies. Parts with relatively large ESR values, exceeding the 3-sigma limit, might have a higher probability of failure during temperature excursions and should not be used for high-reliability applications.

4. Leakage current is a much more sensitive testing parameter to TC compared to capacitance and ESR. Significantly increased DCL after TC was observed in seven out of nine tested lots, and three lots had failures due to exceeding the specified DCL limits. There was no substantial difference in the behavior of commercial and military parts, probably due to the lack of requirements for TC in MIL-PRF-55365.
5. There is a trend of increasing scintillation breakdowns with the number of cycles. No scintillations were observed up to 30 TC, but by 500 TC only two out of nine lots had no scintillations. TC might increase the probability of surge current failures; an average breakdown voltage during step stress surge current testing of 35 V capacitors decreased from 62.7 V initially to 55.4 V after 500 cycles.
6. The requirements of MIL-PRF-55365 regarding TC testing are much less severe compared to ceramic capacitors and microcircuits and are not sufficient to assure the necessary reliability in military-grade hybrids without additional testing. The requirement for ESR measurements after TS during screening should be made mandatory in MIL-PRF-55365, whereas the requirement for capacitance to remain within the 5% limits is not necessary.
7. At least a 100-cycle test within the military range of temperatures should be included in the MIL-PRF-55365 standard, and variations of DCL, ESR, and breakdown voltages should be used to assess the results of this testing. The relevant techniques for breakdown voltage measurements (scintillations and step stress surge current testing) should be specified and used for assessment of the robustness of tantalum chip capacitors.

Part II. Effect of Exposure to Soldering Temperatures on Chip Tantalum Capacitors

II.1. Introduction

Soldering reflow is one of the most stressful processes for all surface mount technology (SMT) components, and for solid chip tantalum capacitors in particular. Due to mismatch of the coefficients of thermal expansion (CTE) between the constituent materials (molding compound, tantalum, manganese, silver epoxy, and metal frame), significant mechanical stresses develop in the bulk of materials and at the interfaces. These stresses might cause cracking in the tantalum pentoxide dielectric and/or delaminations at the interfaces, resulting in different failure modes of the parts. The cracking increases leakage currents, decreases breakdown voltages, and might cause short-circuit catastrophic failure of the part. On the other hand, delaminations would raise the effective series resistance (ESR), thus increasing power dissipation and temperature of the capacitor and thereby decreasing its reliability. Severe delaminations might result in intermittent contacts and open-circuit failures of the parts.

Available literature data indicate the possibility of inducing damage to the parts during the soldering process. Edson and Fortin [4] showed that immersion of tantalum chip capacitors into molten solder can increase leakage currents from 0.1 μA to ~100 μA. It was also noted that devices manufactured by different vendors showed different sensitivity to the solder dipping test. Marshall and Prymak [5] indicated that solder reflow conditions in some cases might affect the results of the step stress surge current testing (3SCT) and cause surge current failures. To mitigate problems developed during reflow soldering in tantalum capacitors, a special technique called "proofing" is recommended in [15]. It is assumed that proofing, or controlled power-up of the part after assembly, allows activation of the self-healing effects in tantalum capacitors, and thus reduces failures in low-impedance applications.

A rapid increase of temperature during the solder reflow process might result in a phenomenon specific to plastic encapsulated components and well known for commercial microcircuits, the so-called pop-corning effect. This phenomenon is due to the presence of moisture in polymer materials. When moisture absorbed within the bulk of material or trapped at the interface between molding compound and assembly is rapidly vaporized at high temperatures, a substantial vapor pressure and mechanical stresses develop. In tantalum capacitors, these stresses might be sufficient for causing damage to a thin tantalum pentoxide layer or fracturing the package. This phenomenon was thoroughly studied and is now well contained for plastic encapsulated microcircuits (PEMs). However, the possibility of this effect for chip tantalum capacitors has not been investigated yet.

In this work, deformation of chip tantalum capacitors during temperature variations simulating reflow soldering conditions was measured to evaluate the possibility of the pop-corning effect in the parts. To simulate the effect of short-time exposures to solder reflow temperatures on the reliability of tantalum capacitors, several part types were subjected to multiple cycles (up to 100) between room temperature and 240 °C with periodical measurements of electrical characteristics of the parts. The requirements of MIL-PRF-55365 for assessment of the resistance of the parts to soldering heat are analyzed, and recommendations for improvements of the qualification testing are discussed.

II.2. Experiment

Temperature dependencies of deformation of chip tantalum capacitors and epoxy molding compounds were measured using a thermal mechanical analyzer, TMA2940, manufactured by TA Instruments. Characteristics of molding compounds, including the glass transition temperature (Tg) and coefficients of thermal expansions, were measured on small pieces of the devices cut from the packages. These measurements were carried out at a rate of 3 $^{\circ}$C/min. during cooling from 220 $^{\circ}$C, followed by heating of the sample in the analyzer at the same rate. This allowed for monitoring of the stress relief in the sample and assured elimination of possible errors related to the presence of moisture and built-in mechanical stresses. Measurements of deformations of the packages were carried out directly on the parts with a probe placed on the back surface of the plastic case. During these measurements, the heating rate was varied from 3 $^{\circ}$C/min. to 20 $^{\circ}$C/min. to simulate soldering reflow conditions. Figure 1 shows a set-up used for TMA measurements.

a) b)

Figure 1. Overall view of the TMA set-up (a) and a view of a tantalum capacitor under the quartz probe (b) with a heating chamber in the upper position.

Multiple cycling to high temperatures (240 $^{\circ}$C) was carried out at a heating rate of 20 $^{\circ}$C/min. using the TMA chamber. The duration of exposure to high temperatures, 239 $^{\circ}$C < T < 241 $^{\circ}$C, was ~60 seconds. Temperature of the samples was monitored during the cycling, and Figure 2 shows an example of temperature variations during high-temperature (HT) cycling.

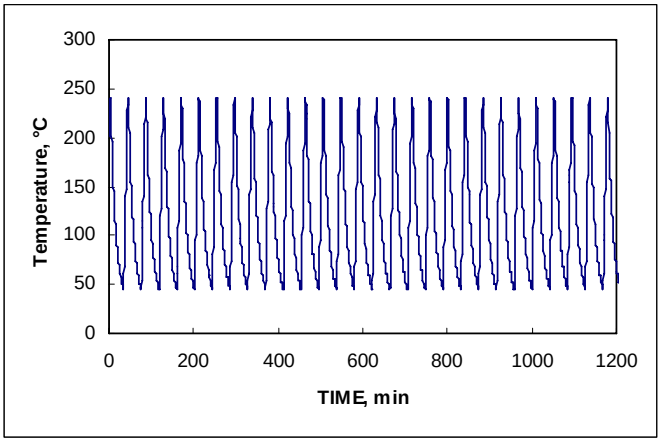


Figure 2. Temperature profile during high-temperature cycling of the parts.

Four groups of capacitors described in Table 1 were used in this study. Each group had 12 to 15 parts and was subjected to 30 cycles (one group was subjected to 100 cycles) with interim measurements after 1, 3, 10, and 30 cycles. Measurements of the AC characteristics including capacitance (C) and effective series resistance (ESR) were carried out using an HP4192A impedance analyzer. Leakage currents (DCL) were measured at rated voltages while monitoring I(t) characteristics using an HP4156 precision semiconductor analyzer. The DCL reading was taken 5 minutes after voltage application.

Table 1. Characteristics of tantalum capacitors.

Part	Type	DC	C Limit, %	ESR Limit, Ohm	DCL Limit, μA
15 μF/50 V	T495X156M050AS	DC 0405	± 20	0.3	7.5
22 μF/35 V	T491D226M035AS	DC 0408	± 20	0.7	7.7
4.7 μF/50 V	CWR09NC475KC	DC 9822	±10	1.5	3
22 μF/ 20 V	CWR09JC226KC	DC 9826	± 10	0.9	4

The susceptibility of the parts to surge current failures was estimated by measurements of the breakdown voltages, at which failures during the step stress surge current testing (VBR_3SCT) occur. During this test, the voltage was increased from the rated one in 2 V increments until the part failed. The testing was carried out using a PC-based data-capturing system with a FET switch described in [8]. The current transients were monitored using an oscilloscope, and the failure event was determined when the current after the initial spike increased to more than 10 mA.

II.3. Thermo-mechanical characteristics of chip tantalum capacitors

Typical results of deformation measurements carried out on 15 μF/50 V capacitors along and across the part at a rate of 3 °C/min. are shown in Figure 2. The TMA characteristics of the molding compound used, which were measured on a piece cut from the part, are also shown on this chart.

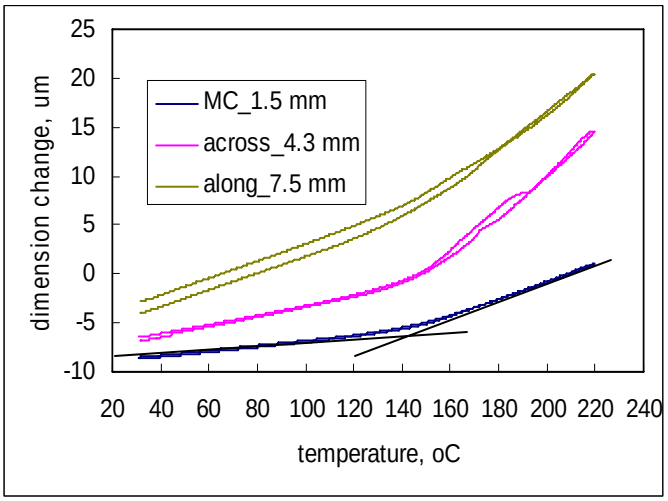


Figure 3. Thermo-mechanical characteristics of a chip tantalum 15 μF/50 V capacitor.

The effective CTE values in glassy (low temperatures) and rubbery (high temperatures) states were calculated as slopes of the curves, whereas a point of inflection of the two straight lines determined the value of Tg. Results of these calculations for 50 μF/50 V capacitors and molding compound (MC) are displayed in Table 2.

Table 2. TMA characteristics of 15 μF/50 V capacitors.

	Tg, °C	CTE1, ppm/°C	CTE2, ppm/°C
Cap. Along	144.2	11.4	26.3
Cap. Across	150.8	11.6	56.4
MC	143.3	17.3	59.2

The results show that the glass transition temperature measured on capacitors and on MC were close and ranged from 144 °C to 151 °C, whereas the effective values of CTE in a glassy state for the part, ~11.5 ppm/°C, were much less than CTE for the MC, 17.3 ppm/°C. A decrease of the effective CTE measured on the part compared to the MC is obviously due to the presence of tantalum slug, which has a CTE = 6.6 ppm/°C and constrains the deformation of the molding compound.

When TMA measurements were carried out on tantalum capacitors at a rate of 20 °C/min., anomalous deformation spikes were detected during the first heating run. Figure 4 shows typical results of these measurements where a spike occurred at ~200 °C, but no anomalies were observed up to 240 °C during the second measurement cycle.

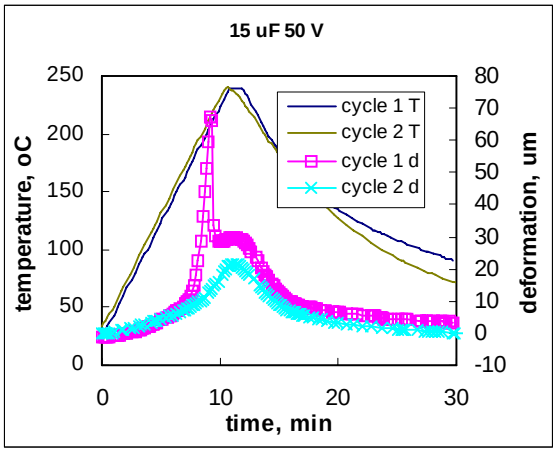
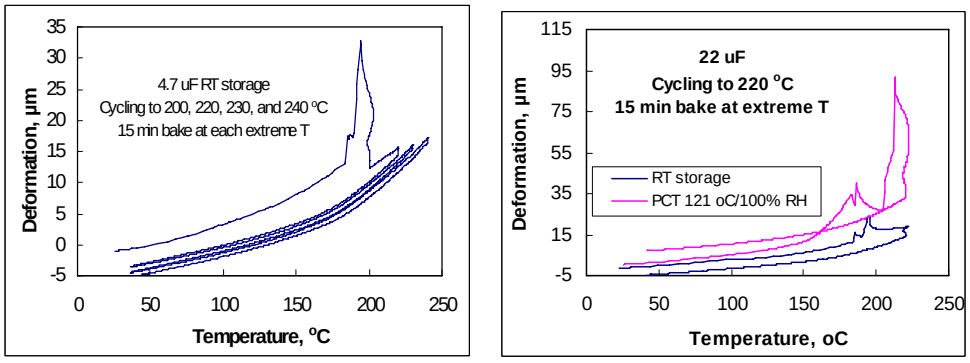


Figure 4. A deformation spike during the first heating cycle on a 15 μF/50 V capacitor. Unmarked lines show temperature variations, and marked lines show deformation of the part.

Figure 5a displays results of experiments where 4.7 μF/50 V capacitors were measured at a rate of 20 °C/min., first up to 200 °C, then to 220 °C, 230 °C, and 240 °C. After each temperature extreme, the part was cooled to room temperature. It is seen that the spike appeared during the first temperature cycle only, and cycling to higher temperatures did not cause any anomalies in the deformation.

The effect of moisture preconditioning on deformation spikes was investigated using 22 μF/35 V capacitors. Three groups with three to five samples each were preconditioned at different humid environments: Group I was stored in laboratory conditions for 3 months at RH ~40% at room temperature, group II was stored for 1 month in vacuum at room temperature, and group III was moisturized for 96 hours at 121 °C/100% RH (pressure cooker test). Figure 5b shows typical TMA characteristics measured on group I and group III devices having substantial deformation spikes. Parts from the second group did not have substantial spiking.



a) b)

Figure 5. Effect of maximum temperature during HT cycling of 4.7 μF capacitors (a) and effect of moisture preconditioning of 22 μF/35 V capacitors (b) on deformation spikes.

Results of the tests on all groups are summarized in Table 3 and indicate a clear trend of increasing of the amplitude of spikes after moisture sorption.

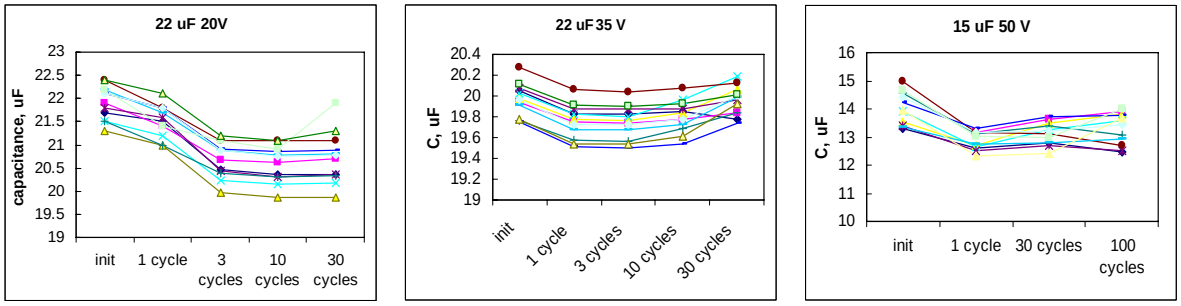
Table 3. Amplitudes of deformation spikes, μm, during reflow soldering simulation.

Condition	N	Average	St. Dev.
Long RT	5	17.6	3.7
Vacuum Storage	3	3.8	5.4
121 °C/100% RH	4	47.5	18.6

II.4. Results of high-temperature cycling

II.4.1 Effect on capacitance

Figure 6 shows variation of capacitance with the number of HT cycles. All parts decreased their capacitance after the first one to three cycles. This decrease varied from 5% to 7% for 22 μF/20 V parts, from 0.9% to 1.3% for 22 μF/35 V parts, and from 2.5% to 12% for 15 μF/50 V capacitors.

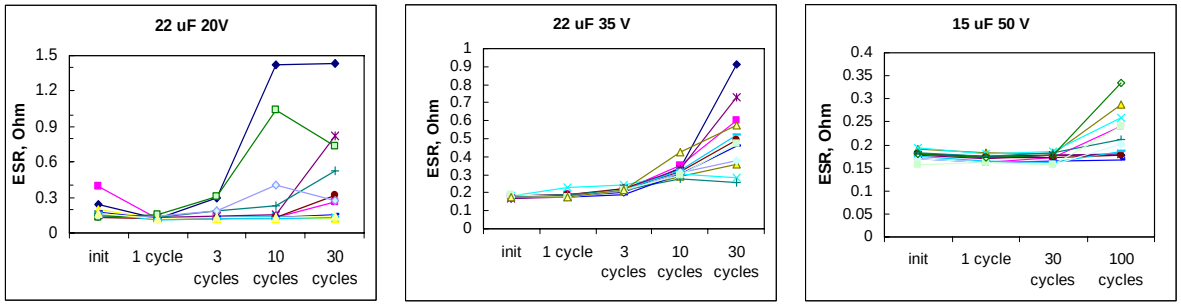


a) b) c)

Figure 6. Effect of high-temperature cycles on capacitance.

II.4.2 Effect on ESR

The effect of HT cycles on effective series resistance of the parts is shown in Figure 7. In all cases, there is a clear trend of increasing of ESR after 10 to 100 cycles. Two out of 12 22 μF/20 V parts exceeded the specified limit of 0.9 Ohm after 10 cycles, five parts did not change ESR significantly, and the others increased ESR by two to five times after 30 cycles. In the 22 μF/35 V group, one part exceeded the specified limit after 30 cycles, and all others increased ESR values by 1.5 to 5.5 times. All 15 μF/50 V capacitors had stable ESR values after 30 HT cycles, but after 100 cycles one part failed the specified limit, five parts had no significant variations, and the others increased ESR by 20% to 80% only.

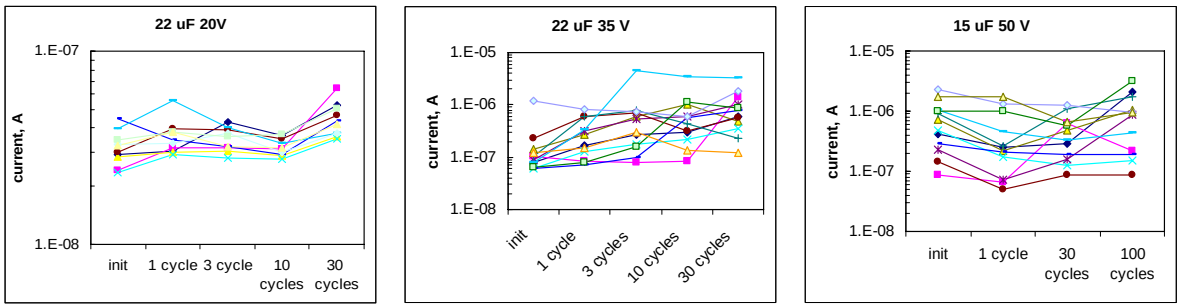


a) limit 0.9 Ω b) limit 0.7 Ω c) limit 0.3 Ω

Figure 7. Effect of high-temperature cycles on ESR. Captions indicate specified ESR limits for the parts.

II.4.3 Effect on DCL

Results of the leakage current measurements during HT cycling are shown in Figure 8. No substantial increase in DCL was observed for 22 µF/20 V parts. Eight out of 12 22 µF/35 V samples increased leakage currents significantly, from three to 40 times. However, these parts did not exceed the specified limit. Only three out of 12 15 µF/50 V capacitors increased DCL by three to five times between 30 and 100 cycles, whereas all other parts had no significant variations.



a) b) c)

Figure 8. Effect of high-temperature cycles on leakage currents.

II.4.4 Effect on surge current testing

Results of step stress surge current testing of capacitors before and after HT cycling are summarized in Table 4. The table shows statistical characteristics of the breakdown voltages and results of the analysis based on Student's t-test. At the confidence level of 95%, only 22 µF/35 V parts had significant decrease in the breakdown voltage from 60 V initially to 48 V after 30 HT cycles. Note that as was shown in the previous section of the report, the same lot had a significant decrease in the breakdown voltages after 500 temperature cycles between -65 °C and +150 °C. Variations in VBR_3SCT in other two groups after HT cycling were not significant.

Table 4. Effect of high-temperature cycling on VBR_3SCT.

Part	Initial			After HT Cycling			Analysis		
	Qty.	Avr.	St.	Qty.	Avr.	St.	T	df	$t_{crit,\ p=0.95}$
22 µF/20 V	10	55.8	9.8	12	53.3	8.9	0.62	18.48	2.10
22 µF/35 V	25	60	10.9	12	48	4.5	4.73	34.56	2.03
15 µF/50 V	8	82.4	11.6	8	90	16.9	-1.05	12.40	2.18

The Student's t-test parameters were calculated according to equation (1), and the degree of freedom (df) was calculated per equation (2).

$$t = \frac{X1 - X2}{\sqrt{\frac{S1^2}{n1} + \frac{S2^2}{n2}}} \quad (1), \qquad df = \frac{\left(\frac{S1^2}{n1} + \frac{S2^2}{n2}\right)^2}{\frac{\left(S1^2/n1\right)^2}{n1-1} + \frac{\left(S2^2/n2\right)^2}{n2-1}} \quad (2),$$

where X1 and X2 are average values, S1 and S2, are standard deviations, and n1 and n2 are numbers of samples.

II.5. Discussion

II.5.1 Pop-corning effect in tantalum capacitors

Deformation spikes during TMA measurements of tantalum capacitors increased with the moisture content of the part and were observed at the first heating cycle and at high heating rates only. The temperature of these spikes was in the range of 180 °C to 200 °C. Similar results were obtained for plastic encapsulated microcircuits. Direct measurements of the deformation during simulated solder reflow on moisturized QFP-132 package style devices revealed deformation spikes up to 200 μm at T ~180 °C [16].

Our results indicate that the pop-corning effect can happen in chip solid tantalum capacitors encapsulated in molding compounds during soldering. However, contrary to plastic encapsulated microcircuits, fractures of the package in tantalum capacitors are relatively rare events. This might be due to a difference in the package design between plastic microcircuits and capacitors allowing relatively large deformations in capacitors to occur without cracking of the package. Nevertheless, excessive deformations of the molding compound in tantalum capacitors during soldering might create substantial mechanical stresses and cause degradation of characteristics or failures in the parts. For this reason, baking of the devices before soldering (e.g., 150 °C for 8 hours) is recommended to reduce the risk of damaging of the parts intended for use in high-reliability applications.

II.5.2 Effect of HT cycling on capacitance

A decrease in capacitance after one to three HT cycles is most likely due to moisture desorption from the part, which removes water condensed in micro-voids along the tantalum pentoxide/manganese interface and thus reduces the effective area of the cathode and capacitance of the part [11]. Note that as was shown in the previous section of the report, a similar decrease in capacitance was observed after temperature cycling and was also related to the moisture desorption process.

Based on temperature dependencies of diffusion characteristics of molding compounds used in tantalum capacitors [11], the diffusion coefficient at 240 °C is $D \sim 5\times10^{-6}$ cm^2/s. Using this value, the characteristic time of moisture diffusion in the package can be estimated as:

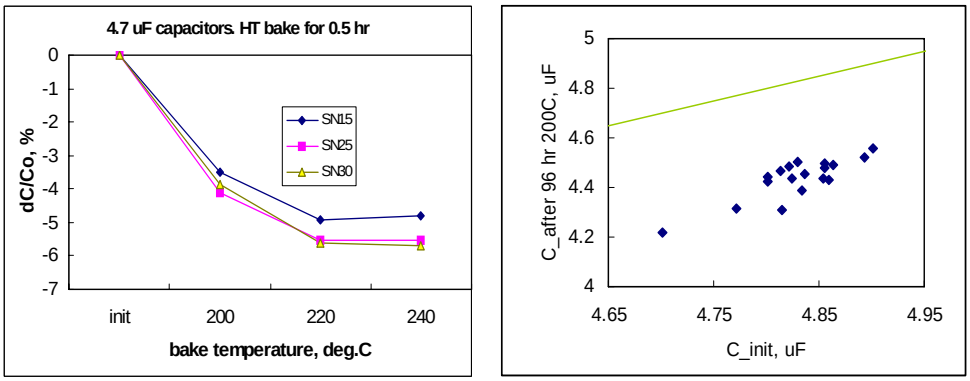
$$\tau_D(T) = h^2/D(T),$$

where h is the thickness of molding compound. At h ~0.3 mm τ_D = 180 s. Although this value is greater than the duration of one HT cycle in our experiments (~60 s), a substantial amount of moisture will be desorbed out of the package during first one to three cycles. The duration of HT exposure of the parts during the real soldering process is ~10 s, which might not be sufficient to substantially dry out the part. However, at temperatures significantly exceeding the glass transition temperature of the molding compound, a gap between the tantalum slug and lead frame will be formed, thus substantially enhancing out-diffusion of moisture from the surface of tantalum pentoxide dielectric.

The values of decrease in capacitance caused by HT cycling are in a good agreement with the values of DC measured for 22 μF/35 V and 15 μF/50 V capacitors after cycling in the military range of temperatures (see section I.3.1). However, the results are substantially different (5% to 7% after HT cycling and 1.5% to 2.5% after mil-range cycling) for 22 μF/20 V capacitors. This is

due to the fact that the same date code parts were used for cycling of the 22 μF/35 V and 15 μF/50 V capacitors, whereas 22 μF/20 V parts had a different date of manufacturing indicating that moisture-related variations of capacitance are lot related.

To assess the effect of exposure to high temperatures on capacitance, a group of 4.7 μF/50 V devices was baked at 200, 220, and 240 °C for 0.5 hour, and another group of these capacitors was stored at 200 °C for 96 hours. Results of these tests are shown in Figure 9. It is seen that most changes occur after 200 °C bake, capacitance stabilizes after 220 °C bake, and there are no significant changes after storing at 240 °C for 30 min. All parts after 96 hours bake at 200 °C decreased C from 5% to 10%, which is consistent with the moisture out-diffusion model.



a) b)

Figure 9. Typical results of 30 min. bake at 200, 220, and 240 °C (a) and 96 hours bake at 200 °C on capacitance of 4.7 μF/50 V capacitors. A green line in Figure 9b shows "no change" conditions.

Different lots of tantalum capacitors might reduce the value of capacitance due to the moisture removal on 1% to 15% and, similar to temperature cycling, this decrease does not pose any reliability risk to the parts. However, MIL-PRF-55365 requires that the capacitance after resistance to soldering heat test should remain within 5% of its initial value. Note that this is the only parameter that is required to be stable after this test. As our results show, variations of C on more than 5% after soldering simulations are possible, they do not reflect any degradation processes in the part, and they are probably harmful. Failures during this test might be misleading and result in formal rejection of a normal quality lot. Note also that these failures could be easily avoided if the parts are baked before initial measurements and/or are stored for long enough to allow moisture sorption after the testing.

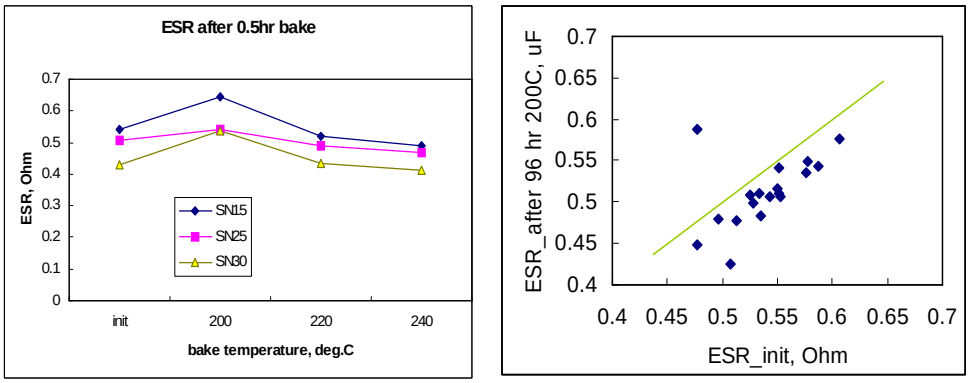
II.5.3 Effect of HT cycling on ESR

Soldering-related failures due to increased ESR or open circuit are relatively rare but still are known events in the history of applications of tantalum capacitors in high-reliability systems. J. Brusse [17] analyzed failures of military CRW09-style capacitors produced by one manufacturer during the period from 1997 to 2000. Out of 31 failure cases, only six were due to short circuit and 25 to open circuit. Two open-circuit failures were caused by a poor anode wire attachment, but the majority of the parts failed due to the cathode detachment. In most cases, this detachment was triggered by a solder reflow process and is believed to be due to degradation of the silver epoxy/cathode lead frame interface.

In our experiments, ESR values increased after three to 30 cycles, suggesting that normally the parts might remain stable after at least three runs during SMT simulation. One of the reasons for the ESR increase after multiple HT exposures might be degradation of the silver epoxy used to attach the tantalum slug to the lead frame. It is known that the contact resistance (Rc) between silver epoxy and non-noble materials, such as Cu, Al, Pb/Sn alloy, etc., increases with time of ageing, especially at high temperatures and humidity. The reason for Rc increase in the presence of moisture is probably due to oxidation of the metal caused by galvanic corrosion at the silver/non-noble metal contacts [18, 19]. Degradation of Rc for Sn/Pb plated metals in dry conditions at temperatures above 150 °C might be caused by the preferential diffusion of Sn from the plating layer into Ag flakes in the conductive adhesive. This diffusion results in formation of Ag/Sn intermetallic compounds in the Ag filler particles adjacent to the plating layer. At high temperatures, micro-voids are created with time in the intermetallics at the Sn/Pb plating layer due to the Kirkendall effect. This process might also result in interfacial de-bonding between the conductive adhesive and the Sn/Pb plating layer [20]. Considering also possible reflow of the tin-based solder during soldering of the capacitors, their use for plating of the lead frames should be avoided for high-reliability parts.

Based on results of capacitance measurements, moisture is mostly released from the part during the first one to three HT cycles. For this reason, the presence of moisture is probably not the major factor of the ESR degradation. To assess the effect of exposure to high temperatures, ESR values were measured on the 4.7 μF/50 V parts during experiments described above. Results of these measurements are shown in Figure 10 and indicate no significant variations in ESR after baking in the range of 200 °C to 240 °C.

It is possible that the observed degradation is related to fatigue processes caused by thermo-mechanical stresses during HT cycling. Thermo-mechanical stresses in tantalum capacitors might disrupt interfaces at the manganese and/or silver epoxy layers, resulting in increased resistance of the contacts. Additional analysis is required to better understand the reason of ESR degradation after HT cycling.



a) b)

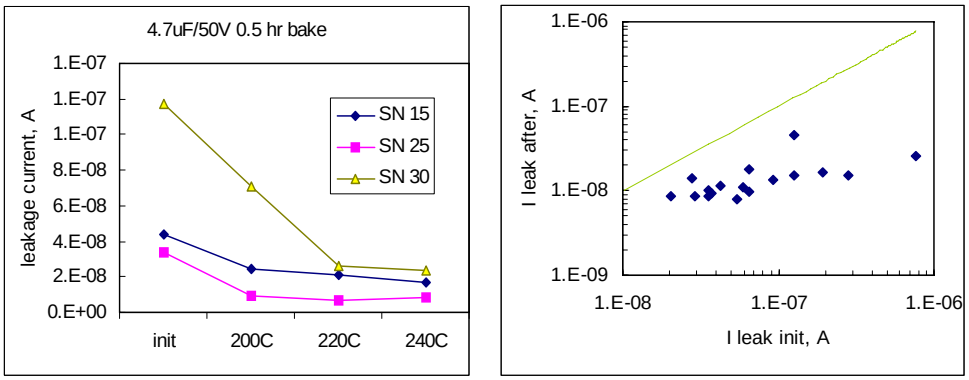
Figure 10. Effect of 30 min. bake at 200, 220, and 240 °C (a) and 96 hours bake at 200 °C on ESR of 4.7 μF/50 V capacitors.

II.5.4 Effect of HT cycling on leakage currents

The increase of leakage currents during HT cycling in our experiments could be due to either high-temperature degradation of the tantalum pentoxide dielectric or micro-cracking of the dielectric

caused by cycling-induced fatigue. It is known that high-temperature annealing of deposited tantalum pentoxide films results in two opposite and competing processes: annealing of the defects and creation of a crystal phase [21]. Crystallization of amorphous Ta_2O_5 films occurs after rapid thermal annealing at relatively high temperatures above 650 °C [22] and results in significant increase of the leakage currents. On the other hand, annealing of the films below the re-crystallization temperature in nitrogen [23] or oxygen [24] environments significantly reduces leakage currents in the oxide by removal of certain structural imperfections present in the layers initially. Oxygen might play an important role in the annealing process by reducing concentration of the oxygen vacancies and/or broken bonds. This decreases the concentration of electron traps in the film and leads to lower leakage current levels.

To evaluate the effect of exposure to high temperatures, leakage currents were measured for the 4.7 μF/50 V capacitors in experiments described above. Results of these measurements are shown in Figure 11 and indicate a significant decrease in DCL during annealing at temperatures above 200 °C. The decrease occurs mostly at 220 °C, and an additional 30 minutes bake at 240 °C does not cause significant changes in the current. Annealing at 200 °C for 96 hours decreases DCL by three to 30 times.



a) b)

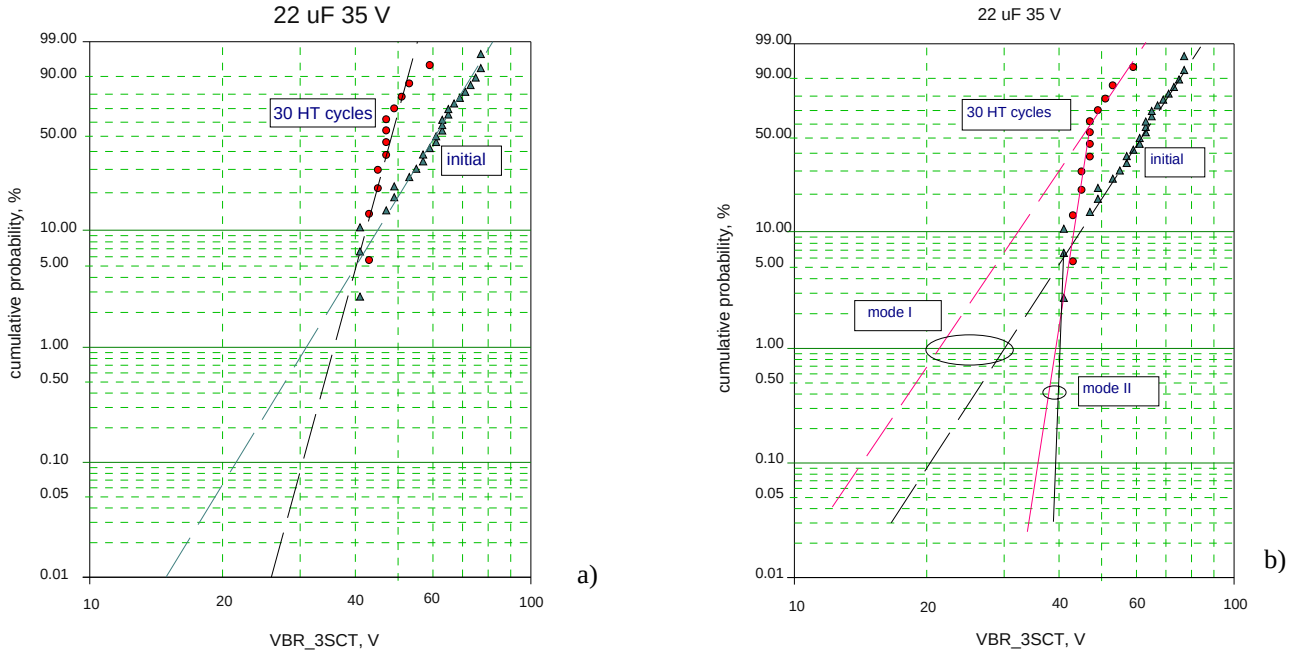
Figure 11. Effect of 30 min. bake at 200, 220, and 240 °C (a) and 96 hours bake at 200 °C on leakage currents in 4.7 μF/50 V capacitors.

These results indicate that an increase in DCL after HT cycling observed in two out of three lots in our experiments is most likely due to the cycling fatigue effect rather than to short-term, high-temperature baking of the capacitors. Note also that the lot having the most substantial degradation of ESR (22 μF/20 V capacitors) had stable leakage currents through the testing, which is related to different mechanisms of degradation for ESR and DCL. To assure the resistance of tantalum chip capacitors to soldering conditions, both parameters should be controlled during qualification testing of the parts.

II.5.5 Effect of HT cycling on surge current breakdown

A significant decrease in the breakdown voltages measured during step stress surge current testing was observed only for one lot, 22 μF/35 V. Interestingly, the same lot had the largest proportion of devices with increased leakage currents, implying a possible correlation between the DCL and breakdown voltages.

Figure 12a shows Weibull distributions of the breakdown voltages measured on the non-stressed devices and those stressed by 30 HT cycles 22 μF/35 V. An increase of the slope of the distribution (β) after HT cycling results formally in a substantial decrease of the probability of surge current failures at voltages below the rated one. This is most likely due to the bimodal character of the distributions, where a group of low-voltage devices has much greater values of β compared to the group of high-voltage devices. The same experimental data as in Figure 12a are approximated with bimodal distributions in Figure 12b. In this case, the probability of surge current failures at voltages below the rated voltage increases more than 10 times after HT cycling. More data are necessary to accurately evaluate distributions of the breakdown voltages and their variations for a low-voltage and high-voltage groups due to exposure to soldering temperatures.



a) b)

Figure 12. Effect of high-temperature cycling on results of step stress surge current testing of 22 μF/35 V tantalum capacitors. The results are approximated with unimodal Weibull distributions in (a) and with bimodal distributions in (b).

II.5.6 Analysis of MIL-PRF-55365 requirements

During screening per MIL-PRF-55365 (conformance inspection), all parts should pass reflow conditioning (one thermal shock to 230 °C minimum with time at T > 230 °C 5 s minimum) to help to remove components with weak internal bonds. However, ESR measurements are optional during the tests following reflow conditioning, so the parts with poor attachment cannot be screened out. Besides, no environmental preconditioning is required. As was shown above, parts exposed to different environments will have different moisture content and might create different level of stress during soldering simulation.

More comprehensive evaluation of the robustness of the parts to soldering stress is expected during a sample-based qualification testing of the lot. Qualification testing per MIL-PRF-55365 evaluates

the susceptibility of the parts to solder reflow stress during the resistance to soldering heat (RSH) test. For this test, 18 samples are soldered onto a board at +245 °C ±5 °C and then subjected to a moisture resistance test. Only DCL, capacitance, and dissipation factor are measured before and after the RHS testing, and one out of 18 parts can fail this combined RSH/moisture resistance test. This testing has several deficiencies and is not sufficient for assuring adequate reliability of the devices after soldering:

- Only moisture resistance testing is performed following RSH, whereas reliability qualification life test and surge current testing can be carried out without reflow soldering (mounting is optional for life test). Results of reliability testing on as-manufactured parts and parts that have experienced soldering stress might be different. Note, for example, that life testing of PEMs per JESD22-A113 is performed after solder reflow simulation.
- No environmental preconditioning is required before RSH testing. However, due to the pop-corning effect in tantalum capacitors, it is reasonable to expect that the parts with greater moisture content would be more susceptible to formation of soldering-induced defects. Compare this with a system of moisture sensitivity levels (MSL) developed for PEMs to address this issue and a special procedure including moisture soak, SMT simulation, and flux application used as preconditioning to simulate stresses during soldering.
- Only DCL, DF, and C are required to be measured and remain within the specified limits after resistance to soldering heat test. However, it was shown above that capacitance variations in most cases are not related to degradation processes in the part, and the requirement for capacitance to remain within 5% might be misleading. Also, the real values of leakage currents are typically ~2 orders of magnitude lower that the DCL limits, so even parts with significantly increased leakage currents might be considered as passing the test.
- Only one heat cycle during the resistance to soldering heat test is allowed. Compare this with the requirements for PEMs, where the parts are subjected to three consecutive runs simulating solder reflow process before reliability qualification testing. Our results show that normal quality tantalum capacitors are capable of withstanding three reflow cycles, and this requirement should be used to evaluate their robustness to soldering.
- The effect of soldering reflow on the susceptibility of tantalum capacitors to surge current failures is not assessed. However, our data as well as technical literature indicate that for some lots soldering stress might be significant enough to increase the probability of surge current failures.
- Leakage currents, ESR, and breakdown voltages measured during step stress surge current testing are the most important and sensitive parameters to the reflow soldering stress. Measurements of these parameters, their acceptable variations, and proper preconditioning of the parts before qualification testing should be specified in MIL-PRF-55365 to assure that the reliability of solid chip tantalum capacitors remains high after soldering.

II.6. Conclusion

1. Measurements of deformation of chip tantalum capacitors during soldering simulations showed the presence of anomalous spikes at temperatures from 180 °C to 200 °C, indicating the pop-corning effect. For high-reliability applications, baking of the devices before soldering is recommended to reduce the risk of damaging the parts.

2. Three lots of chip tantalum capacitors were subjected to multiple temperature cycling between room temperature and 240 °C to simulate thermal stresses in the parts during reflow soldering. The results indicate that exposure to high temperatures might cause degradation of leakage currents and ESR and increase the probability of surge current failures. Different lots have different susceptibility to soldering stress.
3. After the first one to three high-temperature exposures, the capacitance in all parts decreases by 0.9% to 15%. The effect is most likely due to moisture desorption and is not a reliability concern.
4. All tested parts withstood three HT cycles without substantial variations of ESR, but additional cycling increases the resistance indicating onset of wear-out degradation in the parts. The number of cycles to this degradation is lot-dependant and varied from 10 to 100 cycles.
5. A significant increase in leakage current was observed in two out of three lots, and one of these lots had also decreased surge current breakdown voltages. Both results are due likely to thermo-mechanical stresses rather than to the high-temperature exposure of the parts.
6. Recommendations to improve screening and qualification testing per MIL-PRF-55365 to assure better resistance of the parts to soldering stress are discussed.

Part III. Effect of Cryogenic Temperatures on Solid Tantalum Capacitors

III.1. Introduction

Space exploration programs often require that sensors and instruments with related service electronics are exposed to outer space, thus subjecting them to extreme environmental conditions. In programs such as Lunar and Martian expeditions and deep-space exploration, these conditions include cryogenic temperatures.

Tantalum and ceramic capacitors are widely used at the power supply pins of microcircuits to short high-frequency signals and provide the necessary charge during burst increases of the load currents. Typically, most capacitors decrease their values as the temperature decreases [25-27]. However, there is no sufficient information in relevant literature regarding frequency dependencies of capacitance (C) and effective series resistance (ESR) at cryogenic temperatures, and the mechanism of parametric degradation of tantalum capacitors at these conditions has not been investigated properly yet.

Failure of a tantalum capacitor used in power supply lines might cause a short circuit and result in a catastrophic failure in the system. Typically, a current surge test is performed to assure the robustness of the parts to transient currents, but no such data have been available yet for cryogenic conditions.

During the ground-phase integration and testing period of a space system, the parts are subjected to multiple exposures to cryogenic conditions. This requires investigation of the effect of cryo-cycling on the behavior of parts intended for applications at extremely low temperatures.

In this work, performance of different types of solid tantalum capacitors was evaluated at room temperature and low temperatures, down to 15 K. The effect of temperature on frequency dependencies of capacitance, effective series resistance, leakage currents, DC leakage current (DCL), and breakdown voltages (VBR) have been investigated and analyzed. To assess thermo-mechanical robustness of the parts, several groups of capacitors were subjected to multiple (up to 500) temperature cycles between room temperature and 77 K. Mechanisms of degradation of AC and DC characteristics at cryogenic conditions are discussed.

III.2. Experiment

Frequency characteristics of capacitors were measured using an HP4192A LF impedance analyzer. Leakage currents were measured with time at different voltages and temperatures using a precision semiconductor analyzer HP4156A. Step stress surge current testing (3SCT) was carried out using a PC-based system with the effective resistance of the circuit ~0.3 Ohm.

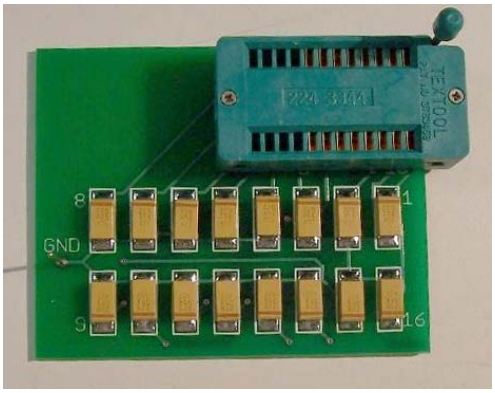
Experiments were carried out on different types of commercial solid tantalum leaded (TAP) and chip (T495/T491) capacitors manufactured by Kemet and AVX (see Table 1). Three samples minimum of each type were used for testing.

Table 1. Capacitors used for testing.

PN	C, μF	V, V	ESR Limit, Ohm	DCL Limit, μA
TAP106K050SCS	10	50	1.6	4
TAP106K025SCS	10	25	2.5	2
T495X156M050AS	15	50	0.3	7.5
CWR09JC226KC	22	20	0.9	4
T491C106K016AS	10	16	1.8	1.6
T491D226M035AS	22	35	0.7	7.7

Low-temperature measurements were carried out either at a liquid nitrogen temperature (liquid nitrogen [LN] conditions, T = 77 K) or in a Cryodyne chamber allowing testing down to 15 K.

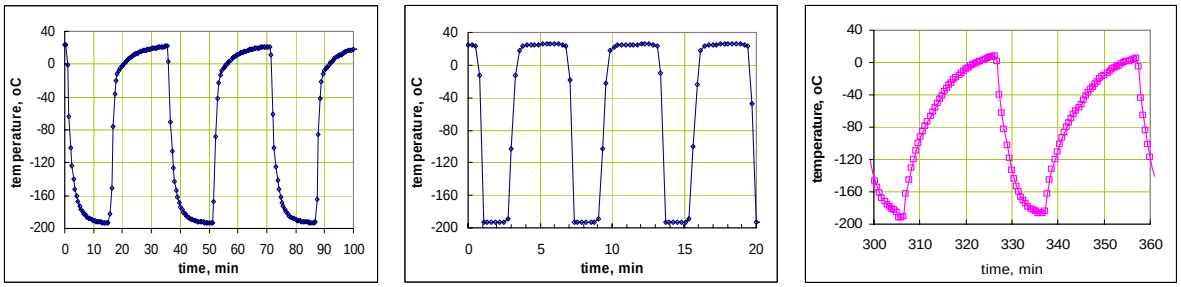
For cryo-cycling, different groups of capacitors, with 12 to 15 parts in each group, were placed in hermetic cells and immersed periodically into LN dewar using a PC-based system, which controlled a mechanical armature and allowed monitoring of the temperature inside the cells. A set-up used for temperature cycling is shown in Figure 1a. To assess the effect of lot-to-lot variations, two lots of 15 μF/50 V capacitors with different date codes were used. Experiments were carried out on loose parts and capacitors soldered onto a board as shown in Figure 1b. Characteristics of the parts were measured periodically during this testing, which continued until 500 cycles were completed for loose parts and 100 cycles were completed for the parts soldered on FR4 boards.



a) b)

Figure 1. A set-up used for cryo-cycling (a) and capacitors soldered on an FR4 board (b).

Cryo-cycling of loose capacitors was carried out also in a cell made out of a metal grid allowing direct immersion of the parts into liquid nitrogen. Figure 2 displays temperature profiles for various cycling conditions used. The dwell time at the temperature extremes was ~3 min., and the temperature rate was ~40 °C/min. for normal cycling and ~650 °C/min. for direct immersion. The rate of temperature variations during cycling of capacitors soldered onto the boards was ~15 °C/min.



a) b) c)

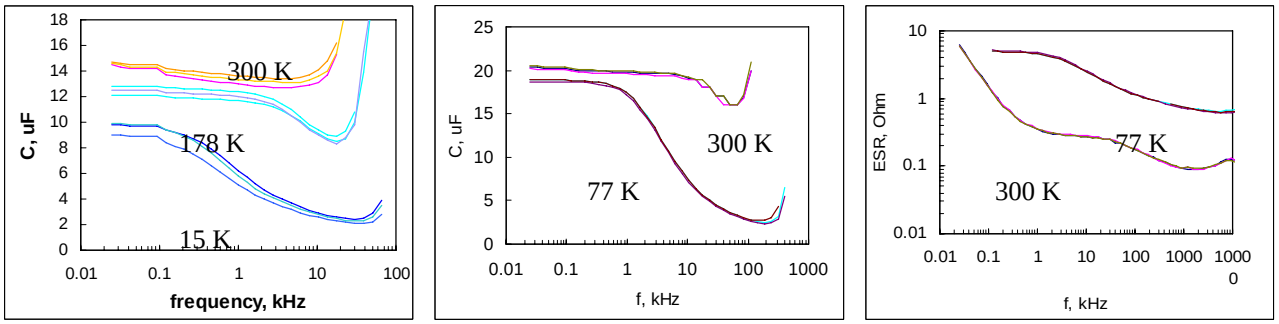
Figure 2. Temperature profiles for normal (a) and fast (b) cryo-cycling of loose parts between RT and LN and for the parts soldered onto FR4 boards (c).

III.3. Performance at cryogenic conditions

III.3.1 Frequency dependencies of C and ESR

Figure 3 shows typical frequency dependencies of capacitance for two part types at room and cryogenic temperatures. At low frequencies (<0.1 kHz), a decrease of C is relatively small (10% to 30%), whereas at high frequencies capacitance decreases five to seven times. This behavior is due to the so-called roll-off effect, in which a slope of C-f characteristics of tantalum capacitors increases when frequency exceeds the roll-off frequency, f_r. The effect is qualitatively explained by an R-C-ladder behavior of the capacitor in the frequency domain [28].

A characteristic feature of the C-f dependencies measured at low temperatures is a significant decrease of f_r with temperature. At room temperature f_r is ~10 to 30 kHz and decreases to ~1 kHz at LN conditions and to ~0.1 kHz at 15 K.



a) b) c)

Figure 3. Frequency dependence of capacitance (a, b) and ESR (c) at different temperatures for three 15 µF/50 V (a) and three 22 µF/35 V (c) capacitors.

Average values of capacitance measured at 1 kHz and ESR measured at 100 kHz for different part types are summarized in Table 2. At 1 kHz a decrease of C at 77 K is relatively small and varies from 7% to 26%, whereas ESR increases more dramatically, from four to 18 times. This increase of ESR is most likely due to temperature variations of the resistivity of manganese cathode layers.

Table 2. Average values of capacitance and ESR at room and liquid nitrogen temperatures.

Type	C, µF		ESR, Ohm	
	RT	LN	RT	LN
10 µF 50 V	10.3	8.8	0.42	2.4
10 µF 25 V	9.6	8.9	0.36	2.2
15 µF 50 V	15.1	11.1	0.19	0.73
10 µF 16 V	10.1	8.6	0.45	7.9
1.5 µF 16 V	1.5	1.35	4.8	89
22 µF 35 V	19.8	17.3	0.17	1.1

To explain the observed frequency variations at low temperatures, a tantalum capacitor was represented with a distributed one-dimensional R-G-C circuit shown in Figure 4. In this figure ρ is the specific (per unit length) surface resistivity of the manganese layer, and C_o and g are the specific capacitance and conductance of the tantalum pentoxide layer.

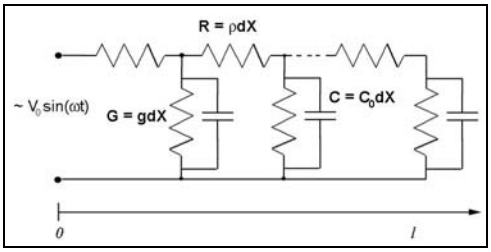


Figure 4. Equivalent schematic of a tantalum capacitor.

Distribution of the potential, *V(x,t)*, along this R-G-C ladder is given by the following equation:

$$\frac{\partial u}{\partial \theta} = \frac{\partial^2 u}{\partial \xi^2} - \alpha \times u^2, \tag{1}$$

where $u = V/V_o$, $\xi = x/l$, $\theta = t/(C_o \times \rho \times l^2)$, $\alpha^2 = g \times \rho \times l^2$.

Assuming that an AC signal applied to the capacitor has a circular frequency ω, the border conditions can be written as follows:

$$\left.\begin{aligned} u(0,\theta) &= \sin(\omega' \times \theta) \\ \frac{\partial u}{\partial \xi}(1,\theta) &= 0 \\ u(\xi,0) &= 0 \end{aligned}\right\}, \tag{2}$$

where $\omega' = \omega \times \rho \times C_o \times l^2$.

Input currents at the beginning of the ladder can be expressed through the voltage gradient:

$$I_0 = V_0 \times \left.\frac{\partial u}{\partial \xi}\right|_{\xi = 0} \times \frac{1}{\rho \times l}$$

This allows calculation of the equivalent capacitance of the ladder:

$$C_{eq} = \frac{I_0}{\omega \times V_0}$$

Using a solution for the problem Eq. (1, 2) at stationary-state conditions [29] and neglecting g, the expression for C_{eq} can be written as:

$$C_{eq} = 2 \times l \times \sqrt{A^2 + B^2} \quad , \qquad (3)$$

where

$$A = \sum_1^\infty \frac{C_0 \times \omega'}{\lambda_n^4 + \omega'^2}.,...B = \sum_1^\infty \frac{C_0 \times \lambda_n^2}{\lambda_n^4 + \omega'^2}.,...\lambda_n = \frac{(2n-1) \times \pi}{2}., \quad \text{n = 1, 2, 3, …}$$

Effective length and surface area of electrodes of a typical chip tantalum capacitor are l ~3 mm and S ~100 cm^2, and the thickness of Ta_2O_5 dielectric, h, ~3×10^{-4} cm [7]. At room temperature, the values of the specific volume resistivity, ρ_v, of MnO_2 vary from 1 Ohm×cm to 10 Ohm×cm [28, 30, 31]. At these conditions the equivalent specific resistivity, which is $\rho = \rho_v \times l/(S \times h)$, will be ~10 to 100 Ohm/cm. Based on the ESR measurements, the resistance of MnO_2 is increasing at liquid nitrogen conditions in four to 18 times, resulting in variation of ρ from 40 to 1,800 Ohm/cm. These relatively weak temperature variations are in agreement with an assumption that manganese dioxide is an N-type semiconductor with a shallow donor level having energy of ~40 meV [32].

Using these data, frequency dependencies of capacitance were calculated for a 10 μF capacitor at the effective surface resistances of MnO_2 layer ranging from 10 to 1,800 Ohm/cm. Results of these calculations are displayed in Figure 5. A comparison with Figure 3 shows reasonably good agreement with the experimental data. Assuming that the value of ρ of MnO_2 at RT is ~10 Ohms/cm, the calculated roll-off frequency, f_r, is ~10 kHz. An increase of ρ_v to 300 Ohms/cm at LN conditions decreases f_r to ~1 kHz, which corresponds to the experimental data.

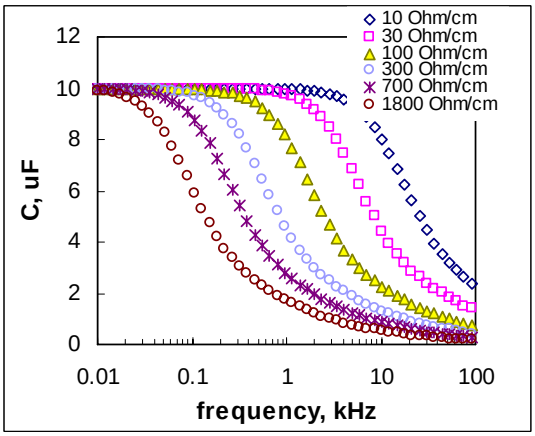
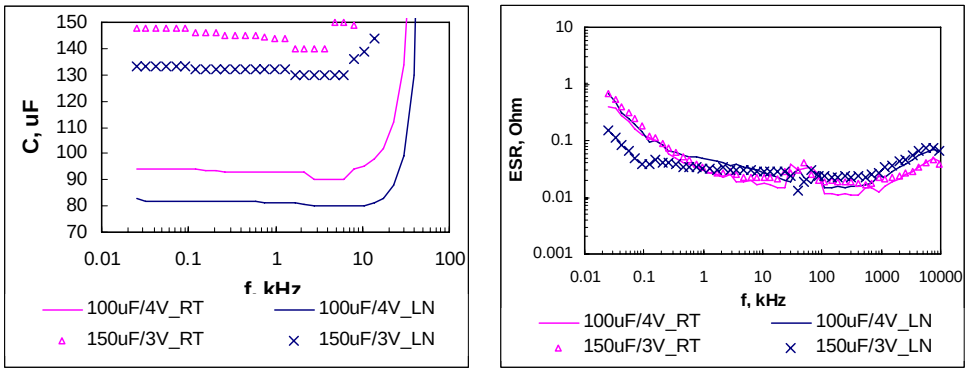


Figure 5. Frequency dependencies of a 10 μF tantalum capacitor at different surface resistivity of manganese cathodes calculated according to Eq. (3).

The results indicate that at low temperatures and relatively high frequencies, $f > f_r$, a significant decrease in C is due to increase of the resistance of manganese cathode. Contrary to that, at low frequencies, $f < f_r$, a relatively small decrease of capacitance is due to temperature variations of the dielectric constant of tantalum pentoxide dielectric. It is important to note that tantalum capacitors with polymer cathodes, which remain high conductivity of the polymer at low temperatures, do not degrade significantly at cryogenic conditions (see Figure 6). This makes polymer tantalum capacitors promising for low-temperature applications. However, additional analysis of the reliability of these parts is necessary before their application in high-reliability systems.



a) b)

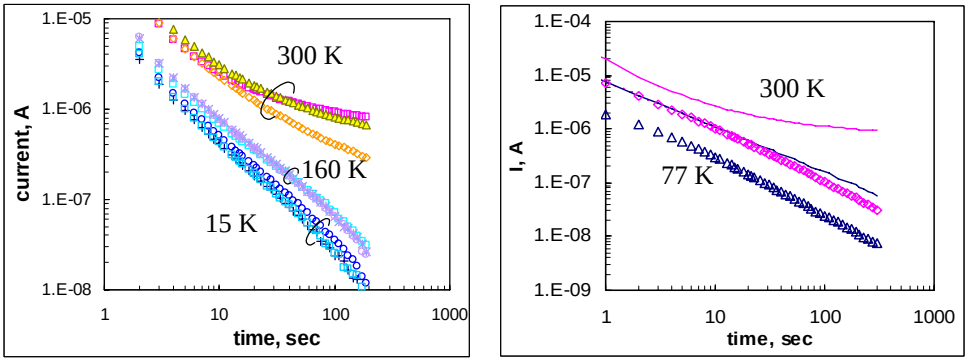
Figure 6. Frequency dependencies of capacitance (a) and ESR (b) of 150 µF/3 V (marks) and 100 µF/4 V (lines) tantalum polymer capacitors at room (pink) and LN (blue) temperatures.

III.3.2 Leakage currents

A forward current (normal polarity) in a tantalum capacitor is a sum of time-dependent absorption currents and time-independent leakage currents [7]. Absorption currents are due to accumulation of trapped charges in Ta_2O_5 dielectric and decrease with time after applying voltage following a power law, $I \sim t^{-m}$, with the exponent m varying at room temperature from 0.8 to 1.1.

Figure 7 shows typical time dependence of forward currents (I-t characteristics) for a 15 µF 50 V capacitor at different temperatures. It is seen that at the rated voltage, after 5 min. leakage currents can be observed at room temperature only, and at low temperatures they decrease below the nanoampere range. This agrees with the reported activation energies of leakage currents, which vary from 0.3 to 0.7 eV [7, 33]. Even at Ea = 0.3 eV, the leakage currents decrease more than 10^{15} times as the temperature decreases from room to LN conditions.

Absorption currents follow a power law, $I \sim t^{-m}$, down to 15 K, and they do not change with temperature significantly, decreasing about three times only between RT and LN conditions and about five times down to 15 K. The exponent m does not depend on temperature significantly either, remaining in the range from 0.9 to 1.1. Depolarization currents also decrease with time according to a power law with the exponent close to the one for polarization currents.



a) b)

Figure 7. Variations of currents with time after voltage application in 15 µF/50 V capacitors at different temperatures (a) and comparison of polarization (lines) and depolarization (marks) currents at RT and LN conditions (b).

Voltage dependence of leakage currents in Ta_2O_5 is explained usually either by a bulk-limited Pool-Frenkel (PF) mechanism of conductivity or by a surface-barrier-limited Schottky mechanism [24, 34]. The PF mechanism can be described by the following equation:

$$J = C_t E \exp\left(-\frac{q\Phi}{kT}\right)\exp\left(-\frac{\beta_{PF} E^{1/2}}{kT}\right), \quad (4)$$

where J is the current density, C_t is a trap density related constant, E is the electric field, q is the charge of electron, Φ is the barrier height, k is the Boltzmann constant, and T is the absolute temperature, and

$\beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon}\right)^{1/2}$ is the PF constant, ε_0 is the permittivity of the free space, and ε is the high-frequency dielectric constant, which for Ta_2O_5 is $\varepsilon_{HF} \approx 5$.

A corresponding equation for the Schottky mechanism can be written as

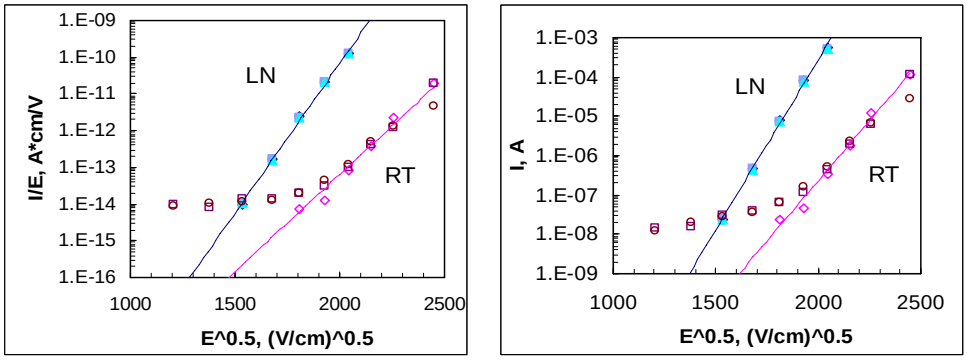
$$J = C_{RD} T^2 \exp\left(-\frac{q\Phi}{kT}\right)\exp\left(\frac{\beta_S E^{1/2}}{kT}\right), \quad (5)$$

where $\beta_S = \left(\frac{q^3}{4\pi\varepsilon_0\varepsilon}\right)^{1/2}$ and C_{RD} is the Richardson-Dushman constant.

To discriminate between these two mechanisms, the dielectric constant ε was calculated based on experimentally determined values of slopes β_{PF} and β_S. The values of leakage currents (in our experiments, the currents were measured in 5 min. after voltage application) in different groups of capacitors were measured at room and LN conditions at voltages varying from the rated voltage to the breakdown voltage in 5 V increments. The data were plotted in PF coordinates, $ln(I/E)$ vs $E^{0.5}$, and in Schottky coordinates, $ln(I)$ vs. $E^{0.5}$. The electric field E was calculated as $E = V/h$, where the thickness h was assumed to be 110 nm, 240 nm, and 350 nm for 16 V, 35 V, and 50 V capacitors, respectively. Figure 8 shows results of these experiments for 10 µF/16 V capacitors. Similar charts were obtained for other part types.

At room temperature, deviations from the straight line are due most likely to a significant contribution of the absorption currents, which do not follow PF or Schottky mechanisms. In all cases, at relatively large $E > 3\times10^6$ V/cm I-V, characteristics could be could be equally well approximated with both equations having R-squared values for the regression trend lines exceeding 0.995.

In an attempt to discriminate between these models, the values of high-frequency dielectric constants were calculated for the PF, ε_{PF}, and Schottky, ε_S, models (see Table 3). At room temperature, ε_S varies from 0.5 to 4, whereas ε_{PF} varies from 2.4 to 11.6. These data suggest that at room temperature the PF conductivity is more probable compared to the Schottky-controlled mechanism. At LN conditions the situation is different, and the values of ε_{PF} (from 32.6 to 93.7) are much higher than the expected value of the high-frequency dielectric constant. The values of ε_S at cryogenic condition vary in a relatively narrow range, from 8.2 to 8.7, which is reasonably close to ε_{HF}.



a) b)

Figure 8. I-V characteristics of 10 µF 16 V Ta capacitors at RT and LN conditions in Pool-Frenkel (a) and Schottky (b) coordinates.

Table 3. Calculated values of the dielectric constant.

Part	PF RT	Sch. RT	PF LN	Sch. LN
1.5 µF 16 V	11.6	2.33	39	8.24
10 µF 16 V	5.8	1.08	36.9	8.25
22 µF 35 V	10.6	4.03	32.6	7.26
15 µF 50 V	2.4	0.53	93.7	8.67

It should be noted that in the presence of multi-level traps and partial compensation of the donor centers, the number of electrons participating in conduction decreases, and the conduction can be described by a modified PF equation [24, 34, 35]:

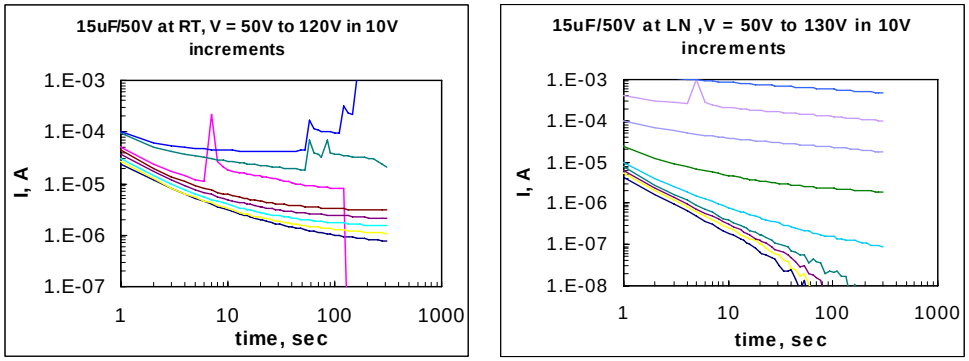
$$J = C_t E \exp\left(-\frac{q\Phi}{kT}\right)\exp\left(-\frac{\beta_{PF} E^{1/2}}{rkT}\right), \quad (6)$$

where r is a coefficient in the modified PF effect with compensation.

Use of the modified Poole-Frenkel model can decrease the estimated values of ε up to four times; however, even in this case, they remain larger than those obtained by the Schottky model. This indicates that at cryogenic temperatures, the mechanism of conduction in tantalum capacitors most likely changes from the bulk-controlled PF trap-assisted conductivity to a surface-barrier-controlled Schottky mechanism.

III.3.3 Breakdown voltages

As the voltage applied to a tantalum capacitor increases, a so-called scintillation or local momentary breakdown in the dielectric occurs, causing current spikes in the I-t curves as shown in Figure 9. These current pulses are believed to be due to a local breakdown of the Ta_2O_5 dielectric, which is terminated by the self-healing mechanism [36]. According to this mechanism, temperature of the manganese cathode in areas of breakdown increases, resulting in conversion of conductive MnO_2 into a high-resistive Mn_2O_3 (~10^4 Ohm×cm) and thus reducing breakdown currents. Comparison of typical results of I-t measurements at RT and LN conditions shown in Figure 9 suggests that at 77 K, scintillations are observed at much higher voltages than at room temperature.

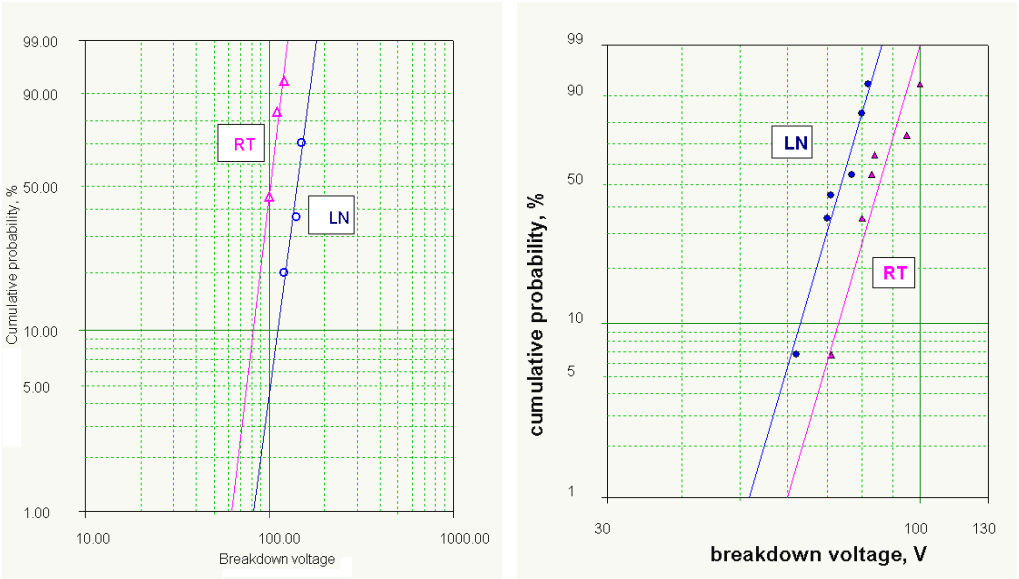


a) b)

Figure 9. Typical I-t characteristics of 15 μF/50 V capacitors during step voltage testing at room (a) and liquid nitrogen (b) conditions.

To assess the effect of temperature on breakdown voltages quantitatively, two groups of 15 μF 50 V capacitors with nine samples in each group were tested for 5 min. at voltages increasing with 10 V increments. The scintillation breakdown voltage, V_S, was determined as the voltage at which the first current spike was observed.

Results of these experiments are presented in Weibull coordinates in Figure 10a. At room-temperature conditions, the characteristic scintillation voltage was ~40% lower than at LN conditions (148.7 V and 105.3 V, respectively). The slope of the distributions was similar and varied in the range from $\beta = 7.8$ to 8.8, suggesting that at both temperatures the mechanism of breakdown was similar. These results are consistent with the overall trend of increasing breakdown voltages of dielectrics at cryogenic conditions [37].



a) b)

Figure 10. Weibull distributions of breakdown voltages for 15 μF/50 V capacitors: a) scintillation breakdown voltages, and b) step surge current test breakdown voltages.

Distributions of the breakdown voltages measured during step stress surge current testing (3SCT) at room-temperature and liquid nitrogen conditions are shown in Figure 10b. Similar to scintillation measurements, both distributions were parallel with the slope β varying from 11 to 12,

but the characteristic breakdown voltage, VBR_3SCT, at LN (75.9 V) was ~40% lower than at room temperature (88.1 V).

One of the reasons for this might be related to increased resistance of the manganese layer at low temperatures. Figure 11 shows variations of amplitudes of the currents with voltage measured during the step stress surge current testing. The results can be approximated with straight lines, and the slopes of these lines indicate the effective resistances, R_{ef}, of the circuit used for the testing. At room temperature R_{ef} = 0.32 Ohm and at 77 K it increases to 0.76 Ohm, which is close to the variations of ESR for 15 μF/50 V capacitors shown in Table 2. The increase in ESR substantially increases the proportion of energy dissipated during surge current testing in the capacitor [8], which might be one of the reasons for decreasing of the breakdown voltage.

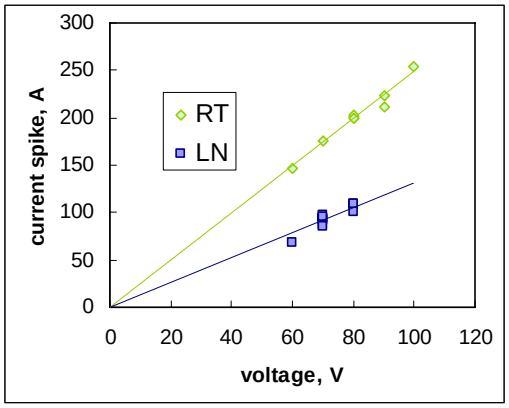
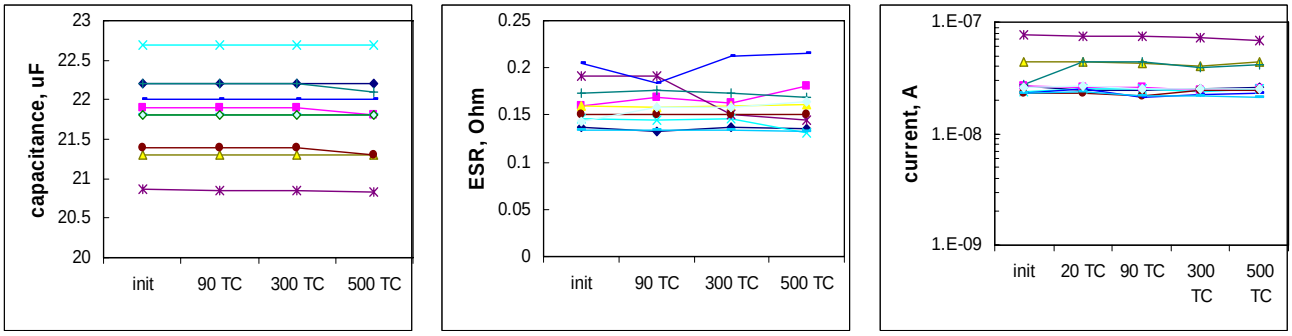


Figure 11. Variations of current spike amplitude with voltage during step stress surge current testing (3SCT) at room temperature and 77 K.

The difference in the effect of temperature on breakdown voltages measured during scintillation testing and surge current testing is due to different mechanisms of breakdown in high- and low-impedance circuits. Although the mechanism of failures under surge current testing and factors affecting the probability of these failures are not well understood yet, it is known that there is no correlation between the results of surge current testing and leakage currents in tantalum capacitors [38]. Our data indicate also that VBR_3SCT is not related directly to the breakdown voltage of the tantalum pentoxide dielectric.

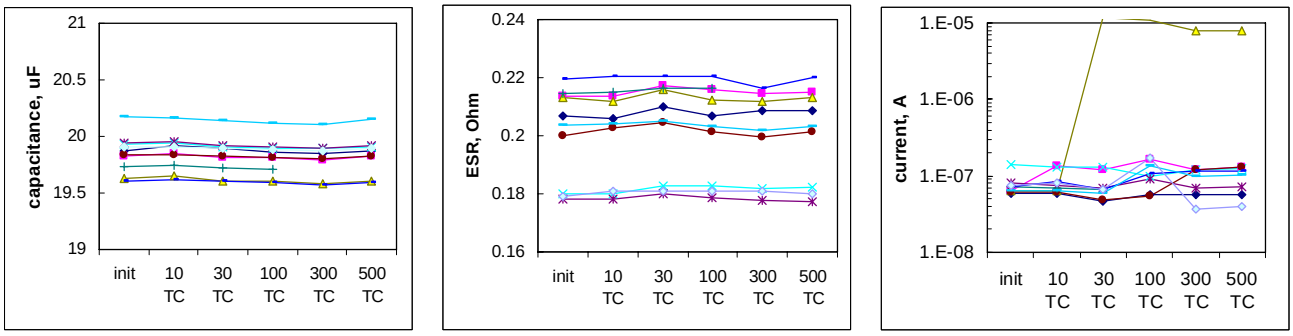
III.4. Effect of cryo-cycling

Results of cryo-cycling of six lots of solid tantalum capacitors are shown in Figures 12 to 17. In all cases, there were no substantial variations of capacitance and ESR up to 500 cycles. However, failures due to leakage currents exceeding the specified limits were observed in two lots: in 22 μF/35 V, where one out of 10 parts failed after 30 cycles, and in 15 μF/50 V gr. I, where 40% of the parts failed between 300 to 500 cycles. Note that in the 15 μF/50 V gr. I lot, 80% of the parts increased leakage currents significantly by the end of testing, whereas in all other lots the currents remained stable. The second lot of 15 μF/50 V capacitors (gr. II parts) behaved differently compared to the first group and had no degradation of leakage current and/or failures.



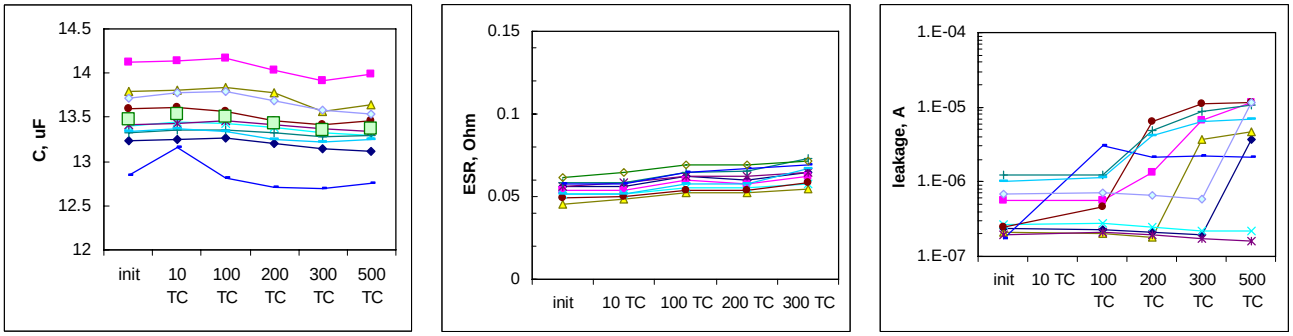
a) b) c)

Figure 12. Effect of cryo-cycling on capacitance (a), ESR (b), and leakage currents (c) of 22 μF/20 V chip tantalum capacitors.



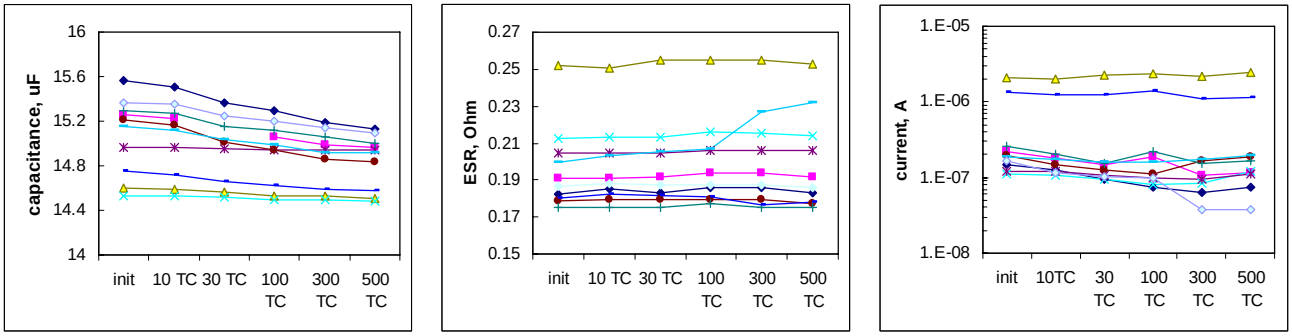
a) b) c)

Figure 13. Effect of cryo-cycling on capacitance (a), ESR (b), and leakage currents (c) of 22 μF/35 V chip tantalum capacitors.



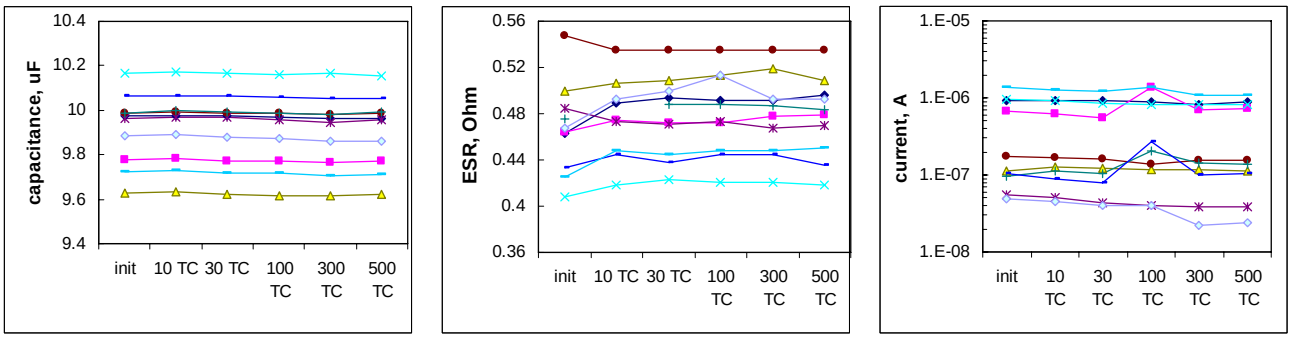
a) b) c)

Figure 14. Effect of cryo-cycling on capacitance (a), ESR (b), and leakage currents (c) of 15 μF/50 V gr. I chip tantalum capacitors.



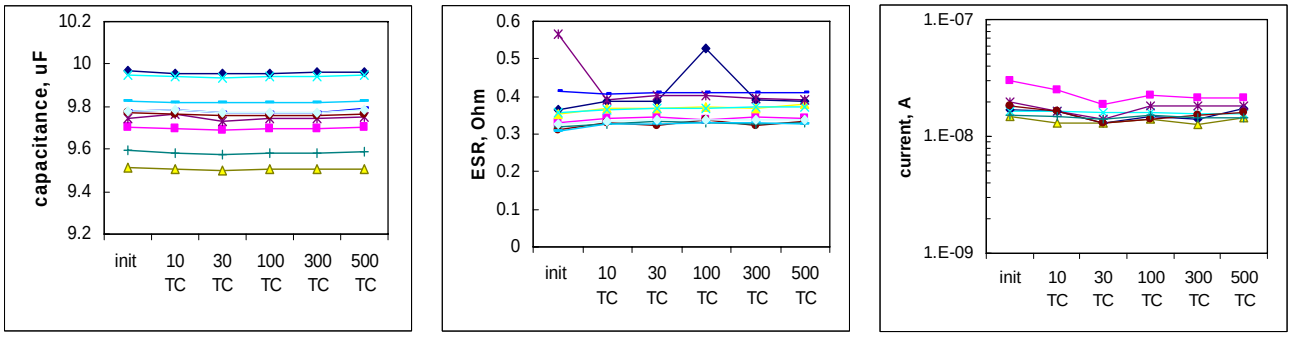
a) b) c)

Figure 15. Effect of cryo-cycling on capacitance (a), ESR (b), and leakage currents (c) of 15 μF/50 V gr. II chip tantalum capacitors.



a) b) c)

Figure 16. Effect of cryo-cycling on capacitance (a), ESR (b), and leakage currents (c) of 10 μF/50 V leaded tantalum capacitors.



a) b) c)

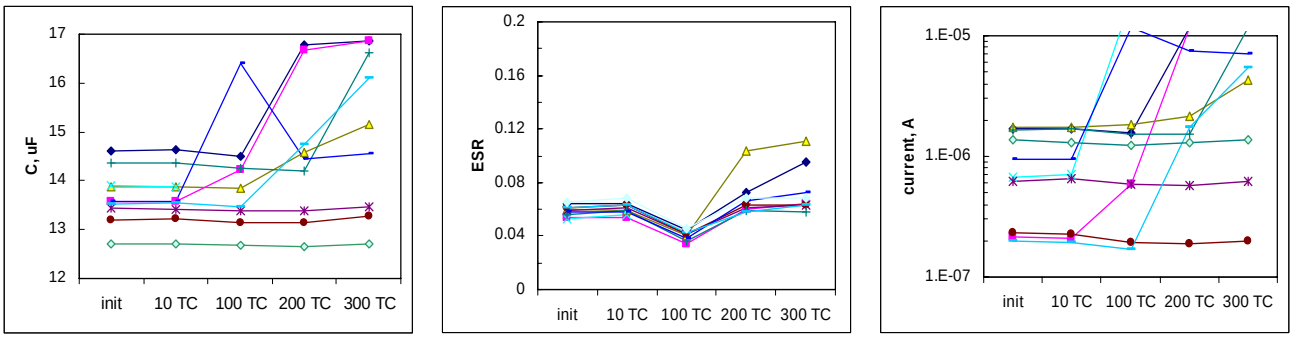
Figure 17. Effect of cryo-cycling on capacitance (a), ESR (b), and leakage currents (c) of 10 μF/25 V leaded tantalum capacitors.

These results indicate that solid tantalum capacitors are capable of withstanding multiple exposures to cryogenic conditions. However, failures due to increased leakage currents are possible in some lots, and the robustness of the lot to cryo-cycling should be evaluated before using the parts in cryogenic applications.

It is interesting to note that the span of temperatures during cryo-cycling, ~220 °C, is the same as the span used for high-temperature cycling described in the previous section of this report. However, the results of cycling were different. HT cycling caused degradation of ESR in all tested

lots, and two out of three lots had failures and degradation of DCL. Apparently, exposure to high temperatures might be more detrimental for chip tantalum capacitors compared to low-temperature exposures.

Figure 18 shows results of "fast" cryo-cycling, during which 10 chip tantalum capacitors of 15 μF/50 V gr. I were periodically immersed in liquid nitrogen. Comparison with Figure 14 shows much more severe degradation of capacitance and leakage currents. The results are obviously due to the increased temperature gradients in the part, which substantially enhances mechanical stresses in the molding compound and tantalum slug.



a) b) c)

Figure 18. Effect of fast cryo-cycling on capacitance (a), ESR (b), and leakage currents (c) of 15 μF/50 V gr. I chip tantalum capacitors.

Considering that similar equations describe processes of thermal conductivity and moisture diffusion in plastic packages, it is possible to use a simple expression for the characteristic time of moisture diffusion [39] to assess the characteristic time of thermal stabilization, ϑ. For a rough assessment, it can be assumed that the package of a tantalum capacitor is a cylinder of a radius R. In this case:

$$\theta = 0.45\frac{R^2}{\alpha} \quad , \qquad (7)$$

where α is the thermal diffusivity of molding compound (MC), α = k/(ρ×c). Here *k* is the thermal conductivity, *c* is the specific heat capacity, and ρ is the specific density of the MC. For a typical MC *k* varies from 1 to 2 W/m×K, *c* varies from 0.8 to 0.9 J/g×K, and ρ is normally ~1.8×10^3 kg/m^3 [40]. Assuming the size of the part (~4 mm and R = 2×10^{-3} m), calculations yield ϑ = 0.65 to 1.5 s. The temperature rate during cryo-cycling was ~40 °C/min. (0.67 °C/s). This means that temperature variations across the part did not exceed ~1 °C. However, during fast cycling, the rate was ~650 °C/min. (~11 °C/s) resulting in the temperature variation of ~15 °C, which might be substantial enough to cause micro-cracking and/or fractures in the part. Examinations of the parts after fast cycling reveled cracks in the molding compound in some samples, whereas no fractures in any of the parts occurred at a slower rate of the cycling.

Increased stresses during fast cycling resulted in more extensive damage to the dielectric and higher leakage currents. This can explain also variations in the capacitance of the parts. A decreased resistance of the tantalum pentoxide dielectric, R, results in an increase of the effective capacitance according to the equation:

$$C_{eff} = C \times \left(1 + \frac{1}{R^2\omega^2C^2}\right) \quad , \qquad (8)$$

where C is the capacitance of the part and ω is the circular frequency.

Interestingly, during the first 10 fast cryo-cycles all parts remained stable, indicating that chip tantalum capacitors are capable of surviving a few cycles even at these extremely stressful conditions.

To assess the effect of cryo-cycling on susceptibility of the parts to surge current failures, all parts in the 15 μF/50 V gr. I lot were surge current tested after 500 cycles at the rated voltage. Two parts, which had originally failed due to high leakage currents of more than 1E-5 A, failed SCT catastrophically. However, all other parts, even those that had substantially increased leakage currents, passed the test and did not change their characteristics significantly after surge current testing.

To get a quantitative characteristic of the robustness of the parts to surge currents and assess the effect of cryo-cycling more precisely, two other groups of the parts, 15 μF/50 V gr. II and 22 μF/35 V, were subjected to the step stress surge current testing (3SCT). Statistical characteristics of the breakdown voltages, which were measured after 500 cryo-cycles, as well as results that were obtained on virgin parts, are shown in Table 4. The Student's t-test parameters and the degree of freedom (df) were calculated and results are also presented in Table 4.

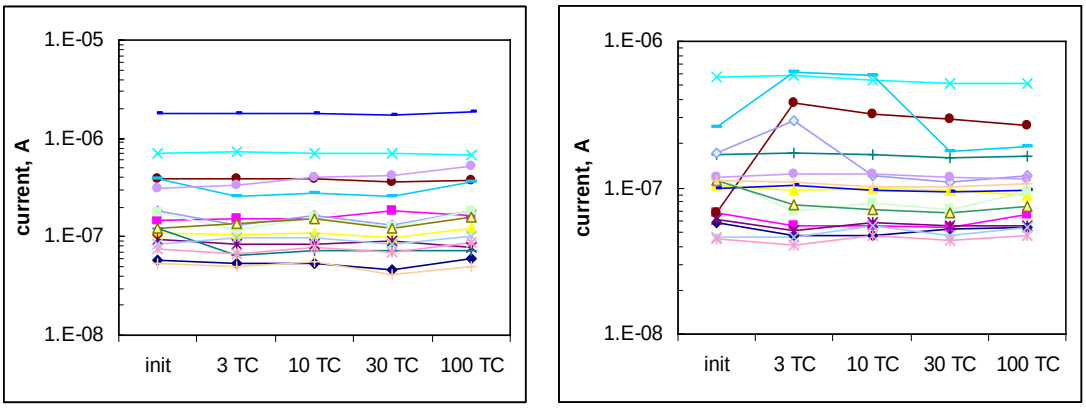
Table 4. Effect of high-temperature cycling on VBR_3SCT.

Part	**Non-Stressed Parts**			**After Cryo-Cycling**			**Analysis**		
	Qty.	**Avr.**	**Std.**	**Qty.**	**Avr.**	**Std.**	**t**	**df**	**$t_{crit.}$**
22 μF/35 V	25	60	10.9	9	57.4	9.2	0.69	16.7	2.12
15 μF/50 V gr. II	3	76.7	4.1	10	69.3	17.3	1.24	10.9	2.23

Analysis of the data indicates that at the confidence level of 95% there is no significant difference in the breakdown voltages measured before and after cryo-cycling. It is interesting to note that even the part, which failed DCL after 30 cycles in the 22 μF/35 V group, had a relatively high breakdown voltage of 61 V. This confirms that there is no direct correlation between the leakage currents and the susceptibility of the part to surge current failures.

Temperature cycling of the parts soldered on the boards was expected to cause more failures compared to loose parts due to development of additional mechanical stresses caused by CTE mismatch between the part and the board materials. However, experiments (see Figure 19) did not reveal failures in soldered parts up to 100 cycles. Similar to results for loose parts, one capacitor in the 22 μF/35 V group significantly (more that five times) increased DCL after three cycles, but the current remained within the specified limits and did not degrade further during the cycling.

It is possible that the robustness of chip tantalum capacitors toward stresses at cryogenic temperatures is high enough to accommodate additional stresses caused by soldering onto the board. However, the result might be due also to a lesser rate of temperature variation during cycling of the boards compared to loose parts. Additional experiments are necessary to evaluate the effect of soldering on the results of cryo-cycling.



a) b)

Figure 19. Variation of leakage currents of 15 μF 50 V gr. II (a) and 22 μF 35 V (b) capacitors soldered on the boards during cryo-cycling.

III.5. Conclusion

1. At relatively low frequencies, $f < f_r$, solid tantalum capacitors with manganese cathode decrease their value at LN compared to RT conditions on less that ~30%. However, at $f > f_r$ the decrease of C might be as large as five to seven times. The ESR values measured at 100 kHz increase 4 to 18 times at 77 K compared to RT conditions.
2. Simulation of a tantalum capacitor with a one-dimensional RC ladder has shown that variations of frequency dependence and decrease of capacitance at low temperatures is mostly due to an increase of resistance of the manganese cathode layer, resulting in substantial decrease of the roll-off frequency.
3. Frequency dependencies of capacitance and ESR in tantalum capacitors with polymer cathodes do not degrade significantly at low temperatures, which makes them promising for cryogenic applications.
4. Absorption currents, which prevail in tantalum capacitors during the first several minutes after applying voltage, do not change significantly at low temperatures down to 15 K and follow a power law, $I \sim t^{-m}$, with the exponent m varying from 0.8 to 1.1.
5. Leakage currents increase exponentially with voltage and can be explained by a surface-barrier-limited Schottky mechanism or a bulk-limited Pool-Frenkel mechanism of conductivity. Based on ε_{HF} estimations, Schottky conduction prevails at cryogenic conditions, whereas the Pool-Frenkel mechanism gives more adequate results at room temperature.
6. Breakdown voltages of tantalum capacitors, measured at the first scintillation, increase ~40% at LN compared to RT conditions. However, breakdown voltages measured during step surge current testing decrease ~40% at 77 K. This indicates that reliability of tantalum capacitors at cryogenic conditions might increase for high-impedance applications and decreases for low-impedance applications.

7. Six lots of tantalum capacitors were subjected to 500 cycles between 300 K and 77 K. No substantial variations of capacitance or ESR were observed, but two lots had increased leakage currents. However, even these two lots did not change significantly their propensity to surge current failures. The results suggest that tantalum capacitors are capable of withstanding up to 500 cycles between 300 K and 77 K, but the probability of failures is lot dependent. Reliability qualification testing of tantalum capacitors should include cryo-cycling and should be performed on each lot of parts intended for cryogenic applications.
8. Chip tantalum capacitors from two lots soldered onto FR4 boards withstood 100 cryo-cycles without failure, thus indicating high robustness of the parts to multiple exposures of extremely low temperatures. However, additional experiments are necessary to evaluate the effect of soldering on the results of cryo-cycling of the parts.

Part IV. Effect of Mechanical Stresses on Chip Tantalum Capacitors

IV.1. Introduction

Mechanical stresses in microelectronic components might significantly affect their performance and reliability. The ultimate manifestation of these stresses is cracking and fracturing of the component, which results in catastrophic failures. At lower stresses, degradation of characteristics and parametric failures might be due to micro-cracking in active and passive elements or to piezo-resistance effects. The latter is known to cause shifts of characteristics in linear devices, such as operational amplifiers and voltage reference microcircuits [41, 42] and excessive noise in ceramic capacitors [43].

Variations of mechanical stresses in components might be related to external factors such as soldering on a board, application of conformal coating, deformation of flexible boards during environmental testing, etc., or by internal factors caused by materials with different coefficients of thermal expansion (CTE) in the parts' design. Normally, manufacturers of components take the necessary measures to control the internal factors and assure that the level of stresses is sufficiently low, so reliability and performance of the parts is not compromised. However, additional mechanical stresses developed due to the external factors depend on the application conditions and design of the system.

Surface mount technology (SMT) passive components might experience especially high stresses due to a lack of stress relief. For ceramic capacitors, these stresses result in so-called flex cracking, which was a subject of multiple studies [43-47]. However, no data on the effect of mechanical stresses on chip tantalum capacitors have been found in technical literature.

Some publications indicate that mechanical stresses related to soldering of chip tantalum capacitors might affect their performance and reliability and might be responsible for turn-on breakdowns in the parts [15]. Surge current testing performed by manufacturers to reduce these types of failures may not be sufficient because thermo-mechanical stresses during reflow mounting process can generate new fault sites in the parts [5]. To avoid these failures proofing, or controlled power-up of the system, was suggested [15]. Soldering-induced defects are believed to be caused by excessive CTE of the molding compound when temperature exceeds Tg during the solder reflow process. The effect of soldering was found to be more pronounced for larger sized products, and capacitors manufactured by different vendors showed different sensitivity to soldering [4].

In this work, for the first time the effect of mechanical stresses on characteristics of chip tantalum capacitors has been demonstrated. Leakage currents and breakdown voltages during step stress surge current testing (3SCT) of several types of capacitors were measured at different compressive mechanical stresses (up to 500 N). An increase of leakage currents up to several orders of magnitude was observed. Contrary to the intuitive expectations, this increase was reversible. Mechanisms of the stress-induced degradation in chip tantalum capacitors and manifestations of the effect during testing and assembly of the parts are discussed.

IV.2. Experiment

To study the effect of compressive mechanical stresses on chip tantalum capacitors, a PC-based set-up shown in Figure 1 was used. A device under test was installed in a fixture with a top

electrode connected to a stress gage (Chatillion DFGS 200) while the bottom electrode was placed on a spring. Both electrodes were isolated from the Chatillion tension/compression tester (TSD 200) with ceramic insulators and connected to a Keithley 236 source measure unit to monitor current variations with time and applied force. For surge current testing, the Keithley 236 instrument was replaced with a test set-up for the step stress surge current measurements, and for capacitance measurements an impedance analyzer HP4192A was used.

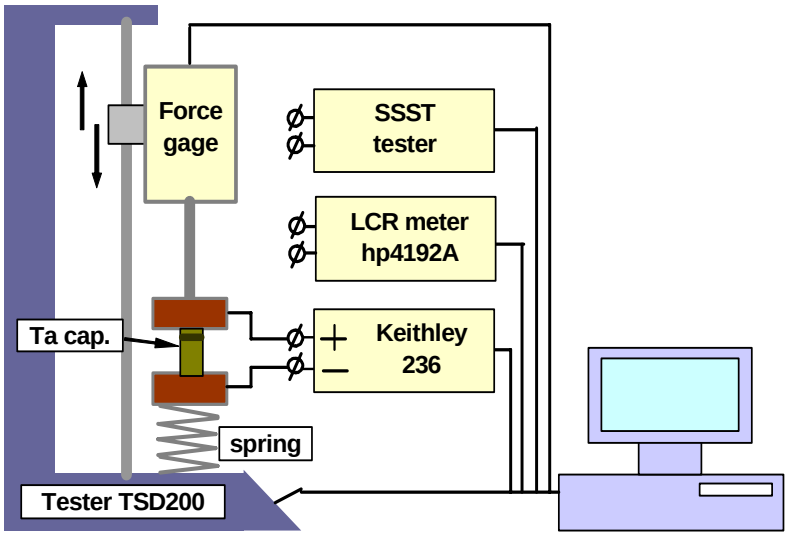


Figure 1. Experimental set-up.

During experiments, the pressure was gradually increased to a level where significant changes in the current were observed and then decreased to a safe level (typically ~10 N). These cycles were repeated with the maximum stress incrementally increasing to check for the effect of increasing stress and reversibility of the changes at different stress levels. To assess the value of parasitic, induced currents, control experiments were carried out when the current was monitored on parts without applied voltage while the stress varied up to 500 N. The results showed that at these conditions the currents were below ~10^{-8} A.

The step stress surge current testing was used to assess the effect of compressive stresses on the probability of surge current failures. During this test, a compressive stress was applied to the part, and the surge voltage was increased from the rated one in 2 V increments until the part failed. The testing was carried out using a PC-based data-capturing system with a field-effect transistor (FET) switch described in [8]. The current transients were monitored using an oscilloscope, and the failure event was determined when the current after the initial spike increased to more than 10 mA.

Parts used for the testing were commercial chip tantalum capacitors listed in Table 1. Five to 10 parts were used in each group.

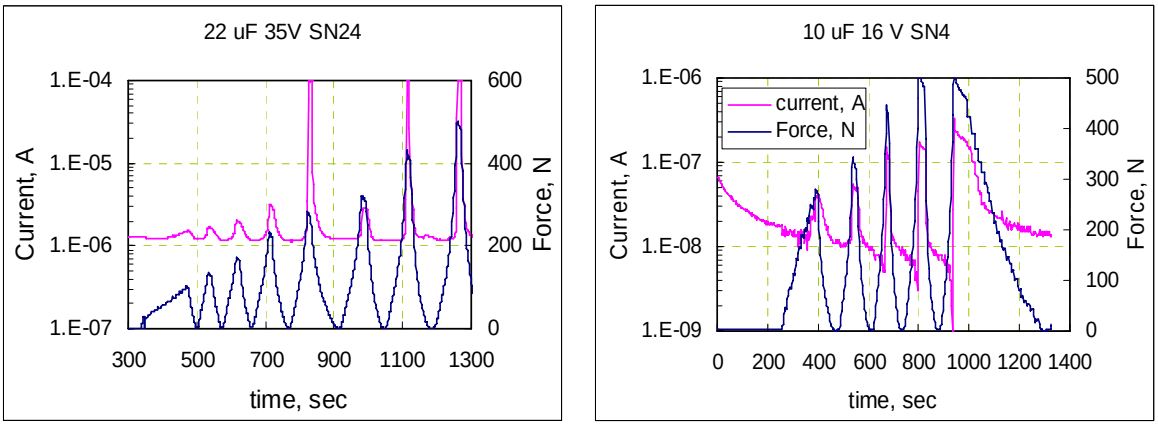
Table 1. Parts used for stress testing.

Capacitor	Type	Case Size EIA	H×W×L, mm^3
2.2 µF/ 35 V	T491C225K035AS	6032	2.49X3.34X6
1.5 µF/ 16 V	T491A155K016AS	3218	1.67X1.82X3.28
10 µF/ 16 V	T491C106K016AS	6032	2.49X3.29X6.08
15 µF/ 50 V	T495X156M050AS	7343	4.28X4.39X7.52
22 µF/ 35 V	T491D226M035AS	7343	2.85X4.33X7.39

IV.3. Results

IV.3.1 Effect of mechanical stresses on leakage currents

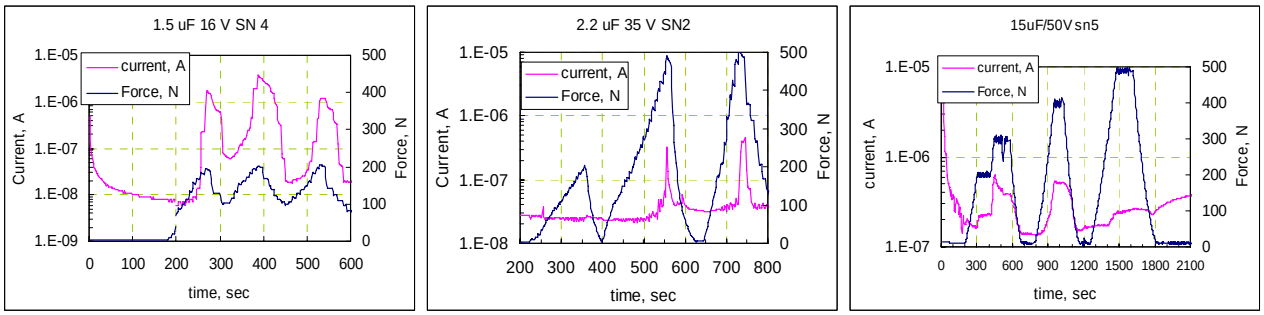
Shown in Figure 2 are typical variations of leakage currents with time for 22 µF/35 V and 10 µF/16 V capacitors, while the applied stress was changing periodically with increasing maximum stress. To allow for relaxation and stabilization of the current, the stress started increasing approximately 5 min. after the rated voltage was applied to the part. The results show that when the stress reaches ~50 N in the first case and ~250 N in the second case, the leakage currents are increasing approximately two times. These forces were defined in this work as critical, f_{cr}. An increase of the forces above the critical level results in further increasing of the leakage currents. At great enough stresses, the currents raised approximately two orders of magnitude as seen at ~250 N for 22 µF/35 V and at ~500 N for 10 µF/16 V capacitors. More surprising and less easily rationalized is the fact that these changes are reversible, and a decrease of the forces to a safe level (below ~10 N) restored the initial levels of the currents.



a) b)

Figure 2. Typical variations of leakage currents and mechanical stresses with time for 22 µF/35 V (a) and 10 µF/16 V (b) capacitors.

Similar results were obtained for all tested lots (see Figure 3). Notably, even after a significant (more than 10 times) increase of the current, the following decrease of the force in all cases returned currents to its initial values. However, the sensitivity to the stress in some cases was decreasing, so the greater stresses did not necessarily result in greater currents.



a) b) c)

Figure 3. Variations of leakage currents and mechanical stresses for 1.5 μF 16 V (a), 2.2 μF 35 V (b), and 15 μF 50 V (c) capacitors.

The level of critical stresses varied from lot to lot and from part to part within one lot. Statistical data for f_{cr}, including average values and standard deviations, calculated for five lots are shown in Table 2. An average critical stress, σ, which is also shown in Table 2, was calculated as a ratio of the average critical force and area, A_{cap}, of the part. The results show that the range of critical stresses in tantalum chip capacitors varies from 10 MPa to 40 MPa, and there is no correlation between σ and the size of the part. Note that although the critical stresses are relatively high, a large standard deviation of the distributions indicates a high probability of having samples with a relatively low σ and respectively with a high sensitivity to mechanical stresses.

Table 2. Statistical data on critical forces and stresses in chip tantalum capacitors.

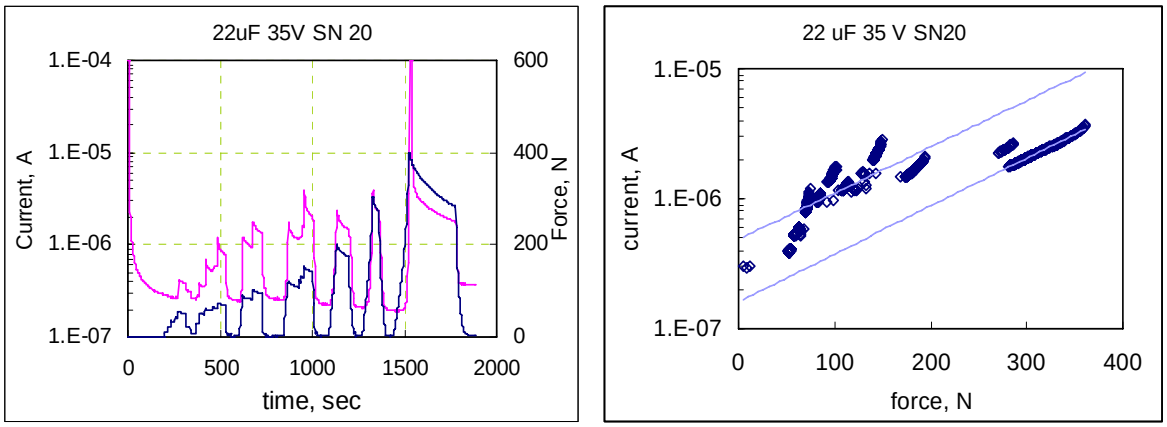
Capacitor	**Qty.**	**A_{cap}, mm^2**	**$f_{cr.\ avr}$, N**	**St. Dev.**	**σ, MPa**
2.2 μF/ 35 V	5	8.3	323	45	38.8
1.5 μF/ 16 V	5	10.0	205	29	20.6
10 μF/ 16 V	5	8.2	311	127	38.0
15 μF/ 50 V	7	18.8	441	201	23.5
22 μF/ 35 V	14	12.3	134	71	10.9

Figure 4a shows characteristics of a 22 μF/35 V capacitor where the stress was varied in such a way to allow estimation of the current-force relationship. Note that for this part, an increase in *f* to ~400 N resulted in a current spike with amplitude of more than 100 μA (compliance current limit). However, even in this case, after the current increased almost three orders of magnitude, a reduction of the force to below 100 N reduced the current to a sub-microampere level, which is only slightly above the initial current.

The *I(f)* relationship plotted based on the data presented in Figure 4a is shown in Figure 4b and suggests an exponential dependence of the current on compressive stresses:

$$I = B \times \exp(\alpha \times f) \quad , \qquad (1)$$

where α and B are empirical coefficients. Estimations showed that the coefficient α is in the range from 0.0082 1/N to 0.0085 1/N.

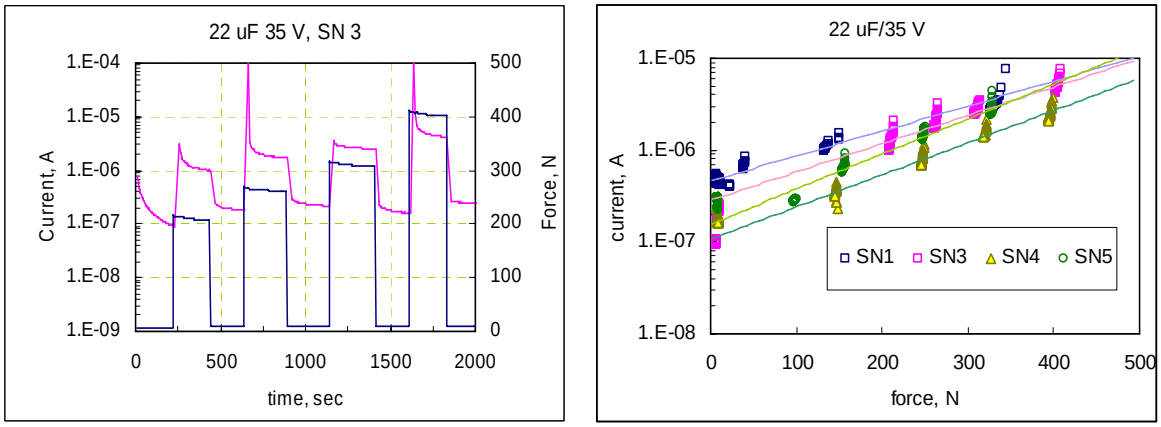


a) b)

Figure 4. Variations of leakage currents and mechanical stresses with time for a 22 μF 35 V capacitor (a) and dependence of the current on applied force (b).

To get a more accurate *I(f)* relationship, variations of the current with stresses were measured on four more 22 μF /35 V capacitors. In these experiments, mechanical stresses were stabilized at different levels for ~3 min. to allow for current stabilization. Typical results of these tests are shown in Figure 5a. In some cases, application of stress results in current spikes exceeding 100 μA. However, the stabilized currents are apparently independent of the initial spike and vary with the level of the stress, suggesting that the stress affects intrinsic leakage currents in the parts rather than trigging electrical breakdown of the dielectric. Note also that there is a time delay of a few seconds between the stress and current variations.

Current versus force characteristics for four 22 μF 35 V capacitors are shown in Figure 5b. The results confirmed that leakage currents increase exponentially with the stress, and the coefficient α in Eq. 1 varies in a relatively narrow range from 0.0063 1/N to 0.0088 1/N.



a) b)

Figure 5. Typical current variations in a 22 μF/35 V capacitor when compressive stresses were stabilized at different levels (a) and effect of the stress on leakage currents for four parts (b).

One might suspect that the observed effect is specific to tantalum capacitors with manganese cathodes only and is due to the presence of manganese crystals similar to those shown in Figure 6.

These crystals are capable of creating significant mechanical stresses and were hypotized to be responsible for failures in tantalum capacitors [49].

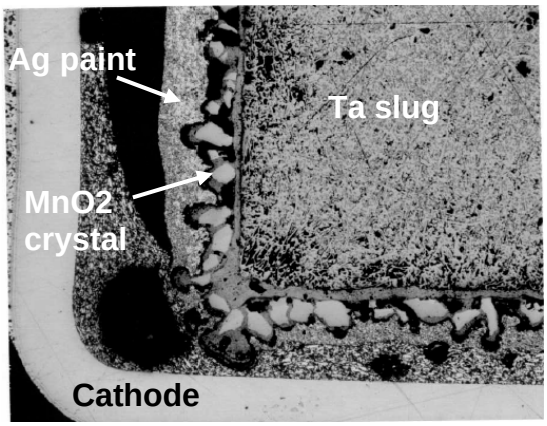
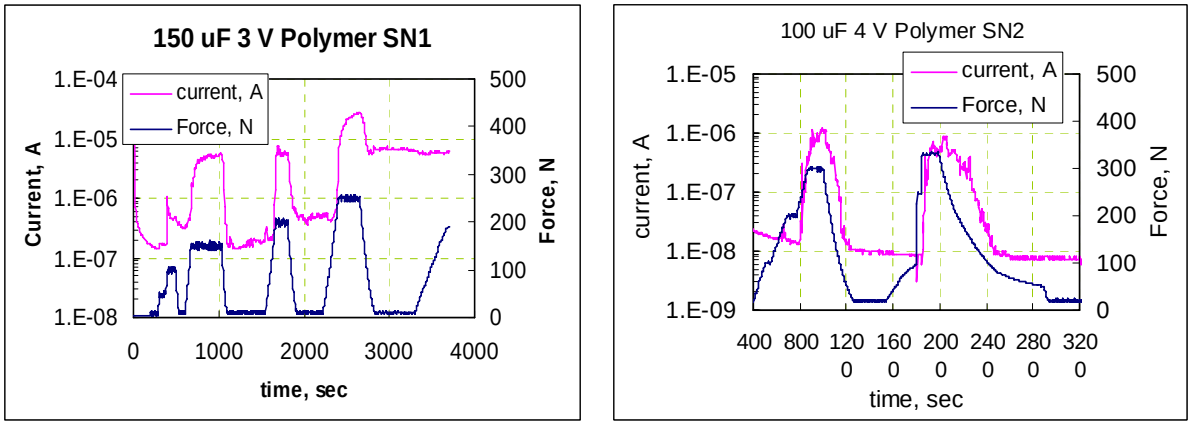


Figure 6. SEM view of a cross section of a tantalum capacitor showing crystals of manganese oxide.

To check whether the stress effect is specific to tantalum capacitors with manganese cathode only, two types of capacitors, 150 μF/3 V and 100 μF/4 V, with polymer cathodes were used. Results of measurements under variable stress conditions for these parts are shown in Figure 7 and clearly indicate that the stress-induced leakage currents vary reversibly in polymer capacitors similar to the manganese cathodes parts.



a) b)

Figure 7. Variations of leakage currents and applied stresses in 150 μF 3 V (a) and 100 μF 4 V (b) polymer tantalum capacitors.

IV.3.2 Effect of mechanical stresses on capacitance

Typical variations of the capacitance (C) and dissipation factor (DF) for a 22 μF /35 V part measured with time, while the compressive stress gradually increased up to 500 N, are shown in Figure 8. Both AC characteristics remained stable within the accuracy of the measurements, indicating that C and DF are not sensitive to mechanical stresses. It is important to note that this behavior is different compared to ceramic capacitors (X7R/X5R types), where mechanical stresses do cause changes in the AC characteristics. This, as well as the presence of the piezo-effect in

ceramic capacitors, results in different behavior of tantalum and ceramic capacitors in the presence of mechanical disturbances.

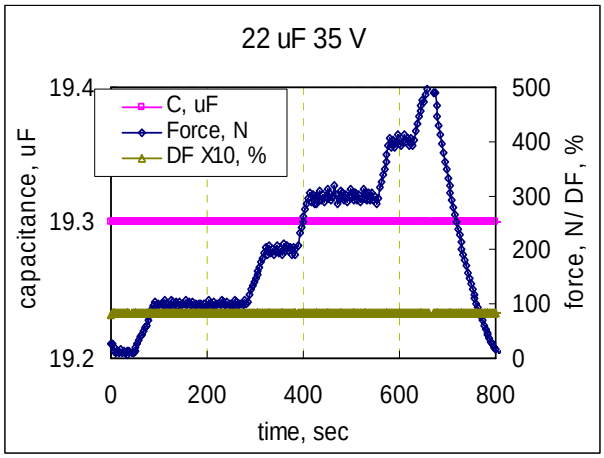
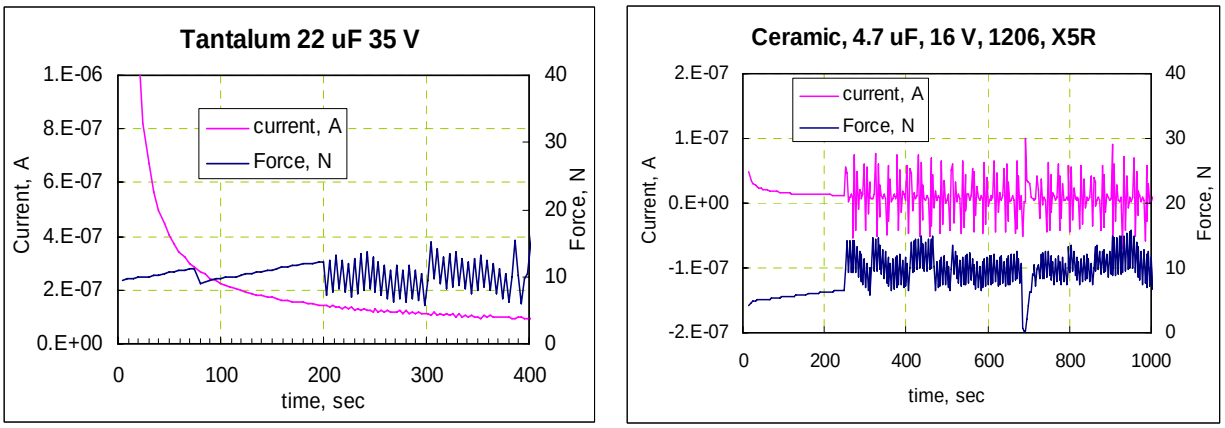


Figure 8. Variations of capacitance, dissipation factor, and compressive stress with time for a 22 μF/35 V capacitor.

A comparison of the behavior between tantalum and ceramic chip capacitors regarding their reaction to mechanical stress variations is shown in Figure 9. During these experiments, leakage currents in the parts were monitored while the stress varied periodically from 9 N to 14 N. It is seen that these stresses did not affect leakage currents in tantalum capacitors, whereas significant noise was generated in ceramic parts.



a) b)

Figure 9. Reaction of tantalum (a) and ceramic (b) capacitors to mechanical noise generated by periodical variations of the force between 9 N and 14 N.

IV.3.3 Effect of mechanical stresses on surge current failures

To assess the effect of mechanical stresses on surge current failures, five 22 μF/35 V capacitors were tested using a step stress surge current testing (3SCT) technique while the parts were stressed with a force of 100 N. A control group of samples was tested in the same set-up, but at a low compressive force of ~10 N or less.

To assure that the stress of 100 N would not cause substantial variations of the current when the rated voltage was applied, I-t characteristics of the parts were monitored prior to the surge current testing. Results of these experiments are shown in Figure 10 and indicate no variations, or relatively minor increase, in the currents, which all remained well below the specified limit of 7.7 μA for this device. Note also that in some cases the current starts increasing with time after the force is stabilized. The time required for current to reach a steady-state condition varies from 10 to 50 seconds and corresponds to the time delays observed in the experiments described above.

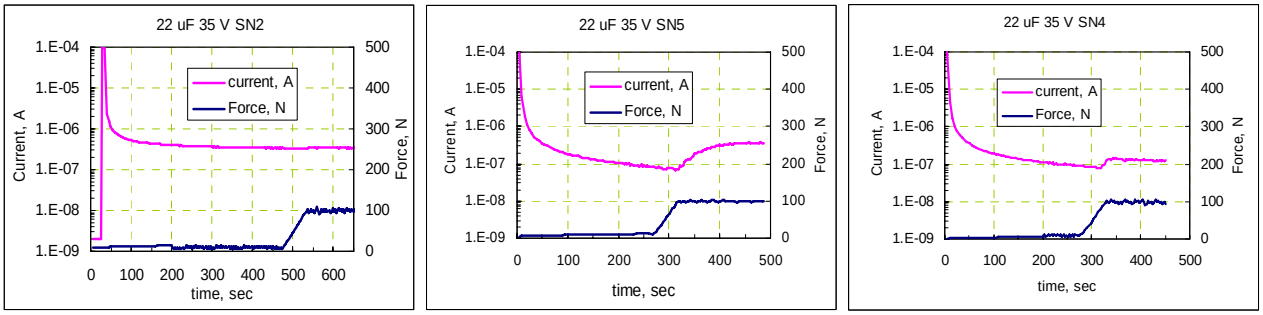


Figure 10. Variations of currents due to application of a force of 100 N in three 22 μF/35 V capacitors.

Weibull distributions of the breakdown voltages measured for the control group and for devices stressed with 100 N are plotted in Figure 11 and indicate a significant decrease in the breakdown voltages caused by the stress. The characteristic breakdown voltage decreased from 66.7 V initially to 46.7 V when the force was applied.

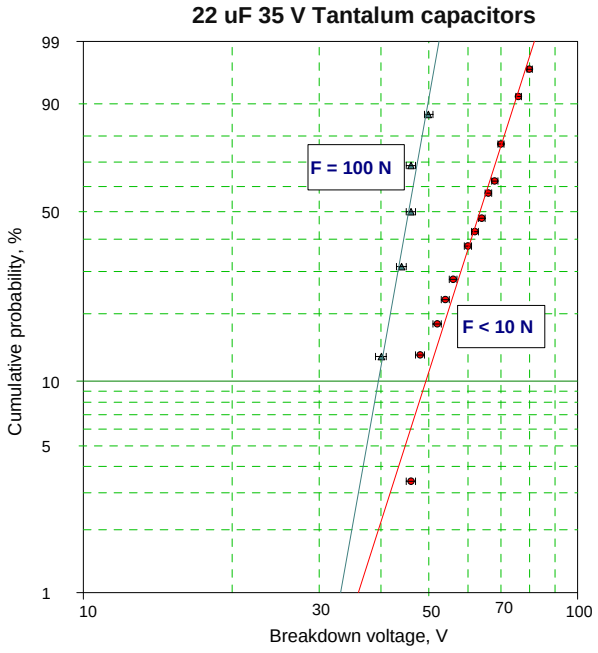


Figure 11. Weibull distributions of breakdown voltages measured during step stress surge current testing (3SCT).

Table 3 shows leakage currents and breakdown voltages for all parts tested under the stress. The current increase was calculated as a ratio of currents under the stress to initial currents. The results indicate a trend of decreasing of breakdown voltages for parts having a greater increase of current. However, additional experiments are necessary to obtain more accurate distributions of VBR and to check for a possible correlation between the current ratio and the level of decrease of the breakdown voltages.

Table 3. Leakage currents (A) and breakdown voltages of the parts used for 3SCT.

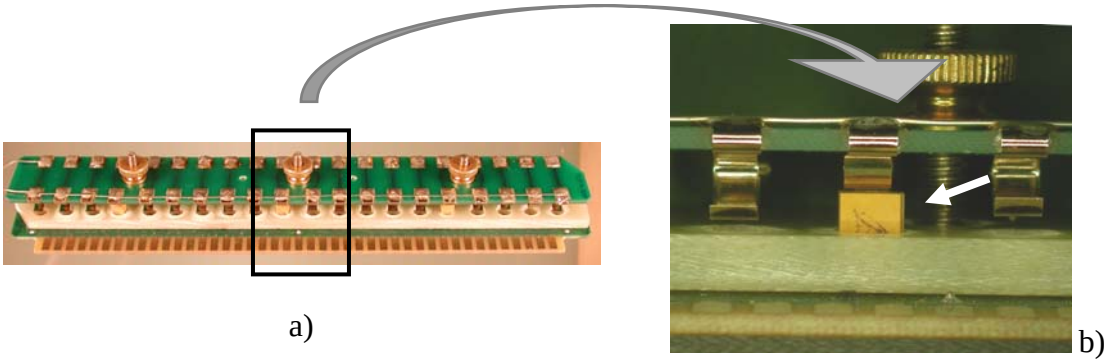
	Leakage Init. at 300s	**Leakage at 100 N**	**Current Increase**	**V_{3SCT}, V**
SN1	5.3E-08	4.3E-07	8.1	45
SN2	3.6E-07	3.5E-07	1.0	51
SN3	1.2E-07	3.6E-07	3.0	47
SN4	8.5E-08	1.3E-07	1.6	47
SN5	7.5E-08	3.6E-07	4.8	41

IV.4. Manifestations of mechanical stresses during testing and assembly

In this section of the report, effects of compressive stresses that might happen during testing (stresses in fixtures) and develop as a result of assembly on the board (soldering and conformal coating) on the performance of chip tantalum capacitors are demonstrated.

IV.4.1 Stresses caused by fixtures during testing

A multi-cell fixture typically used for testing of chip tantalum capacitors is shown in Figure 12. In some cases it is difficult to achieve electrical contacts in parts installed between the screws, and it would seem logical to tighten the screws more to improve these contacts. However, tightening a screw might increase significantly the stress on the parts close to the screw.



a) b)

Figure 12. An overall view of the fixture (a) and a close-up of a tantalum capacitor near the screw (b).

To assess the effect of these stresses, currents in 22 μF/35 V capacitors were monitored during 3 minutes after a certain level of stress in the fixture was achieved and the rated voltage was applied. The parts were depolarized for 3 minutes also after each cycle of measurements. The stress was increased incrementally by tightening the screw before the next cycle of testing. Typical results of these measurements are shown in Figure 13. It is seen that initially, at relatively low stresses, the

currents demonstrate normal and reproducible relaxation according to the power law, $I \sim t^{-n}$, where $n \approx 1$. However, starting from a certain level, an increase of the stress caused increasing of the leakage current, and when tightened firmly enough (the estimated stress was ~300 N), the currents increased more than two orders of magnitude. After this, the current did not return to the initial value, and an irreversible increase of more than an order of magnitude occurred. This behavior is completely consistent with the experimental results described earlier and indicates the possibility of damaging of the parts during testing.

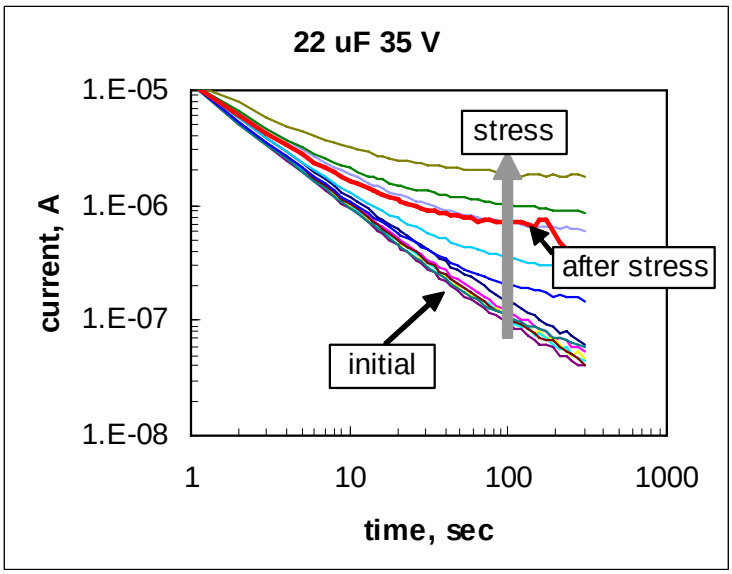
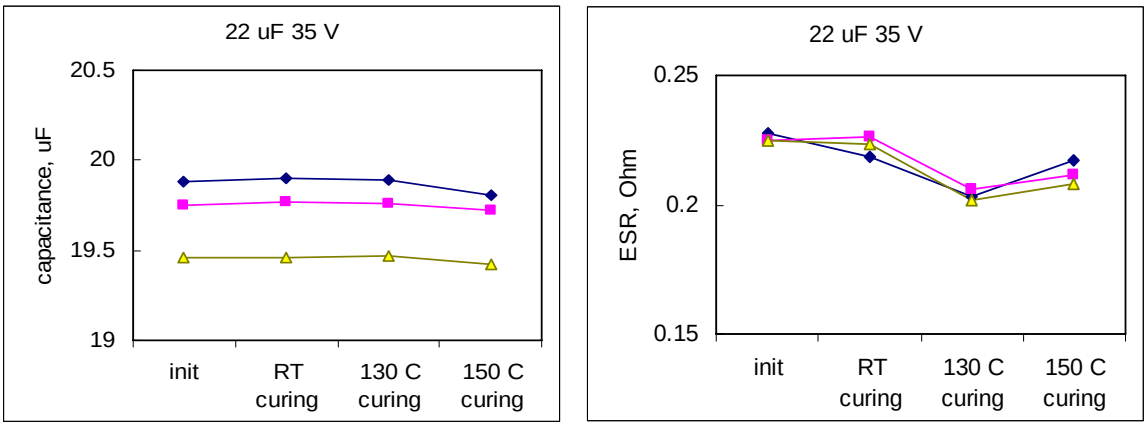


Figure 13. Leakage currents under increasing mechanical stresses caused by tightening of the multi-cell fixture.

IV.4.2 Effect of conformal coating

To simulate the effect of mechanical stresses developing in capacitors due to application of conformal coatings in a controllable way, 15 samples of 22 μF/35 V parts with short (~1 inch) soldered wires were potted into a low-stress, room-temperature curing, Struers EPOFIX epoxy. The parts were characterized initially and then after curing of the epoxy at different conditions, which were expected to increase the level of the stress in the parts. First, the parts were cured at room temperature for 15 hours, then at 130 ^{o}C for 15 hours, and finally at 150 ^{o}C for 15 hours.

Figures 14 and 15 show variations of AC characteristics and leakage currents in the parts caused by different curing conditions. The data indicate no significant variations in capacitance and ESR values, whereas leakage currents increased substantially after additional curing at high temperatures. Note that an increase in currents coincides with significant variations of the strain in the epoxy coating measured with a strain gage.



a) b)

Figure 14. Effect of curing conditions on capacitance (a) and ESR (b) of 22 μF/35 V capacitors potted in a low-stress epoxy.

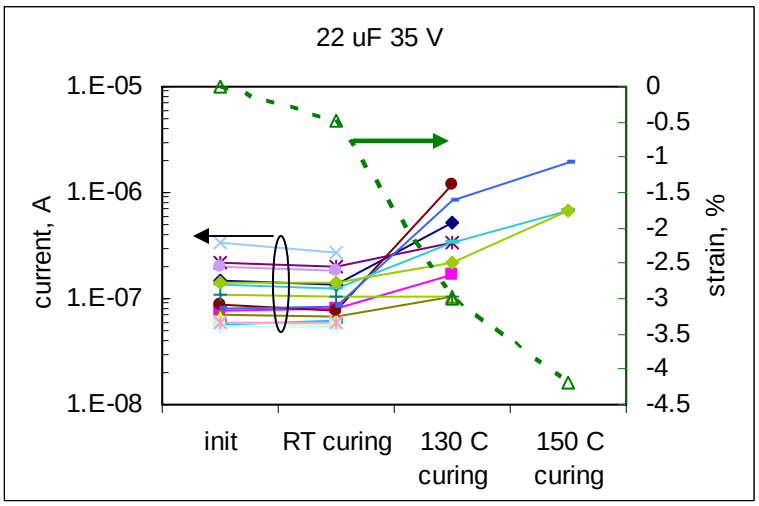


Figure 15. Effect of curing conditions on leakage currents in capacitors and strain in the epoxy compound.

To estimate mechanical stresses caused by the potting epoxy, thermo-mechanical characteristics of the material were measured using a thermo-mechanical analyzer TMA2940. The curing-induced shrinkage, S, was measured with a strain gage, KFG-3-350-C1-11L1M2R, potted in the epoxy together with the parts. Young's modulus of the potting material, E, was estimated based on room-temperature measurements of deformations in a sample under a stress of ~0.5 MPa. Thermo-mechanical characteristics of the potting epoxy cured at different conditions are shown in Table 4. It is seen that a high-temperature curing significantly increases the Young's modulus and the strain, whereas the values of CTE and glass transition temperature increase to a much lesser degree.

Table 4. Thermo-mechanical characteristics of potting epoxy cured at different conditions.

Condition	CTE, ppm/°C	Tg, °C	E, GPa	Strain, %
RT Curing	82	65	0.32	0.48
130 °C Curing	72	70	1.25	3.1
150 °C Curing	70	78	2.41	4.2

Based on these data, mechanical stresses created by the potting epoxy in tantalum capacitors were estimated as a sum of CTE-mismatch-induced and shrinkage-induced stresses using the following equation:

$$\sigma = E \times \left(\alpha_{PE} - \alpha_{cap}\right) \times \left(T_g - T_a\right) + E \times S \quad , \tag{2}$$

where α_{PE} and α_{cap} (~11 ppm/°C) are the coefficients of thermal expansion of the potting epoxy and tantalum capacitor, and T_a is the ambient temperature. Results of these calculations are shown in Table 5 and indicate that curing at high temperatures creates stresses that are above the level of the critical stresses shown in Table 2 of this part of the report. Note also that most stresses in high-temperature cured epoxy were caused by curing-induced shrinkage, whereas the CTE mismatch-induced stresses were only ~8 to 12 % of the total stresses. The results indicate that both, the level of compressive stresses and the degree of the increase of leakage currents are in agreement with the direct experiments described above.

Table 5. Stresses in tantalum capacitors caused by potting epoxy cured at different conditions.

Condition	CTE Stress, MPa	Curing Stress, MPa	Total Stress, MPa
RT Curing	1.1	1.5	2.6
130 °C Curing	4.1	38.8	42.8
150 °C Curing	8.8	101	110

Step stress surge current testing was carried out on two groups with six samples each after room-temperature curing and 130 °C curing and on a group of three samples after 150 °C curing. Results of these tests, together with the data obtained on a separate group of 20 samples tested without epoxy coating, are shown in Table 6.

Table 6. Effect of curing conditions on step stress surge current testing (3SCT) of 22 μF/35 V capacitors.

	Initial	RT Curing	130 °C/15 Hrs.	150 °C/15 Hrs.
VBR_3SCT, V	62.7	68.3	52	42.3
Std. Dev.	10.1	10.7	9.9	7.0
Qty.	20	6	6	3

Analysis of these data using Student's t-tests showed that a decrease of the breakdown voltages after additional high-temperature curing of the potting epoxy is significant at 95% confidence

level, whereas the effect of room-temperature curing is not significant. Based on results of these experiments, variations of leakage currents and average breakdown voltages measured during 3SCT were plotted against the calculated stresses in Figure 16.

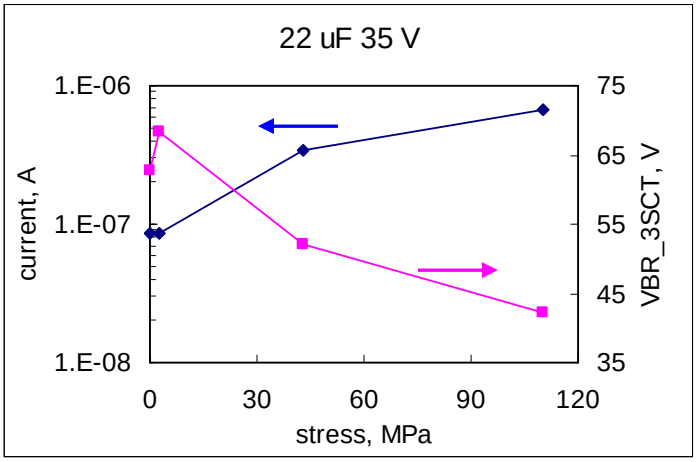


Figure 16. Variations of median leakage currents and average breakdown voltages measured during step stress surge current testing (3SCT) versus compressive stresses created by potting epoxy.

The results show that hydrostatic stresses created by potting epoxy result in degradation of leakage currents and breakdown voltages similar to the axial forces used in experiments described in section IV.3.1. Conformal coatings might affect performance and reliability of chip tantalum capacitors, and the effect might be especially significant for small-sized parts coated with relatively thick layers of polymers having high Young's modulus and curing-related shrinkage.

IV.4.3 Effect of soldering

During soldering of a chip tantalum capacitor onto a printed wiring board (PWB), both the capacitor and the board are heated up to temperatures above the melting point of solder (typically to ~230 ^{o}C), which solidifies when the system is cooled down to room temperature. Due to differences of the coefficients of thermal expansion, mechanical stresses would build up as the temperature decreases below the point of solidification of the solder. However, when the temperature remains above the glass transition temperature of the PWB, Tg_{PWB}, so that the material remains in a rubbery state, the level of these stresses is relatively low, and for rough estimations we can assume that the stresses are building up only after temperature decreases below Tg_{PWB}, when the material transforms into a more rigid, glassy state.

To estimate these stresses, consider a simplified schematic of a tantalum capacitor soldered onto a PWB shown in Figure 17. When a free capacitor of a length l and CTE = α_{cap} and PWB with a CTE = α_{PWB} cool down from T_g to room temperature, T_r, their deformations are:

$$\Delta l_{cap} = \alpha_{cap} \times l \times (T_g - T_r), \qquad \Delta l_{PWB} = \alpha_{PWB} \times l \times (T_g - T_r) \tag{3}$$

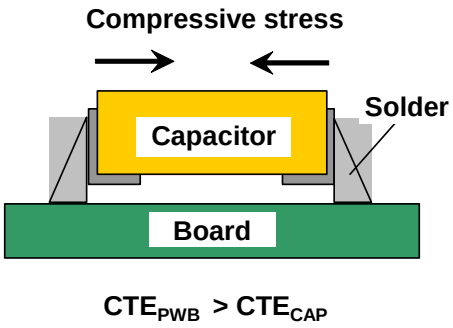


Figure 17. A schematic of stresses developed in a tantalum chip capacitor during soldering.

For a soldered capacitor, the deformation should be the same as for a PWB, and this condition is achieved by developing of a force, F, which compresses the capacitor and expands the board:

$$\Delta l_{cap} + \Delta l_{cap}^{F} = \Delta l_{PWB} - \Delta l_{PWB}^{F} \quad , \tag{4}$$

where $\Delta l_{cap}^{F} = l \times \frac{F}{A_{cap} \times E_{cap}}$, $\Delta l_{PWB}^{F} = l \times \frac{F}{A_{PWB} \times E_{PWB}}$,

are the force-induced deformations, A_{cap} and A_{PWB} are the cross-sectional areas of the capacitor and PWB, and E_{cap} and E_{PWB} are their effective Young's modulus. These equations are based on a one-dimensional model, on an assumption that materials follow Hookian's behavior, and that the temperature variations of E and α in a glassy state can be neglected. Based on these assumptions the compressive force and relevant stress in a tantalum capacitor soldered onto a board can be expressed as:

$$F = \frac{(\alpha_{PWB} - \alpha_{cap}) \times (T_g - T_r)}{(A_{cap} \times E_{cap})^{-1} + (A_{PWB} \times E_{PWB})^{-1}} \qquad \sigma = \frac{F}{A_{cap}} = \frac{(\alpha_{PWB} - \alpha_{cap}) \times (T_g - T_r)}{(E_{cap})^{-1} + \left(E_{PWB} \times A_{PWB} / A_{cap}\right)^{-1}} \tag{5}$$

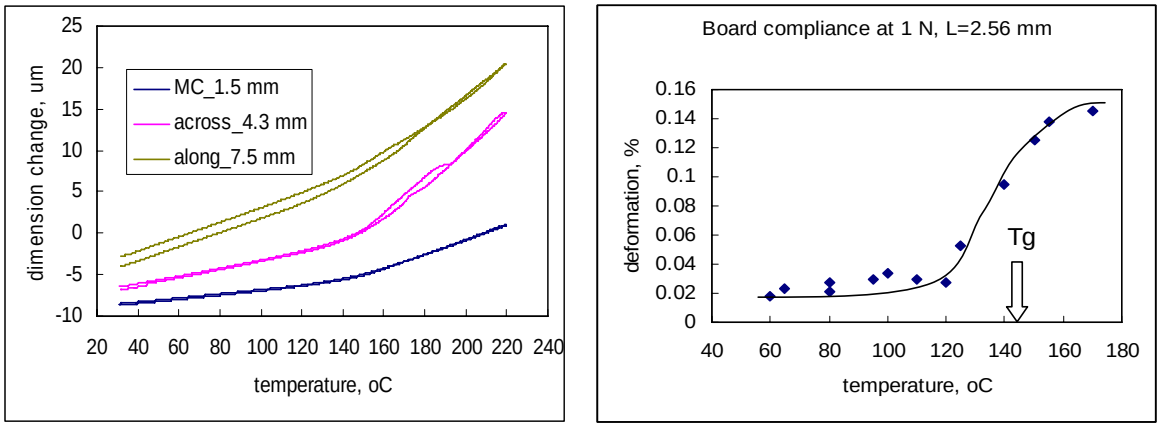
To get the necessary parameters for calculations, thermo-mechanical characteristics of 50 μF/50 V tantalum capacitors have been measured using a thermo-mechanical analyzer, TMA2940. Deformation of the part was measured during heating up to 220 ^{o}C and cooling to room temperature at a rate of 3 ^{o}C/min. along and across the part. Characteristics of the molding compound (MC) were measured on pieces cut from the plastic packages. Results of these measurements are shown in Figure 18a. The slopes of the curves indicated effective values of CTE and the glass transition temperature was determined as a point of inflection of two straight lines. Characteristics of the capacitors are summarized in Table 7.

The results show that the glass transition temperature measured on the capacitors and MC were close and ranged from 144 ^{o}C to 151 ^{o}C, whereas the values of CTE in a glassy state for the part were much less than for the MC. A decrease of the effective CTE of the part compared to the MC is due obviously to the presence of tantalum slug, which has CTE = 6.6 ppm/^{o}C. Interestingly, the effective value of CTE for chip tantalum capacitor is close to the values of CTE for chip ceramic capacitors measured for NPO and BX types to be in the range from 7 ppm/^{o}C to 10.3 ppm/^{o}C [44].

Table 7. Thermo-mechanical characteristics of 50 μF/50V capacitors.

	Tg. °C	CTE1, ppm/°C	CTE2, ppm/°C
Cap. Along	144.2	11.4	26.3
Cap. Across	150.8	11.6	56.4
MC	143.3	17.3	59.2

Thermo-mechanical characteristics of the FR4 board (Tg and E) were estimated based on measurements of deformations of a sample with a size of 2×2×2 mm under a load of 1 N applied periodically as the temperature varied from room to 180 °C. Results of these measurements are shown in Figure 18b. Note that the compliance of the board (~1/E) increases significantly at T > Tg, and the glass transition temperature determined at the point of inflection (141 °C) was close to the Tg of tantalum capacitors (143 °C to 150 °C). For this reason, the value of Tg for calculations per Eq. 5 was assumed to be 145 °C.



a) b)

Figure 18. Thermo-mechanical characteristics of 15 μF/50 V chip tantalum capacitors (a) and temperature dependence of the compliance of the FR4 board (b).

Based on our data and thermo-mechanical characteristics of materials reported in literature, parameters used for estimation of the soldering-induced stresses per Eq. 5 are shown in Table 8.

Table 8. Thermo-mechanical characteristics of materials used for calculations.

	E, Pa	α, ppm/°C	Tg, °C
Ta Cap.	5.00E+10	11.5	145
PWB (FR4)	1.75E+10	16	

The areas of the capacitor and board were calculated as a product of their thicknesses and effective widths, $A_{cap} = h_{cap} \times W_{cap}$ and $A_{PWB} = h_{PWB} \times (W_{cap} + 2 \times h_{PWB})$. Results of calculations per Eq. 5 for different part types and for the boards with the thickness 1.5 mm ($\sigma_{1.5}$) and 3.0 mm ($\sigma_{3.0}$) are presented in Table 9.

Table 9. Calculated soldering-induced mechanical stresses in tantalum capacitors.

Cap.	A_{cap}, mm^2	F, N	$\sigma_{1.5}$, MPa	$\sigma_{3.0}$, MPa
2.2 µF/ 35 V	2.49×3.34	70.8	8.6	16.3
1.5 µF/ 16 V	1.67×1.82	41.5	13.5	21.7
10 µF/ 16 V	2.49×3.29	70.8	8.6	16.3
15 µF/ 50 V	4.28×4.39	96.7	5.1	10.9
22 µF/ 35 V	2.85×4.33	87.2	7.2	14.2

The results show that the stresses for a 1.5 mm board vary from ~5 MPa to 13.5 MPa and are only slightly below the average critical stresses, which according to Table 2 vary from ~10 MPa to ~40 MPa. For a board that is two times thicker, the stresses are greater by approximately two times and are within the range of the average critical stresses. Note also that possible variations in the parameters of the capacitors and boards and, most importantly, variations of the critical level of the stress from part to part might create a situation in which the soldering-induced stresses would be sufficient to degrade characteristics of the capacitor after soldering even on a relatively thin boards.

To assess the effect of soldering experimentally, leakage currents were measured for 15 samples of 22 µF/35 V capacitors before soldering onto an FR4 board having a thickness of 1.5 mm, after soldering, and then after de-soldering. Results of these experiments are shown in Figure 19 and indicate that two parts, which had large currents initially, significantly decreased their leakage currents, and three parts, which had initially low currents, reversibly increased their values from ~7E-8 A to 1.5E-6 A after soldering. It is quite possible that the decrease of the current in the two samples was due to the high-temperature annealing effect, which was discussed in section II.5.4, whereas reversible variations of the currents in the three parts were most likely caused by the soldering-induced mechanical stresses. However, more analysis is necessary to accurately assess the effect of soldering on characteristics of chip tantalum capacitors.

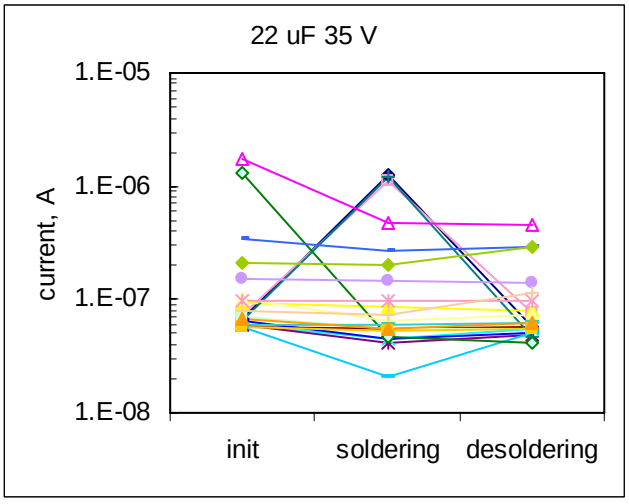


Figure 19. Effect of soldering onto an FR4 PWB of 22 µF/35 V chip tantalum capacitors.

IV.5. Discussion

The observed results can be explained by a combination of two mechanisms: stress-induced scintillations and stress-induced generation of electron traps in tantalum pentoxide dielectric. The first mechanism occurs at relatively great forces, far exceeding the critical ones, and is due to formation of macro-defects in the dielectric (e.g., micro-cracking). Formation of these defects can trigger a local momentary breakdown followed by the self-healing process, which is well known in solid tantalum capacitors with manganese cathodes [36, 50] and was observed recently even in polymer tantalum capacitors [6]. The scintillations result in relatively large current spikes and might cause irreversible increase of the leakage current due to incomplete conversion of the conductive MnO_2 into a high-resistive Mn_2O_3 phase and/or not complete coverage of the whole area of the defective dielectric with Mn_2O_3. However, scintillations cannot explain reversible variations in the leakage currents observed in our experiments after the stress removal.

The second mechanism, trap generation, is due to a stress-induced formation of microscopic defects, such as broken Ta-O bonds, and generation of oxygen vacancies, which increase the concentration of electron traps in the dielectric. According to the Pool-Frenkel mechanism, which is a prevailing mechanism of conductivity in thin tantalum pentoxide films at normal operating conditions [51], the density of leakage current can be described by the following expression:

$$J = C_t E \exp\left(-\frac{q\Phi}{kT}\right)\exp\left(-\frac{\beta_{PF}E^{1/2}}{kT}\right), \qquad (6)$$

where C_t is a trap density related constant, E is the electric field, q is the charge of the electron, Φ is the barrier height, k is the Boltzmann constant, and T is the absolute temperature, and

$\beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon}\right)^{1/2}$ is the PF constant, ε_0 is the permittivity of free space, and ε is the high-frequency dielectric constant.

The trap concentration is determined by a dynamic equilibrium of two concurring and competitive processes: generation of stress-induced defects and their annealing (e.g., recombination of the broken bonds). When the stress is removed, the concentration of the traps returns to its initial value and so does the leakage current. Both generation under the stress and recombination after stress removal develop with time, and based on our data, the characteristic time of the process is in the range of a few seconds to dozens of seconds. Considering exponential dependence of the leakage current on the stress, it is reasonable to assume that the concentration of the electron traps also increases exponentially with the stress.

It should be noted that a similar mechanism related to the enhanced bond breaking due to physical stresses was used to explain factors affecting reliability of gate oxides in microcircuit [52, 53]. The effect of mechanical stresses on the rate of failures caused by the time-dependent dielectric breakdown (TDDB) in the gate-oxide films of MOS transistors was demonstrated in [54]. It was shown that time to failure decreased almost two orders of magnitude as stresses in the oxide increased from 80 MPa to 170 MPa.

The TDDB effect in solid tantalum capacitors was demonstrated in [55] more than 40 years ago. The mechanism of this effect was explained similarly to the TDDB in SiO_2 films by a degradation of the dielectric through creation of defective microscopic sites, such as broken bonds and their

accumulation with time to the moment when a critical density of the defects is forming a conductive path, resulting in a thermal runaway breakdown [56].

Mechanical stresses cause strain in the atomic bonds in a dielectric, thus weakening them and enhancing the rate of de-bonding and generation of the defects in the presence of high electrical fields. Accumulation of these defects with time to a degree to which it affects conduction of the tantalum pentoxide dielectric explains also the time-dependent effects and hysteresis observed during measurements of stress-induced leakage currents.

The value of pressure that causes trap generation is obviously not equal to the average pressure in the package of the part. Due to the sponge-like structure of the tantalum capacitor, mechanical stresses in the package create local stresses in the dielectric, which are spread over the whole slug not uniformly, so in some locations the stress can be substantially greater than an average stress in the package. These locations are most likely responsible for increased leakage currents in the stressed capacitors.

IV.6. Conclusion

1. The effect of compressive stresses on different types of chip tantalum capacitors has been investigated by monitoring characteristics of the parts while the stress applied to the terminals varied up to 500 N.
2. No significant variations in capacitance and ESR were observed. However, at stresses exceeding a certain critical level, leakage currents increased exponentially with the stress and at sufficiently great stresses exceeded the initial currents on more than two orders of magnitude. Different part types have different sensitivity to mechanical stresses, and the average level of critical stresses varied from 10 MPa to 40 MPa.
3. The most interesting feature of the stress-induced currents is that they are completely reversible at relatively low stresses, thus ruling out a simple "damage-induced" mechanism of the phenomenon. After application of sufficiently great stresses only, the currents do not recover completely after the stress removal.
4. Compressive stresses might significantly increase the probability of surge current failures. Application of a stress of 100 N to 22 μF/35 V capacitors reduced the characteristic breakdown voltage from 66.7 V initially to 46.7 V.
5. Capacitors with polymer cathodes have demonstrated stress-induced leakage currents similar to the manganese cathode capacitors. This indicates that the effect is not related to the type of the cathode used and is a characteristic feature of the Ta-Ta_2O_5 system.
6. The effect of stresses developed in chip tantalum capacitors during testing and assembly onto a board on their characteristics has been demonstrated.
    - Mechanical stresses caused by multi-cell fixture can increase leakage currents by more than two orders of magnitude. To avoid damaging the parts, the stresses during testing should be maintained below ~10 N.
    - Stresses caused by conformal coatings might increase leakage currents and the susceptibility of capacitors to surge current failures. Experiments showed that the hydrostatic pressure created by epoxy coating affects leakage currents and surge current breakdown voltages similar to the axial stresses. The effect might be especially significant

for small-size parts coated with relatively thick layers of polymers having high Young's modulus and significant curing-induced shrinkage.

- Estimations showed that compressive stresses caused by soldering of chip tantalum capacitors on FR4 boards are in the range from 5 MPa to 22 MPa, which is within the range of average critical stresses. Variations of the critical stresses from part to part and changes in soldering conditions might result in a situation when soldering-induced stresses would be sufficient to degrade characteristics of the capacitor. Preliminary experiments showed the possibility of the soldering-induced degradation; however, more analysis is necessary to evaluate this effect.

7. The effect of reversible variations of leakage currents with stresses was explained by reversible changes of the concentration of electron traps under local stresses in the tantalum pentoxide dielectric. These traps enhance the conductivity of Ta_2O_5 according to the Pool-Frenkel mechanism, and variations of their concentration with time explain hysteresis and time delay effects in the stress-induced leakage currents. Large current spikes of more than two orders of magnitude and irreversible portion of leakage current variations at high enough stresses are most likely due to the formation of macro-defects and scintillation breakdowns in the parts.

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