Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA

Body of Knowledge Guideline Document on Commercial MNOS EEPROM in Space Applications

NEPP 2005 Task Final Report

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Scope

This investigation is sponsored by NASA Electronic Parts and Packaging Program, 2005. The objective of this task is to prepare a body of knowledge guideline document summarizing recent problems and lessons learned for space applications of the commercial metal-nitride-oxide-silicon technology EEPROMs. Risk mitigation and recommendations are also provided in the final report.

Section I. MNOS EEPROM Technology for Space Applications

MNOS EEPROMs [1] utilize a metal-nitride-oxide-silicon (MNOS) transistor and two MOS switch transistors as a memory cell. For a 2-μm CMOS fabrication process, the cell area is 118 μm^2 and the MNOS structure has a tunnel SiO_2 layer of 1.6 nm and a Si_3N_4 layer of 28 nm in thickness, shown in Figure 1 [1].

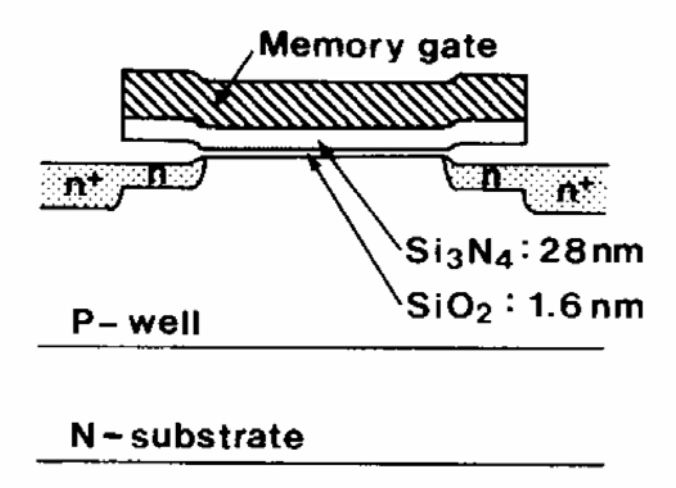

Figure 1. Schematic of the MNOS memory transistor.

Figure 2 [1] gives the basic operations of the MNOS memory cell. V'_{pp} is an internally generated negative high voltage with a typical value of -10V. V_d is a readout drain voltage of approximately 1V.

Program (Write): negative V'_{pp} is applied to the well, 5V is applied to the gate of the selected memory cell, and electrons are injected from the channel and then stored in the electron traps of the Si_3N_4 layer.

Erase: negative V'_{pp} is applied to the gate of the selected memory cell, 5V is applied to the well, and holes are injected from the Si substrate and then stored in the hole traps of the Si_3N_4 layer.

Program (Write) inhibit: 5V is applied to the drain of the de-selected memory cell, and voltage potential between the gate and channel is zero.

Read: 0V is applied to the gate of the selected memory cell, then erased states (ONE's or "1") or written states (ZERO's or "0") are read out, according to the channel current varied with the threshold voltage of the MNOS transistor.

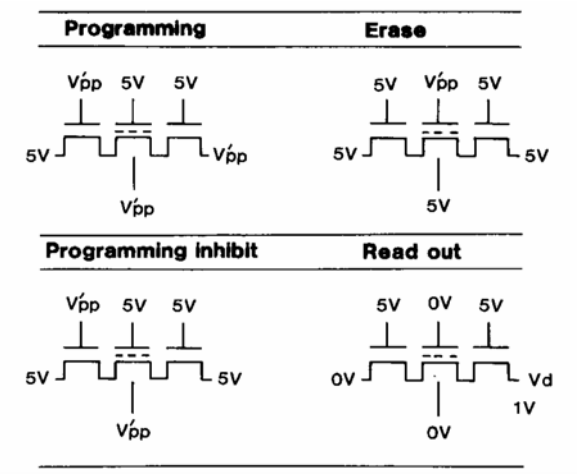

Figure 2. Basic operation schematics for the MNOS EEPROM memory cell.

1.1 Endurance and data retention

Endurance refers to write/erase-cycle endurance and is typically defined in commercial industry as the number of write/erase cycles at which the cumulative chip failure percentage reaches 1%. One write/erase cycle means re-writing all bits on the MNOS EEPROM chip.

Data retention refers to the memory's ability to retain data and is defined in commercial industry as the number of years at which the cumulative chip failure percentage has reached 1% at a certain ambient temperature. The device is regarded as a data retention failure when there is at least 1 bit of data that cannot be read.

Both endurance and data retention characteristics are functions of temperature. Data retention is also a function of the number of erase/write cycles. A typical MNOS EEPROM with zero erase/write cycles has a 10-year life at 70ºC. 10,000 erase/write cycles typically shows a 10X degradation of data retention.

1.2 Radiation

MNOS technology has typical tolerance for a commercial part, i.e. the peripheral CMOS has a TID limit of 30 krad(Si), the charge pump used in write commands has a limit of 7 krad(Si), and the MNOS array is robust to TID well in excess of 100 krad(Si) [2].

Concerning anomalous charge loss from a single bit from a heavy ion strike, Blandford et al. demonstrated that no errors occur in a properly programmed commercial MNOS device after exposure to a flux of 1e7 cm^{-2} of high LET ions [2].

Section II. MNOS EEPROM Reliability – Intrinsic Cells versus Weak Cells

2.1 EEPROM Weak Cells

There are two types of memory cells, “intrinsic or healthy cells” and “extrinsic or weak cells”. Intrinsic or healthy cells represent the majority of the memory cells on chips. Extrinsic or weak cells refer to any memory cell whose reliability behavior is not related to its structural, functional or material properties.

10-year data retention, as we mentioned in the previous section, is for intrinsic cells, not for weak cells. Weak cells may have several order of magnitude shorter lifetime, i,e, shorter data retention or endurance life, higher failure rate, lower activation energy, etc.

“Weak cells” can be induced by process and/or poor programmed timing and/or noise margin.

2.1.1 Weak cells induced by process defects

Process-induced weak cells can be defective cells resulting from defective oxide, oxide thinning, oxide excessive trapping, abnormal leakage path through silicon or oxide, adjacent via bridging, adjacent metal bridging, metal flake, metal void, etc. As a result, these weak cells cannot hold as much charge as nominal cells, nor as long as nominal cells.

2.1.2 Weak cells induced by users

Errors in timing margin in programming can also induce weak cells. In this case, the cell may either have lower write voltage or shorter write time, which results in less charge stored in the cell to begin with and therefore shorter data retention lifetime. One example is when the write time is less than 100ns and/or hold time is less than 10ns before performing read-after-write operation. Errors in noise margin can also cause weak cells. One case is when the noise width on the control pins is over 20ns during read and standby mode that may act as a trigger to turn the device to programming mode.

Key point #1:

EEPROM reliability concerns come from weak cells, which can be induced by either processes or users.

Key point #2:

The best practice of avoiding the process defect induced weak cells is to perform effective screening on the EEPROMs.

Key point #3:

The best practice of avoiding the programming induced weak cells is to understand the EEPROM device and make sure that all worst case timing meets the requirements in the data sheet.

2.2 Screening for Weak Cells

In addition to the screening process of MIL-PRF-38535, an effective data retention screening process should require the following:

1. EEPROMs are programmed with a checkerboard pattern and then placed un-powered for at least 78 hours at 150ºC;
2. Upon completion of the 78-hour data retention test, the patterns need to be verified;
3. EEPROMs which have passed the pattern verifications are programmed with the inverse checkerboard pattern and then placed un-powered for at least 78 hours at 150ºC;
4. Upon completion of the 78-hour data retention test, the patterns need to be verified and EEPROMs which have failed the pattern verification should be removed from the lot.

Activation energy of 1.1eV [1] was used to estimate the testing duration and testing temperature for the above data retention screening for a target 10-year data retention time at 70ºC. It should be noted that both static and dynamic burn-in as well as electrical characterizations at both high temperature (85ºC) and low temperature (-55ºC) need to be performed on the EEPROMs during the MIL-PRF-38535 process.

2.2.1 Screening does NOT mean zero failure in applications

Performing screening testing on the EEPROMs does not guarantee zero failure of the devices.

First, the purpose of an effective and successful screening testing is to eliminate the infant mortality failures and, therefore, the devices which have passed the screening testing should be operating at the bottom portion of the bath tub curve, shown in Figure 3. Compared to infant mortality region and wearout region, the failure rate of the operational region, i.e. the bottom portion of the bath tub curve, is much lower. The typical failure rate for the operational region is around 20 to 100 FIT, which is 20 to 100 failures per 10^9 device hours. The failure rate is low, but it is NOT zero.

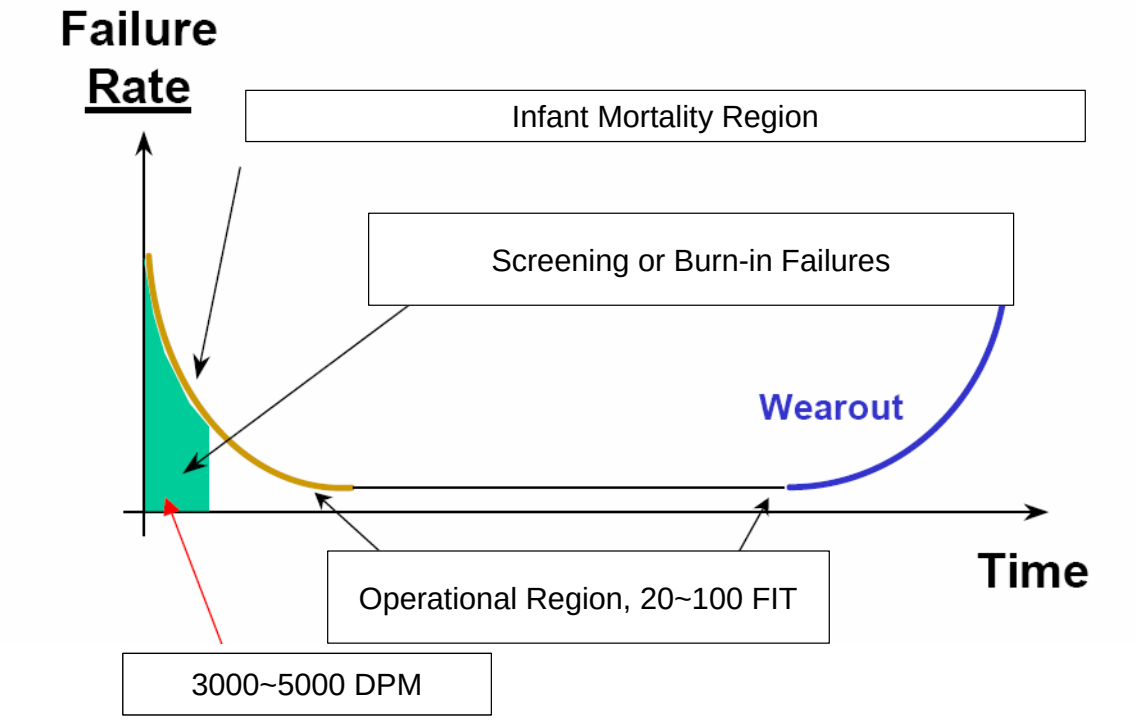

Figure 3. Bath tub curve.

Second, no screening testing can eliminate ALL POTENTIAL RELIABILITY DEFECTS. An effective screening testing can only detect ALL yield defects and SOME of the potential reliability defects.

Shown in Figure 4, process defects can be categorized by four groups depending on their sizes and locations on the circuits:

1. Defects which are smaller enough or in locations where they will never be yield or reliability concerns.
2. Potential reliability defects: defects are smaller enough or in locations where they may not be yield concerns, but can cause reliability failures in applications. In this case, time-dependent nature of some failure mechanisms can contribute to the potential reliability field failures.

3. Potential yield defects: defects are smaller enough or in locations where they do not cause initial yield failures, but can potentially cause parts to fail if parts are tested under an accelerated condition. In this case, the defects can be detected during screening testing.
4. Yield defects: defects are large enough or in locations where they cause yield failures, i.e., functional failures during wafer level or package level initial electrical testing.

As we can see, screening testing can reduce the failure rate by screening out the yield defects (category 4) and some of the potential yield (category 3) and reliability defects (category 2). But no screening testing can guarantee to screen out ALL the reliability failures for ALL parts. Therefore, in order to achieve a possible near-to-zero failure for mission, redundancy at different levels i.e. bit, page or image, is needed for the EEPROMs.

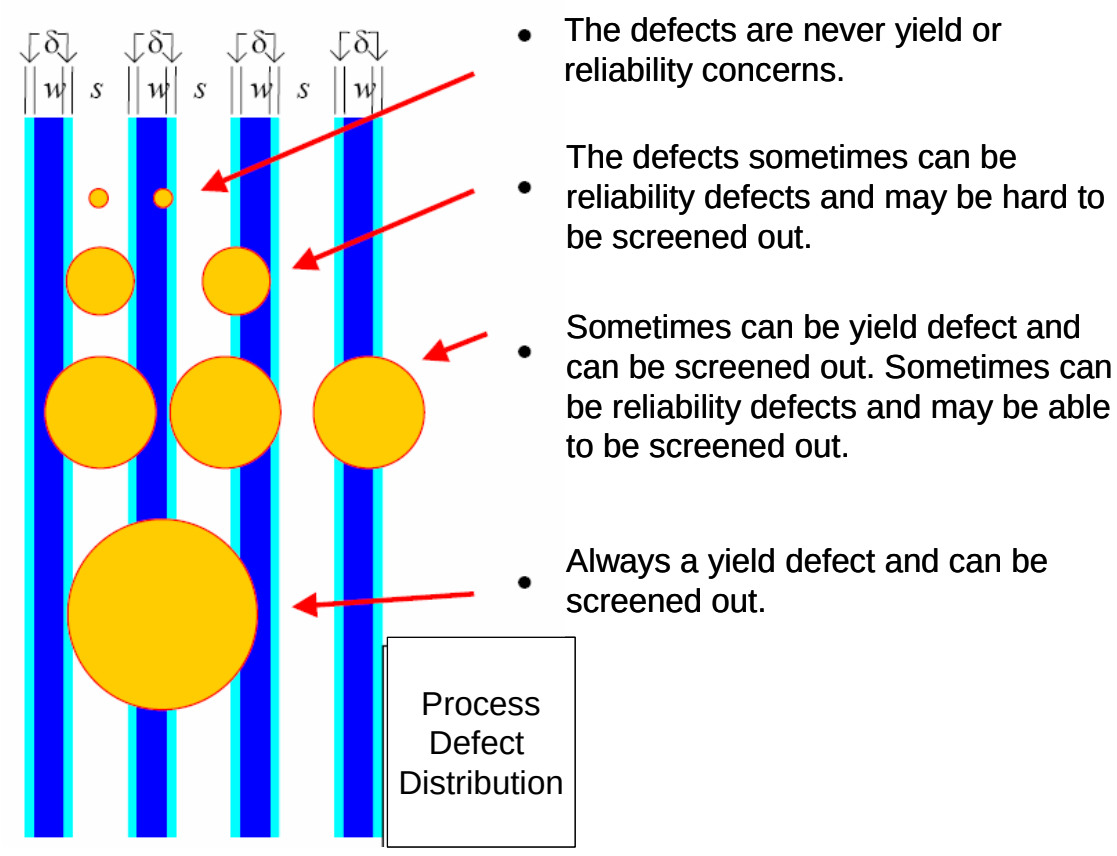

Figure 4. Defect distribution – schematics of yield and reliability defects.

Key point #4:

Screening testing can eliminate infant mortality failures and some potential reliability failures. Screening testing defined in MIL-PRF-38535 and in this document or its equivalent should be performed on all EEPROMs.

Key point #5:

No matter how effective it is, NO screening testing can guarantee that the EEPROMs have zero failures in applications. Therefore, redundancy at different levels, i.e., bit and/or page and/or image, needs to be used in space application for risk mitigation of the EEPROMs.

2.3 Process-Induced Weak Cells Modeled by Poisson Distribution

The endurance and data retention characteristics are for intrinsic chips and cells and so cannot project the lifetime or failure rate for weak cells. However, weak cells determine the MNOS EEPROM chip reliability simply because they fail before intrinsic cells.

Since weak cells can be induced by any random process or programming factors, we assume that the weak bit failures are randomly distributed. Therefore, Poisson distribution is used to describe the EEPROM weak bit failure statistics and to calculate the MNOS EEPROM weak bit failure rates.

When the number of bit failures follows Poisson distribution, then the probability of x number of bit failures is

$$P(X = x) = \frac{(\lambda t)^x e^{-\lambda t}}{x!} \qquad (1)$$

Where λ is the bit failures per hour and t is the total time (in the unit of hour) of interest. $P(X=0)$, $P(X=1)$, $P(X=2)$, … … $P(X=n)$, gives the probability of having one, two, three or n bit failures up to time t.

The bit failure rate λ is estimated based on the bit population and failures. JPL has used the MNOS EEPROM bit information on JPL missions currently in flight to estimate the bit failure rate for weak bits and has performed this mission success probability assessment on missions including TES, DI and DAWN.

Key point #6:

Weak cell failure rate needs to be estimated for each mission.

2.3.1 Impact of image redundancy

Image redundancy also has a big impact on improving overall mission reliability from the perspective of the MNOS EEPROM. Again, assuming that equation gives a 90% reliability for one image, then a mission reliability will be 90% for no image redundancy, 99% for redundancy

of two images with only one needed to achieve mission objectives, 99.9% for redundancy of three images with only one needed to achieve mission objectives, 97.2% for redundancy of three images with two needed to achieve mission objectives, 99.63% for redundancy of four images with two needed to achieve mission objectives. This indicates that the image redundancy will greatly improve the system/mission reliability.

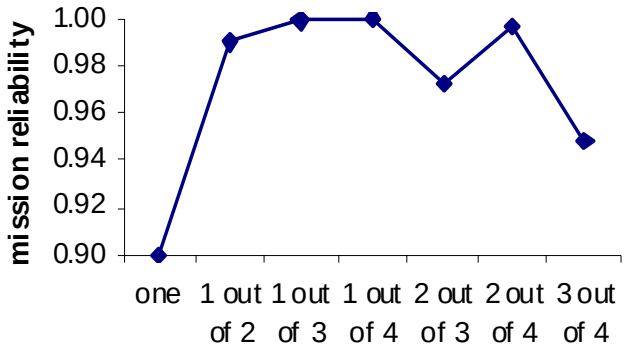

Figure 5. Impact of image redundancy on mission overall reliability.

Section III. Mission Experiences of MNOS EEPROM

3.1 JPL Mission Experiences and Investigations

This section summarizes JPL's mission experiences and investigations of the commercial MNOS EEPROMs. The total number of MNOS EEPROMs in service in the following JPL spacecraft is estimated to be 240: MCO, MPL, Stardust, Mars Odyssey, GALEX, SIRTF, Genesis, and MER. MER uses the RAD6000 single board computer of which these EEPROM are an integral component. Of these spacecraft only Genesis was affected by single bit failures in flight. There were a couple of single bit failures and page failures observed for MER and DI on the ground. The following sub-sections give a more detailed description of these failures, a summary of the investigations performed and the investigation results.

3.1.1 Genesis

The Genesis mission observed two single bit errors within one year of its flight operation. The Genesis operations team observed the first bit failure approximately six months into the mission and the second bit failure approximately seven months later. Genesis performs daily memory Cyclic Redundancy Check (CRC) verification.

There are three 8Mb MNOS EEPROM MCM U25, U32 and U38 on the RAD6000 card and two redundant RAD6000 cards in the Genesis computer and data handling (C&DH)

subsystem. The boot code is located in those EEPROMs that exhibited the errors. The Genesis operations team down-linked a complete memory dump of the A Side EEPROM contents and isolated the error to a single bit in the device in U25 board location, which is the first Megabyte of EEPROM memory. The contents 0ec0d0d9 at location 00a6f0c were observed to change to 0ec0d0f9. In other words the 6th least significant bit changed from a "0" to a "1" (i.e., from a charged state to a discharged state) in this 32 bit word. The corrupted memory contents were then loaded into the Genesis Software Test Lab (STL) and simulated. The corrupted code, when executed, would not enable a system reboot. The Software Engineers at Lockheed-Martin Aeronautics Company (LMA) mitigated the problem with a software patch. Basically, the normal download would occur then another download would overwrite the possibly corrupted information before any other action in the reboot process. A CRC value was established for the corrupted EEPROM contents as well as for the existing correct EEPROM content. This made it possible to monitor the situation to determine which state the bit was in as well as to detect any additional EEPROM errors while restoring the ability to reboot Side A with two acceptable CRC values and no change to Side B. The CRC values are on board for the two possible states of the most recently failed bit. This first bit failure stabilized in the failed state and both of the currently acceptable CRCs depend on it staying in that state.

Seven months after the patch was uploaded occasional CRC errors were detected again and for a different bit. This second bit failure was an undesired change from a "0" to "1". The location was in the same physical MCM package (U25) but on a different die at address 003b2d0. The contents changed from c0241095 to c02c1095 (20th least significant bit changing from "0" to "1"). This time it was found that the system would reboot with the corrupted code, however, the same type of patch strategy was applied to this second occurrence of the problem. The new software patch was up-linked and no further bit failures have been observed since (7 months since the new software load). At this point the original failed bit is steady in the “1” state and the two acceptable CRC values deal with the two possible states of the second failed bit. The return of the original failed bit to the zero state would be viewed as a new failure by the CRC check.

3.1.2 Mars Exploration Rover

There were two parts with page failures observed on Mars Exploration Rover (MER), one part was used in the non-volatile memory board (NVM_CAM) breadboard and the other was on the RAD6000 computer board.

3.1.2.1. EEPROM page failure #1

On December 5, 2002, the MER project reported one page failure of EEPROMs on the camera NVM_CAM on their breadboard during system test. The breadboard experienced many Reset commands during power on and so may have accidentally erased the EEPROM many times. The device went through numerous write cycles, but they were not recorded. The Cognizant Engineer suspected that this page failure could be a wear-out phenomenon. When the part was taken off the breadboard for troubleshooting, the Cognizant Engineer could not duplicate the failure until he tried the following sequence.

a. Write all "1", i.e., erase all cells.
b. Then write all "0", i.e., write all cells; or write a 33 or AA pattern.
c. Read.

The number of read cycles to observe the first failure is random using the above testing sequence.

3.1.2.2. EEPROM page failure #2

On March 1st, the MER project reported two distinct errors in PFR # 79647 [1] during their pre-launch testing and one of the errors turned out to be EEPROM page failure. The page failure is described in detail in PFR # Z79906 [2], showing that there were numerous fluctuating errors that were all confined to a single page of a single device. The values continued to fluctuate for over an hour after being written, and were still fluctuating when the testing was stopped.

The checksum recorded in block 5 of the primary SEQ file system changed over time, which appears to be an intermittent failure of the EEPROM device corresponding to the low-order byte of the lower part of the address space on the CPU board. Blocks are numbered starting at 0, and are 288 bytes long, i.e. 256 bytes of data, plus a 4-byte checksum and 4-byte padding. A page has 512 bytes. Block 5 starts before the faulty EEPROM page and ends in the middle of it. This means that block 6 and 7 still have bits from the faulty page since block 6 doesn't quite fill out the balance of the faulty page. Block 8 is entirely within the following page, and so should not contain any bits in the faulty page. The faulty device was not removed from the spacecraft; the start of the primary SEQ file system was moved to the following page, past the bad page of the EEPROM.

3.1.2.3. EEPROM single bit failure

On December 5, 2002, the MER project reported one single bit failure of EEPROMs on the camera NVM_CAM on their breadboard during system test. The EEPROM bit failure seemed to be a pattern sensitive problem. The exact S/W code was used to duplicate the failure. The expected pattern at location 0x0AD97 was 0x45, however the observed pattern, indicating a possible failure was 0x4d. The bit failure locations reported by the software engineers were from the same sub-page, 0x0AD91, 0x0AD96, 0x0AD97. The Cognizant Engineer was only able to verify the error at the last location.

3.1.3 Deep Impact

On October 31, 2002, Ball Aerospace reported a possible bit failure of one of the EEPROMs on the Flight Instrument Controller board SN0002 for Deep Impact. After the board had passed all the board-level test procedures, which included a full EEPROM test, the Flight code was then programmed into the EEPROM. During this procedure, there were no failures indicated either from the CRC after programming or subsequently when the board was booted up after the software installation. This board was then put on the shelf for several days before being integrated with the High Resolution Imager (HRI) Instrument Electronics box. During the

Integration test on the HRI box, it was discovered that the CRC of the primary EEPROM bank didn't match the expected value. This prevented the boot up from this bank.

Further investigation revealed a particular memory location that had a “1” in it instead of the “0” that had been written during the Flight code installation. The failure started out as a single location that apparently was failed, but as time went on, it seemed to be in an address region rather than a single location. The address region is 0x0C4C8 to 0x0C4E8. Previous to writing the Flight software image into the EEPROM banks, the Cognizant Engineer of the HRI performed a board-level EEPROM test that wrote 0xAAAAAAAA to every location, followed by a read of the entire array for verification, followed by a write of 0x55555555 to every location followed again by a verification read. This test passed at the time it was run. Subsequently, the Flight software was programmed into EEPROM, followed by a CRC check that passed at the time. After about 2 days of sitting on the shelf un-powered at room temperature, the board was again installed into the chassis and functional tests were performed. It was at this time that a CRC failure was discovered. Troubleshooting revealed the location where they first discovered what should have been a zero was now a one. Further troubleshooting a day or two later revealed this CRC failure occurred whenever attempting to read the previously described region. This problem only seemed to occur when reading in sequence a group of locations. While trying to pin down the problem in the lab, a different failure mode was observed, where the TSC695 micro controller on the Instrument Controller board went into the exception reset condition, with the reason for reset being traced to an internal parity error on the EEPROM read. This failure occurred when attempting to read from the memory area where the original problem was identified.

More investigation resulted in pinning down the exact reason why the TSC695 went into the exception reset condition while reading from this EEPROM. When the failure occurs, it can be seen that the data coming out from the EEPROM is not stable during the read cycle as it needs to be for the TSC695 to latch the data internally. A "good" read from a nearby EEPROM location is shown in figure 2 to illustrate what the read cycle should look like.

The presumed defective EEPROM chip on the Instrument Controller board SN0002 was sent to failure analysis to determine the exact reason for this failure. The chip in question is U5.

3.1.4 EEPROM failure investigation summary

3.1.4.1 Single bit failures

- Two single bit failures observed on Genesis within one year of its flight operation.
- One single bit failure observed on MER NVM_CAM breadboard
- One single bit failure observed on DI Flight Instrument Controller SN0002

Investigation:
Without re-writing to the failed bits on Genesis, JPL has performed the diagnostic testing on both the MER and DI single bit failure parts, but could not verify the single bit failures on

either of the two parts with Advantest and PCI interface board. Both parts passed read-after-write testing.

Conclusion:
This suggested that the parts are functional in the benchmarked timing regime and that the single bit failures may be related to board level programming timing and/or noise margins.

Lesson learned #1:

While intrinsic EEPROM cells can have 10-year retention time at 70ºC, weak cells can fail any time before the guaranteed 10-year retention life.

Lesson learned #2:

Risk mitigation should be at both parts level and system/design level. Hardware and software designs should be considered at the system level to avoid negative impacts to EEPROMs.

Lesson learned #3:

Risk can be mitigated by utilizing CRC computations to monitor bit errors and trigger software reloads.

3.1.4.2 Page failures

- One page failure observed on MER NVM_CAM breadboard (MER breadboard part)
- One page failure observed on MER RAD6000 pre-launch (MER R6K part)

Investigation:
a. The MER R6K part was previously un-used until the pre-launch testing, when a page failure was observed.
b. The MER breadboard page failure part went through the following test steps:

1 Verified page failure on Advantest and PCI interface board
2 Failure analysis under EMMI and a "glow" was observed
3 Baked at 150ºC for 24 hours
4 No read-after-write errors at -30ºC, 27ºC, 70ºC and 80ºC
5 "Glow" under EMMI remained

Conclusion:
1. We believe that the page failure on MER R6K part is possibly due to infant mortality. Any inappropriate handling of the part may also be a cause of the failure.

2. The MER breadboard part went through numerous write cycles and reset during power on and therefore wear-out could be a possible cause.

Lesson learned #4:

EEPROMs need to be screened and properly handled.

Lesson learned #5:

Write/erase cycles are consumable; Keep a record of write cycles performed on the parts to aid in reliability analyses of parts being considered for flight or aid in failure analysis.

3.2 GSFC Mission Experiences and Advisory

3.2.1 Mission experiences

3.2.1.1 Success

EO-1 used the NMOS EEPROM devices packaged from SEI (now Maxwell Technologies). They were the single die devices, 128Kx8. Almost every subsystem contained at least one device. There were no problems experienced.

GLAS (instrument on SWIFT) also used the NMOS EEPROM devices from Maxwell Technology. Instrument subsystems used both single die devices, as well as the larger 4-die (512kx8) modules. There were no problems experienced.

3.2.1.2 Single bit failures

SWIFT BAT used the MNOS EEPROM devices packaged by Austin Semiconductor. They were built for use on the RAD6000 computer boards, as well as the other Instrument Processor subsystems. In addition, the UVOT electronics contained both a Maxwell single die device and a 4-die module, both from Maxwell Technologies.

The UVOT breadboard device (single die) did experience a failure, which was diagnosed as a failing bit, but only after many years of operation and "less-than-optimum" handling. This breadboard was used as a test bed, as well as a breadboard development unit, so handling and other issues were considered to have been the cause of the failure. There were no problems with any of the flight units, for any of the subsystems.

The EEPROM devices used in the New Millennium Program Space Technology –5 (ST-5) are two 8-1Mbit-128Kx8-die MCM modules (256kx32), each packaged in a 96-pin RAD-PAK Quad Flat package from Maxwell Technologies. The EEPROM modules were used for each flight C&DH to hold boot and flight code for Mongoose 5 processor. Breadboards used

Atmel commercial equivalent parts. There were no problems during development, but a failed bit was found on spacecraft unit #1 during ground testing when different EEPROM checksums were recorded before and after Thanksgiving 2003. Examination of the failure by the C&DH team found that a design change in the controlling FPGA caused the write timing to be non-compliant with the EEPROM datasheet data hold specification. The FPGA code was corrected, the part was replaced, and there have been no EEPROM anomalies on this mission.

Repeat of Lesson learned #3:

Risk mitigation should be at both parts level and system/design level. Hardware and software designs should be considered at the system level to avoid negative impacts to EEPROMs.

3.2.2 Advisory

The Applied Engineering and Technology Directorate of GSFC has generated NASA-Wide Advisory NA-GSFC-2005-04 providing recommendations to present and future programs on strategies to retire, or as a minimum mitigate, the risk of the EEPROM data retention failure as a mission failure possibility. The Advisory recommends limiting the EEPROM use to non-critical code applications only and establishing the ability to effectively and safely detect an EEPROM bit error in such a way to allow the system to continue operating, in a predictable manner, from an alternate memory source while the error is corrected either from the software code or the ground. All mission-critical software functions, including boot code capable of performing such basic functions as executable code memory checking, basic command and telemetry capabilities to load and dump memory contents and safe-hold mode, be stored in PROM or other similar permanent storage technology. The Advisory recommends that each program be assessed individually to determine its susceptibility to EEPROM failures, the level of risk to the project associated with an EEPROM failure and the acceptability of that level of risk. Risk mitigation strategies are provided by the Advisory from the system architecture, component level and system level test.

3.3 EEPROM Mission Experiences by Other Agencies

3.3.1 Agency 1

Agency 1 has performed a reliability analysis on the commercial MNOS EEPROMs based on life tests on a total of 111 parts at temperatures of 175ºC, 200ºC, 225ºC and 250ºC. Radiation testing was also done on some of the aged parts.

Agency 1 believes that data retention activation energy is in the range of 0.9 to 1.1 eV and states that all their devices under testing have demonstrated greater than 10 years at 70ºC upon projection. But, Agency 1 also claims that there is a likelihood of having a sub-population of early failures within the total population, likely to represent no more than 1-in-15 to 1-in-30 devices. Intermittent data retention behavior was observed during the testing, but the cause of

this behavior is not understood. A screening procedure was developed to weed out the potential early-failure parts, but Agency 1 does not guarantee that the screening procedure will successfully remove all infant mortality parts.

Radiation hardness evaluation test was also performed on the parts, using a total dose of 78 krad in an unbiased condition. This total dose was 50% above the requirement for survival and all parts showed only minor changes in the data retention performance, access time and electrical performance characteristics, prior to and after radiation testing. Accelerated temperature evaluation of the parts was then re-done after irradiation. The measured changes in the electrical properties after 160 hours and 200ºC was found to be the same as similarly aged parts without radiation exposure. Thus, Agency 1 has concluded that the long-term effect of radiation on the unbiased parts has been demonstrated to be small.

3.3.2 Agency 2

A programming failure was found on an EEPROM device. One bit of one address of an EEPROM device was found unable to program at temperature at –25ºC during board test in June 2005. Seven EEPROM parts from the same lot were then tested over the temperature of –55ºC and 60ºC and no failure was observed. One of the seven EEPROMs was used to replace the failed part. Further analysis found that the temperature threshold of the program failure was -10ºC. The part worked fine above -10ºC and extra numbers of write cycles were needed to program the failed bit. The bit needed two write cycles at the temperature of -10ºC to -25ºC and three write cycles at the temperature of -25ºC to -55ºC.

Lesson learned #6:

EEPROMs need to be functionally tested over full operating temperatures, i.e. -55ºC to 70ºC.

3.3.3 Agency 3

Agency 3 has not had EEPROM failure on their RAD750 computer board, but encountered problems related to intermittent readout on two EEPROMs during lab testing and one EEPROM during thermal vacuum (TVAC) testing. The first EEPROM had intermittent readout issue with all bits. Failure analysis was performed. The part failed the gross leak test. Seal leaks and corroded leads were found. Chlorine contamination inside of the part was determined as the root cause of failure. The intermittent readout issues with the second and third EEPROMs were isolated to one page of the parts. Further investigation was performed on these second and third parts by re-programming and no failures were observed. One of the resulting recommendations from this Agency is to ensure that CS* is asserted sufficiently long enough before OE* is asserted so that no glitches are present on the data output pins when the outputs are switching and the EEPROM is enabled.

Lesson learned #7:

CS* needs to be asserted sufficiently long enough before OE* is asserted to avoid glitches on the data.

3.3.4 Agency 4

Agency 4 characterized the noise sensitivity on the EEPROMs. Twelve (12) EEPROMs were used in this study and all the EEPROMs were locked by the software protection algorithm during the characterization testing. No generalized conclusion was drawn in terms of noise impact on the EEPROMs as function of write strobe frequency or write strobe pulses. No indication of sensitivity to disturbances on the reset signal was observed. However, it was found that the EEPROMs were sensitive to perturbations on the write strobe, and since the internal noise filter in the EEPROM can filter out noise less than 20ns, short pulses of about 12ns on the write strobe at the end of write cycle could pass the internal filter and affect the EEPROMs undesirably. When buffers are used for driving EEPROM control signals, the output of the buffers may start to oscillate if the input signals to the buffers are left floating at any time. For unlocked EEPROMs, violating 10 ms delay when writing to the EEPROM and crossing a page boundary may result in sub page corruption; violating the byte load window timing requirement may affect the page which was written. For locked EEPROMs, *WR_N* cannot be below 100ns.

Lesson learned #8:

EEPROMs need clean and noiseless control signal.

Lesson learned #9:

Avoid floating signals as input to buffers driving EEPROMs.

Lesson learned #10:

EEPROMs are affected by a write access and will be unavailable for 10 ms even if the Software Data Protection is enabled.

Lesson learned #11:

Lock EEPROMs. All timing needs to meet the requirements in data sheet.

3.3.5 Agency 5

Agency 5 observed a page failure on one EEPROM in July 2004. Memory loss was located to a single page of the EEPROM die within a MCM package. Unlike the intermittent page failures previously observed at JPL and Agency 1, the page failure can be re-created and

repeated shortly after writing to the page. Agency 4 believes that their EEPROM part is one example of an EEPROM device with consistent single page failure while JPL and Agency 1 devices exhibited intermittent page write failures with longer time to fail characteristics.

3.3.6 Agency 6

Agency 6 observed bit failures on EEPROMs in RAD750s. Further investigation indicated that the bit failures may be related to at-speed timing. On request, additional data retention screening can be performed, which consists of the following steps: 1) program EEPRMs to "0"s with SW write protect off; 2) verify "0"s at speed timing; 3) burn-in for 72 hours at 150ºC; 4) verify "0"s at speed.

Lesson learned #12:

Request that data verification be performed at speed after data retention screening test.

3.4 Summary of Lessons Learned

The following table summarizes all the missions and MNOS EEPROM bit/page failures we have discussed in this section, along with lessons learned:

Mission/Agency	Failure	Lessons Learned
Genesis	Single bit failures	• Weak cells can fail any time before the guaranteed 10-year retention time. • Risk can be mitigated by utilizing CRC computations to monitor bit errors and trigger software reloads
Deep Impact	Single bit failure	• Risk mitigation should be at both parts level and system/design level. • Hardware and software designs should be considered at the system level to avoid negative impacts to EEPROMs.
MER	Single bit failure	• Risk mitigation should be at both parts level and system/design level. • Hardware and software designs should be considered at the system level to avoid negative impacts to EEPROMs.

	Page failure	• EEPROMs need to be screened and properly handled. • Write/erase cycles are consumable; keep a record of write/erase cycles performed on the EEPROMs to aid in reliability analysis.
ST-5	Single bit failure	• Risk mitigation should be at both parts level and system/design level. • Hardware and software designs should be considered at the system level to avoid negative impacts to EEPROMs.
Agency 2	Single bit program failure	• EEPROMs need to be functionally tested over full operating temperatures, i.e., -55ºC to 70ºC.
Agency 3	Intermittent readout	• CS* needs to be asserted sufficiently long enough before OE* is asserted to avoid glitches on the data.
Agency 4	Noise	• EEPROMs need clean and noiseless control signal. • Avoid floating signals as input to buffers diving EEPROMs. • EEPROMs are affected by a write access and will be unavailable for 10 ms even if the Software Data Protection is enabled. • Lock EEPROMs. All timing needs to meet the requirements in data sheet.
Agency 6	Single bit failures	• Request that data verification be performed at speed after data retention screening test.

Section VI. Risk Mitigation and Recommendations

Based on our EEPROM weak cell analysis and all the lessons learned, the following analysis and practice are strongly recommended to ensure the reliability of the MNOS EEPROMs in space applications:

1. Key points are:
    a. EEPROM reliability concerns come from weak cells, which can be induced by either processes or users.
    b. The best practice of avoiding the process defect induced weak cells is to perform effective screening on the EEPROMs.

c. The best practice of avoiding the programming induced weak cells is to understand the EEPROM device and make sure that all worst case timing meets the requirements in the data sheet.
d. Screening testing can eliminate infant mortality failures and some potential reliability failures. Screening testing defined in MIL-PRF-38535 and in this document (Section II) or its equivalent should be performed on all EEPROMs.
e. No matter how effective it is, NO screening testing can guarantee that the EEPROMs have zero failures in applications. Therefore, redundancy at different levels, i.e. bit and/or page and/or image, needs to be used in space applications for risk mitigation of the EEPROMs.
f. Weak cell failure rate needs to be estimated for each mission.
g. Risk mitigation needs to be in both parts and system/design levels.

2. Parts level:
   h. Use the parts per the specification on operating voltage and timing.
   i. Make sure the parts have gone through pre-screening and been characterized at full temperature, i.e. –55ºC to 70ºC.
   j. If the parts are already stored on board and you are not sure of the testing history of the parts, the following procedures need to be performed on the parts for detecting possible weak bits:
      i. Program with a checkerboard pattern and read a couple of thousand times;
      ii. Program with the inverse checkerboard pattern and read a couple of thousand times.
3. System and design level:
   k. Use EDAC code.
   l. Use redundancy in image/code.
   m. Design in bit and page redundancy to allow for programming around failed bit or pages.
   n. Perform worst-case timing analysis in board level to make sure that the timing meets the manufacturer's specification with necessary margin.
      i. Assert RES* on power up and power down to avoid data corruption.
      ii. RES* asserted too early could corrupt write. Since the reset protect time t_{RP} (starts when RES*=V_H=V_{CC}–0.5V) is 100 μs minimum, do not write until 100 μs after power-up.
      iii. During power-up, RES* needs to be less than V_{IL}=0.8V before V_{CC}=1V and asserted until V_{CC}> V_{CCmin}.
      iv. During power-down, RES* needs to be less than V_{IL}=0.8V before V_{CC}< V_{CCmin} and asserted until V_{CC}<1V.
      v. Power-up sequence: RES/low, V_{CC} on, RES/high 1μs after V_{CC}=4.5V, wait 100μs, WE/low.
      vi. Power-down sequence: Last write complete, RES/low, wait 1μs, V_{CC} off.
   o. Minimize crosstalk and signal/V_{CC} noise.
      i. Be careful not to allow noise of a width of more than 20ns on the control pins.
      ii. CS* needs to be asserted sufficiently long enough before OE* is asserted to avoid glitches on the data.
   p. Minimize the number of write/erase cycles during ground and pre-launch testing.

i. Keep a record of number of write/erase cycles on the parts.

4. The operating temperature (or ambient temperature, back of die temperature) cannot be over 70ºC.
5. If the mission life is over 10 years, additional analysis is needed.

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