National Aeronautics and Space Administration

IR DirectFET Extreme Environments Evaluation Final Report

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NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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Abstract

In 2007, International Rectifier (IR) introduced a new version of its DirectFET metal oxide semiconductor field effect transistor (MOSFET) packaging. The new version (referred to as "Version 2") enhances device moisture resistance, makes surface mount (SMT) assembly of these devices to printed wiring boards (PWBs) more repeatable, and subsequent assembly inspection simpler. In the present study, the National Aeronautics Space Administration (NASA) Jet Propulsion Laboratory (JPL), in collaboration with Stellar Microelectronics (Stellar), continued an evaluation of the DirectFET that they started together in 2006. The present study focused on comparing the two versions of the DirectFET and examining the suitability of the DirectFET devices for space applications.

This study evaluated both versions of two DirectFET packaged devices that had both been shown in the 2006 study to have the best electrical and thermal properties: the IRF6635 and IRF6644. The present study evaluated (1) the relative electrical and thermal performance of both versions of each device, (2) the performance through high reliability testing, and (3) the performance of these devices in combination with a range of alternate solder alloys in the extreme thermal environments of deep space.

Both versions of the IRF6635 and IRF6644 devices exhibited nearly equivalent electrical and thermal performance. Both versions of IRF6644 had identical RdsOn values while the IRF6635 Version 2 had RdsOn values up to 45 percent lower than Version 1. The thermal resistances of both versions of IRF6635 and IRF6644 were essentially equivalent. The IRF6635 devices appeared to have 50 percent lower resistance junction to lead (Rj-l) than the IRF6644 devices. The addition of finned heat sink reduced thermal resistances (both Rj-a and Rj-l) of both versions of IRF6644 by 15 percent. The finned heat sink reduced the Rj-a of both versions of IRF6635 also by 15 percent but Rj-l was reduced by 28 percent. The cause of the larger reduction IRF6635 Rj-l is unknown.

Both versions of each device performed well through temperature cycling (100 Cycles, -65°C to +150°C). No electrical failures were observed. A general reduction of up to 3 percent in RdsOn on all devices was observed after temperature cycling. All other device parameters remained unchanged.

Both versions of IRF6635 experienced leakage current failures after approximately 325 hours of Temperature-Humidity-Bias Testing (85% Rel. Humidity/85°C/24V Bias). The failures were all attributed to moisture condensation on the devices and subsequent migration of silver particles from the silver epoxy die attach that shorted drain-to-source or source-to-gate leads. The destructive effects of humidity can be avoided by conformal coating or underfilling the DirectFET devices, thereby preventing silver migration and protecting the die as well.

Both versions of each device soldered with lead-tin eutectic solder alloy (Sn63:Pb37) were subjected to 100 temperature cycles between -120°C and +115°C (Mars thermal environment) followed by 100 temperature cycles between -180°C and +85°C (Deep Space thermal environment). The DirectFET devices with pre-tinned pads (pre-tin with Sn76.5:Ag3.0:Cu0.5 [SAC305]), regardless of which version or device type, passed electrical testing after the extreme temperature cycling testing with only a single failure. Only relatively minor shifts of up to 5 percent were observed in RdsOn measurements. All other device parameters appeared unchanged. The IRF6635 Version 1 devices, which did not have pre-tinned pads, began to fail test after only 50 cycles in the Mars thermal environment. However, cross-sectional analysis of "good" electrical units, which passed all the temperature cycling, showed clear evidence of fatigue crack formation. The fatigue cracks were all in the solder joint adjacent to the die pads and in many cases traversed the entire length of the solder joint. Consequently, the authors conclude that electrical test data cannot be solely relied upon in assessing assembly reliability.

Both versions of each device were also soldered with tin-indium-silver (Sn77.2:In20:Ag2.8) and lead-indium (60Pb:In40) solder alloys. These test devices were tested side by side with the lead-tin eutectic soldered parts and subjected to the same extreme temperature cycles and electrical tests.The tin-indium silver parts with pre-tinned pads regardless of which version or device type, passed electrical testing after the extreme temperature cycling testing with only a single failure. The lead-indium IRF6644 Version

1 parts had a larger proportion of electrical failures. All lead-indium Version 2 parts passed all electrical and temperature cycle testing. Cross-sectional analysis of electrically good tin-indium-silver parts showed that the solder joints had largely de-bonded from the PWB solder pads. This was observed on all cross-sectioned parts, regardless of device type or version. Cross-sectional analysis of electrically good lead-indium parts showed substantial creep deformation of solder joints regardless of device type or version. Consequently, as with the lead-tin soldered parts, while the assemblies passed electrical testing, their solder joints were mechanically compromised and constitute failures.

1.0 Introduction

1.1 Summary of Previous Work

In 2006, the Jet Propulsion Laboratory (JPL) and Stellar Microelectronics (Stellar) with the support of NASA Electronics Packaging Program (NEPP) and International Rectifier (IR) conducted a joint study to evaluate the performance of IR's DirectFET metal oxide semiconductor field effect transistor (MOSFET) packaging in comparison with SO-8 and Toshiba High Efficiency packaging [1]. That study concluded that the DirectFET packaging offered substantially reduced thermal and electrical resistance over conventional packaging. Additionally, the DirectFET packaging exhibited comparable reliability when subjected to environmental testing.

1.2 DirectFET Packaging Version 2

In late 2006, IR began pre-production of a new version (referred to hereafter as "Version 2") of the DirectFET packaging. IR made a number of significant changes to the die and the packaging. Figure 1 illustrates the key differences between Version 2 and the original DirectFET packaging (referred hereafter as "Version 1").

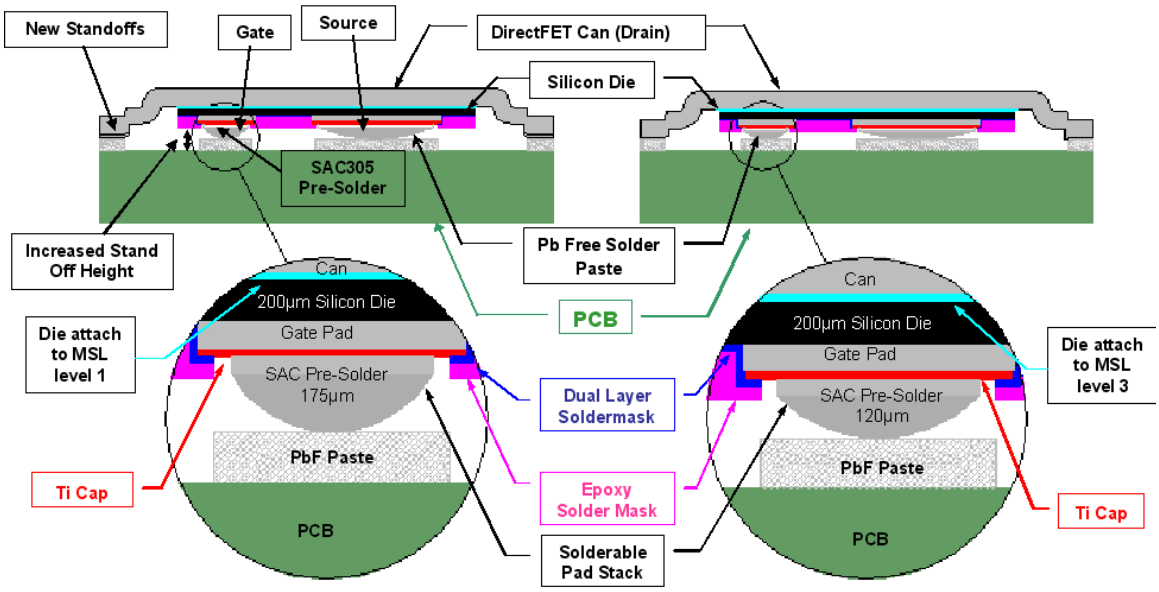


Figure 1. DirectFET Packaging: Version 1 versus Version 2*

These design changes are summarized as follows:

- Addition of four stand-offs to the drain pads to ensure consistent placement height above the printed wiring board (PWB) and consistent solder column thickness of the source and gate leads.

* Illustration courtesy of International Rectifier, Inc.

- Increased solder bump height increases the gap underneath the parts when mounted on the PWBs. The increased gap makes it easier to inspect the source and gate solder joints. It also increases the solder volume of these joints, which should improve assembly reliability.

- The addition of the Ti metal layer "cap" underneath the source and drain solder pads improves the moisture resistance of the device, bringing it from a Moisture Sensitivity Level (MSL) 3 to MSL 1, per J-STD-020.

1.3 Objectives of the Present Study

The present study continues where the previous study left off. The principal focus of the new work is the evaluation of the DirectFET packaging for use in space applications. The specific objectives of this study are fourfold:

a) To evaluate the relative electrical and thermal performance of the two versions of the DirectFET packaging.
b) To subject both versions to a sequence of high reliability qualification tests and demonstrate that the parts are suitable for high reliability applications.
c) To evaluate the reliability of the devices when subjected to the thermal extremes of the deep space environment.
d) To evaluate the reliability of alternative solder alloys to eutectic lead-tin.

1.4 Overview of Testing

In the 2006 study, the test results showed that the IRF6644 and IRF6635 DirectFET devices exhibited the best thermal and electrical performance. Consequently, the two versions of these devices were chosen as the test vehicles for this study. A series of the electrical, thermal, and environmental tests were designed to achieve the objectives outlined in Section 1.3 and are listed in Table 1.

1.4.1 Electrical and Thermal Comparison of DirectFET Versions 1 and 2

The electrical and thermal tests were the first to be performed. The intent of these tests was straightforward: perform a direct comparison of the electrical and thermal performance of Versions 1 and 2. Given that the design changes made in Version 2 were relatively minor, it was unlikely that there would be any significant differences between the two Versions of the devices. Yet, it was essential to establish baseline measurements against which the results from subsequent tests could be gauged.

1.4.2 High Reliability Evaluation of DirectFET

The intent of the tests in this evaluation was to determine whether both versions of the DirectFET parts could be qualified for high reliability applications. To this end, the parts were subjected to a reduced set of qualification tests: temperature cycle and moisture resistance. These are tests that high reliability parts must normally pass in qualifications.

Table 1. Test Matrix

Objective	Test	Test Description	Measured Parameters
Electrical/ thermal comparison: Version 1 vs. Version 2	Electrical	Measure device parameters of IRF6635 and IRF6644 Versions 1 and 2 per IR version 1 device specifications.	Device electrical parameters*: RdsOn, Idss, Vgs(th), BVdss, Igss, Vsd
	Thermal	Measure thermal resistance of IRF6635 and IRF6644 Versions 1 and 2per JEDEC JESD24-3	Thermal resistances: junction-to-air (Rj-a) junction-to-lead (Rj-l)
High reliability evaluation	Temperature cycle	24-hr. heat soak at 150°C followed by temperature cycling (-65°C to +150°C), 100 cycles per MIL-STD-883, Method 1010,Test Condition C	Electrical parameters: before and after temperature cycle
	Moisture resistance testing	Temperature-humidity-bias testing, 1000 hr., 85°C, 80% R. H., 0.0 A current, voltage drain-source bias per JEDEC J-STD-020	Electrical parameters: before and after test and at 250-hr. intervals during test. Monitor source-drain current during test.
Deep space thermal environment and alternate solder alloy evaluation	Deep space thermal Environment	Use temperature cycle samples from high reliability evaluation: 1. Perform Mars Environment Temperature Cycle†: -120°C to +115°C, 100 cycles; 2. Perform Deep Space Environment Temperature Cycle†:-180°C to +85°C, 100 cycles.	Electrical parameters: before and after tests and at 50-cycle intervals during tests.
	Alternate solder alloys	Evaluate the use of Indium solder alloys: Sn77.2:In20:Ag2.8 and Pb60:In40. Perform Deep Space thermal environment testing alongside lead-tin solder samples.	Electrical parameters: before and after tests and at 50-cycle intervals during tests.

* = Device electrical parameters acronyms: Static Drain-to-Source Resistance (RdsOn), Drain-to-Source Leakage Current (Idss), Gate Threshold Voltage (Vgs(th)), Drain-to-Source Breakdown Voltage (BVdss), Gate-to-Source Forward/Reverse Leakage Current (Igss), Body Diode Forward Voltage (Vsd)

† = Temperature Cycle Conditions: 5°C/min ramp-up and ramp-down rates, 45-minute dwell at high temperature and 10-minute dwell at low temperature.

1.4.3 Evaluation of DirectFET and Alternative Solder Alloys in Deep Space Environment

The cycling between temperature extremes that assemblies are subjected to in the deep space environment can lead to creep and fatigue failure of solder joints and other electronic assembly materials. Consequently, to protect the electronics from this extreme thermal environment (as well as from cosmic and space debris), they are kept within the confines of the spacecraft and their temperatures are regulated. However, this places significant limitations on spacecraft design as well as mission life. It is then of interest to determine whether electronic devices can perform reliably in the deep space thermal environment.

In this study, the reliability of the DirectFET packaged devices was evaluated in two space environments: the Mars thermal environment (-120°C to +115°C) and the Deep Space (Asteroid) thermal environment (-180°C to +85°C).

1.4.3.1 Alternative Solder Alloys

There are many solder alloys available that can offer better performance than conventional lead-tin eutectic solder. The alloys best suited to these extremes require an ability to absorb thermomechanical stresses if electronic devices are not to be damaged. Only lead or indium bearing alloys have this property.

Two indium solder alloys were selected for the study: 60Pb:40In and Sn77.2:In20:Ag2.8. The properties of these alloys as compared with lead-tin eutectic are listed in Table 2. Both these solder alloys were chosen in part because their liquidus points were within a few degrees of eutectic point of Sn63:Pb37. The two solders also represented two extremes of ductility as measured by their tensile modulus and strength: the 60Pb:40In is a very ductile alloy whereas the Sn77.2:In20:Ag2.8 is a rigid alloy, more rigid even than the lead-tin eutectic. Consequently, the alloys are likely to exhibit varying degrees of creep and fatigue resistance and differences in reliability.

Table 2. Solder Alloy Material Properties

Solder Alloy	Solidus / Liquidus (°C)	Density (g/cc)	CTE (ppm/°C)	Thermal Conductivity (W/mK)	Tensile Strength (psi)	Tensile Modulus (psi x 106)
Sn63:Pb37	183 / 183	8.40	25	50	7500	4.35
60Pb:40In	173 / 181	8.52	27	29	4150	1.94*
Sn77.2:In20:Ag2.8	175 / 187	7.25	28	54	6800	5.6

* = Modulus is for 50Pb:50In; the modulus of 60Pb:40In should be similar.

In this study, assemblies were built with the indium solder alloys and tested side by side with the lead-tin eutectic soldered parts.

2.0 DirectFET Version 1 versus Version 2 Comparison

2.1 Experimental

2.1.1 Electrical Testing

2.1.1.1 Devices and Test Assemblies

2.1.1.1.1 Test Devices

In the previous study, the test results showed that the IRF6644 and IRF6635 DirectFET devices exhibited the best thermal and electrical performance (shown in Figure 2). Consequently, these two devices were chosen for this study.

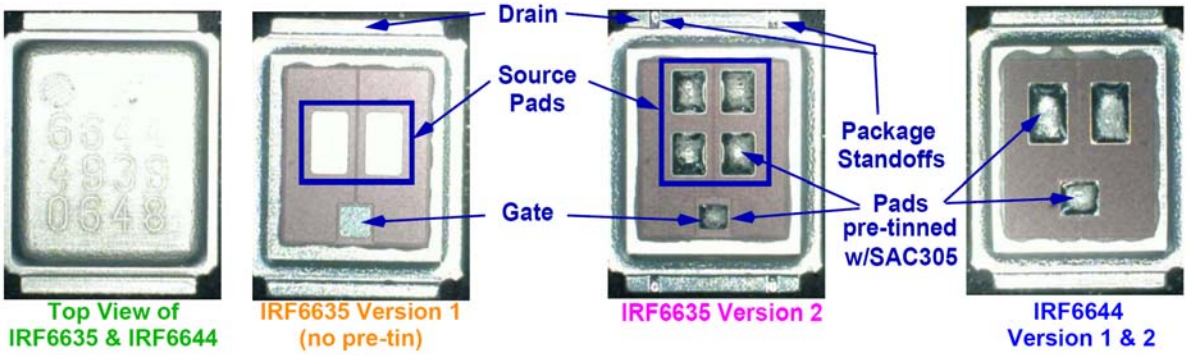


Figure 2. IRF6635 and IRF6644 Devices

The Version 2 devices of each device type were obtained from International Rectifier (IR) while the Version 1 devices were purchased by Stellar Microelectronics from Digi-Key. In addition to the differences between Version 1 and Version 2 devices outlined in Section 1.2, there are structural differences that are specific to the versions of each part type. These differences are described in Table 3 and are also indicated in Figure 2.

Table 3. Other Key Structural Differences between Test Devices

Feature	IRF6635		IRF6644	
	Version 1	Version 2	Version 1	Version 2
Source pads, geometry/configuration	Four small square pads	Two large rectangular pads	Pads have identical shape and size	
Pre-tinned source and gate pads	No Pre-tin	Pre-tin with Sn96.5:Ag3.0:Cu0.5 solder alloy (SAC305)	Pre-tin with Sn96.5:Ag3.0:Cu0.5 solder alloy (SAC305)	

Table 4 lists the electrical parameter specifications for the test devices. Version 1 and Version 2 devices of each device type should conform to the same electrical specifications.

Table 4. Device Electrical Parameters: Specification Limits

Measurement	IRF6635 Version 1 and 2	IRF6644 Version 1 and 2
Max. RdsOn 1 Static Drain-to-Source Resistance (mOhm)	1.8 *(Vgs= 10V; Id= 32A)*	13 *(Vgs= 10V; Id= 10.3A)*
Max. RdsOn 2 Static Drain-to-Source Resistance (mOhm)	2.4 *(Vgs= 4.5V; Id= 25A)*	*No requirement per IR device specification*
Max. Idss Drain-to-Source Leakage Current (nA)	1,000 *(Vds= 24V; Vgs= 0V)*	20,000 *(Vds= 100V; Vgs= 0V)*
Max. Vgs(th) Gate Threshold Voltage (Volt)	2.35 *(Vds=Vgs; Id=250µA)*	4.8 *(Vds=Vgs; Id=150µA)*
Min. BVdss Drain-to-Source Breakdown Voltage (Volt)	2.35 *(Vgs=0V; Id=250µA)*	100 *(Vgs=0V; Id=250µA)*
Max. Igss 1 Gate-to-Source Forward Leakage (nA)	100 *(Vgs= 20V)*	100 *(Vgs= 20V)*
Max. Igss 2 Gate-to-Source Reverse Leakage (nA)	-100 *(Vgs= -20V)*	-100 *(Vgs= -20V)*
Max. Vdsp Body Diode Forward Voltage (Volt)	-1.0 *(Is = 25A; Vgs = 0V)*	-1.3 *(Is = 6.2A; Vgs = 0V)*

Additionally, IR provided "dummy" DirectFET outline packages. In these dummy devices, the die is replaced with a copper slug. This device was used to baseline the contribution of the circuit board and device packaging to the measured electrical resistance of the circuit board assemblies.

2.1.1.1.2 Test PWB Assemblies

The devices were mounted onto three different circuit board designs shown in Figure 3. The board designs were obtained from IR and fabricated using standard epoxy FR-4 laminate materials and 0.5 oz. copper with electroless nickel immersion gold (ENIG) surface finish.

Figure 3. Electronic Test Circuit Boards

The test assemblies were fabricated using automated assembly equipment and lead-tin eutectic solder paste. The finished assemblies are depicted in Figure 4. X-ray inspection of the DirectFET assemblies revealed significant voiding in the source and gate solder joints and evidence of solder balls entrapped under the devices (see Figure 6). This suggests that the solder reflow profile requires further optimization. However, with the exception of the electrical resistance, the voiding should have minimal effect on the measured device electrical parameters. The effect of

voiding on the measured resistance can be subtracted using the averaged data obtained from dummy DirectFET assemblies.

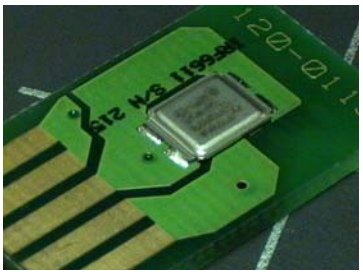


Figure 4. Electronic Test Assembly

2.1.1.2 Electrical Tests

Electrical testing was performed using an automatic Field-Effect Transistor (FET) Test system Model 9400. The system was programmed to measure all the electrical parameters of each device specified in Table 4 and using the test conditions outlined in the device specifications. The specifications were taken from the data sheets for the Version 1 IRF6635 and IRF6644 devices. According to IR, these specifications were also taken to be valid for Version 2 of these same devices.

2.1.2 Thermal Resistance Testing

2.1.2.1 Experimental

2.1.2.1.1 Devices and Test Assemblies

The thermal test board design shown in Figure 5 was obtained from IR and is the same board design used in the previous study. The boards were fabricated using standard epoxy FR-4 laminate materials and 0.5 oz. copper with ENIG surface finish.

The IRF6635 Version 2 and both versions of IRF6644 were surface mounted onto thermal test boards (see Figure 5). The IRF6635 Version 1 devices were not assembled onto boards, since these had already been tested in the previous study. The devices were only mounted on the medium copper pad configuration location, since the effect of copper surface area on thermal resistance had already been evaluated in the previous study.

Heat sinks (16-pin dual in-line package [DIP] finned heat sinks) were bonded on top of all the devices as shown in Figure 5 using Ablebond 84-1 LMINB-1 silver filled epoxy. These are the same heat sinks that were used in the previous study. Once the thermal resistance of the devices with heat sinks was measured, the heat sinks were removed and the resistance measured again. In this way, the effect of the heat sink on thermal resistance could be measured and the data compared to that obtained in the previous study.

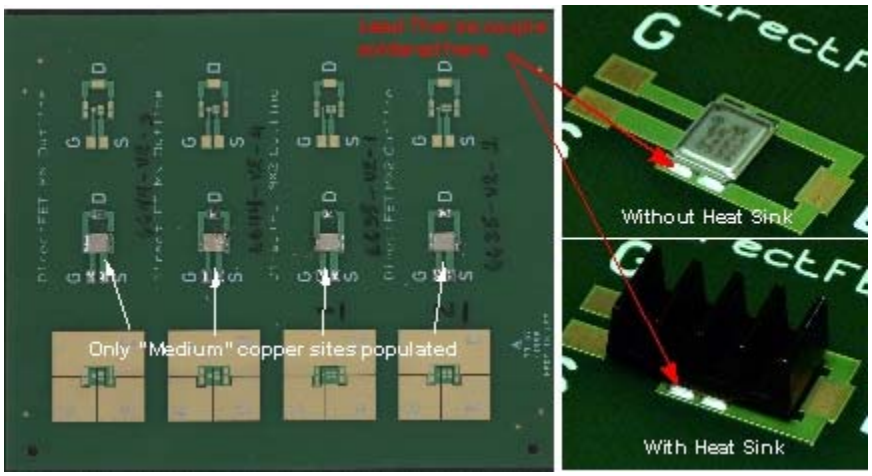


Figure 5. Thermal Resistance Board Assembly

2.1.2.1.2 Thermal Resistance Testing

The thermal resistance testing was performed by Analysis Tech (Wakefield, MA). Analysis Tech measured two thermal resistances for each device type: junction-to-ambient and junction-to-lead. The latter resistance used a thermocouple soldered to the DirectFET drain lead (see Figure 5) in order to obtain the junction-to-lead resistance. All measurements were carried out in still air at ambient (~25°C) temperatures.

An Analysis Tech Phase 11 Thermal Analyzer was used for all measurements. Measurements were performed according to the guidelines established in the JEDEC JESD24-3 standard. The metal oxide semiconductor field effect transistor (MOSFET) diode junction was used as the reference. Three devices for each device type were used for calibrating each device (K-Factor and intercept). The calibrations were carried out in a constant temperature bath.

2.2 Results and Discussion

2.2.1 Electrical Performance

2.2.1.1 General

The electrical test results, along with the specification maximum values, for each device type are presented in Table 5. The RdsOn value of the dummy DirectFET was measured using the IRF6635 and IRF6644 test conditions. The average value was 0.8 mOhms and 1.02 mOhms for IRF6635 and IRF6644, respectively. These values correspond to the contribution of the circuit board and solder joints to the RdsOn value of the assembly. These values were then subtracted from all the measured RdsOn values of all test assemblies.

A Cpk value was computed using the specification values and the measured RdsOn and Vth values. No Cpk was calculated for Ids, since in all cases the measured values were orders of magnitude below the specification maximum. The Cpk gives a measure of how well within specification the measured values are as well as the variance in the measured values from part to part. A Cpk value of 1 represents a 3-sigma part (i.e., there are three standard deviations between the specification maximum and the mean measured value) and a Cpk of 2 represents a 6-sigma

part. In general, the larger the Cpk, the more within specification and the more consistent the part measured values.

2.2.1.2 DirectFET Version 1 versus Version 2

All assemblies tested well within specification as is evident from the high Cpk values. Even the lowest values indicated a 6-sigma compliance to the device specifications.

Both versions of the IRF6635 and IRF6644 exhibited nearly identical electrical performance. The only significant difference was in the RdsOn values between Version 1 and Version 2 of IRF6635, where Version 2 had lower resistance values. The source pad configuration of Version 2 is different than Version 1 and this may have contributed to the measured differences. There were no differences in RdsOn between the two versions of IRF6644; the source pad configuration of both versions are identical.

Table 5. Electrical Test Results

Measurement	IRF6635*			IRF6644†		
	Version 1	Version 2	Spec. Req.	Version 1	Version 2	Spec. Req.
Max. RdsOn 1‡ (mOhm)	1.17 ± 0.374 *Cpk = 5.54*	0.829 ± 0.498 *Cpk = 6.50*	1.8	10.3 ± 0.384 *Cpk = 2.28*	10.4 ± 0.105 *Cpk = 8.14*	13
Max. RdsOn 2‡ (mOhm)	1.77 ± 0.362 *Cpk = 5.82*	1.45 ± 0.530 *Cpk = 5.96*	2.4	*Not Applicable*		
Max. Idss (nA)	5.44 ± 0.380	3.72 ± 0.505	1,000	5.50 ± 2.39	4.81±.415	20,000
Max. Vgs(th) (Volt)	1.78 ± 0.01 *Cpk = 26*	1.84 ± 0.022 *Cpk = 7.40*	2.35	3.79 ± 0.114 *Cpk = 2.96*	4.00 ± 0.070 *Cpk = 3.80*	4.8
Min. BVdss (Volt)	32.5 ± 0.2 *Cpk = 3.74*	33.3 ± 0.5 *Cpk = 2.19*	2.35	105 ± 0.006 *Cpk = 271*	105 ± 0.658 *Cpk = 2.45*	100
Max. Igss 1 (nA)	10.1 ± 10.8	4.24 ± 7.94	100	0.130 ± 0.212	0.0601 ± 0.0372	100
Max. Igss 2 (nA)	-30.0 ± 121	-1.53 ± 3.10	-100	-0.177 ± 0.264	-0.334 ± 0.440	-100
Max. Vdsp (Volt)	-0.778 ± 0.0011	-0.772 ± 0.0013	-1.0	-0.748 ± 0.0020	-0.750 ± 0.0020	-1.3

* = Sample quantity of IRF6635 Versions 1 and 2 for these tests was 30 each.

† = Sample quantity of IRF6644 Versions 1 and 2 for these tests was 25 each.

‡ = A constant of 1.02 mOhm, representing the resistance contribution from the circuit board and solder joints, was subtracted from all RdsOn measurements for all IRF6644 devices. A similar constant of 0.8 mOhm was subtracted from all RdsOn measurements for all IRF6635 devices.

2.2.2 Thermal Performance

2.2.2.1 DirectFET Version 1 versus Version 2

2.2.2.1.1 Thermal Resistance: Junction-to-Air (Rj-a)

The measured Rj-a resistance values of both versions of the IRF6635 and IRF6644 are displayed in Figure 6. The IRF6635 Version 1 data were obtained from the 2006 study. The junction-to-air resistance of both versions of these devices were essentially identical. The thermal resistances ranged between 38°C and 40°C/Watt. These numbers compare well against the data obtained for DirectFET devices in the 2006 study.

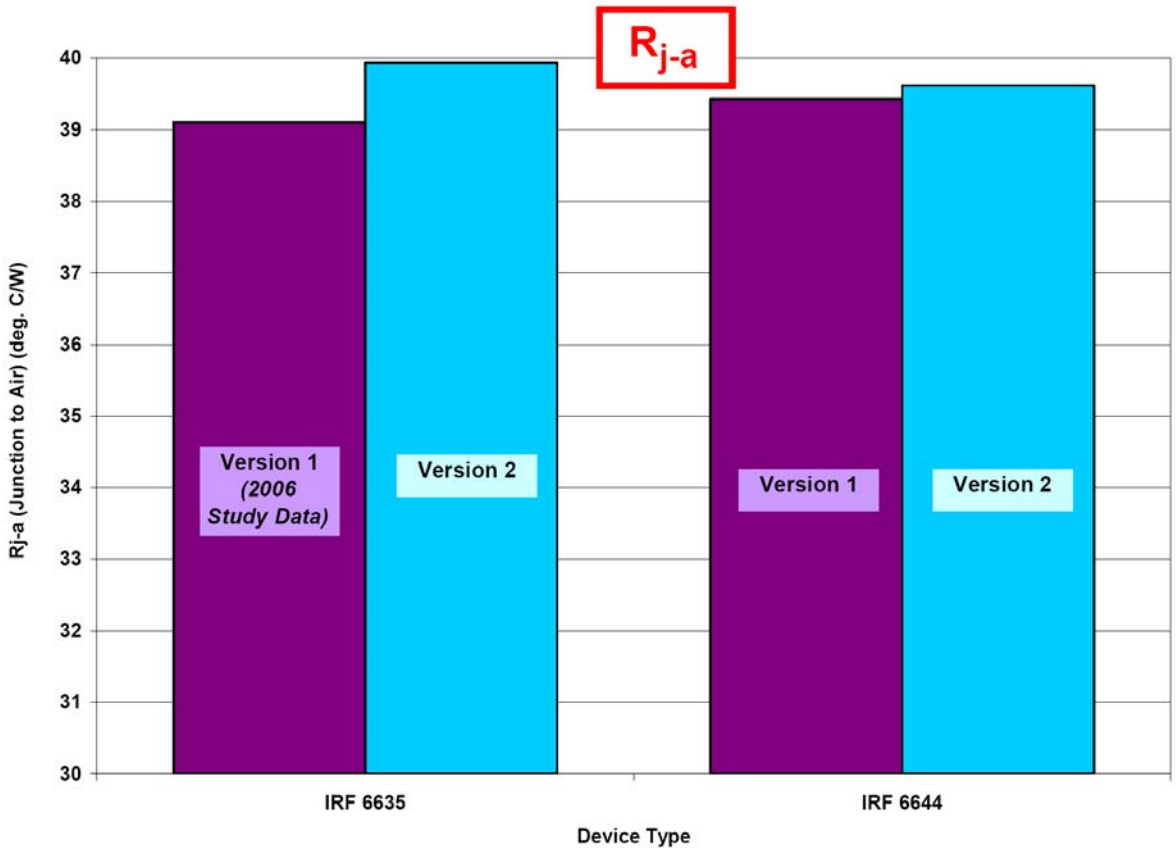


Figure 6. DirectFET Version 1 versus Version 2: Comparison of Thermal Resistance, Junction-to-Air (Rj-a)

2.2.2.1.2 Thermal Resistance: Junction-to-Lead (Rj-l)

The measured Rj-l resistance values of both versions of the IRF6635 and IRF6644 are displayed in Figure 7. The IRF6635 Version 1 data were obtained from the 2006 study. The Version 1 of the IRF6635 appears to have a lower resistance than the Version 2 while for the IRF6644 the opposite is true. It had been expected that both device types would show the same trends. A closer examination of the data sets using t-test indicates that while the IRF6644 Version 1 and 2 mean resistances are statistically different, the IRF6635 resistances are not. Furthermore, the IRF6635 data sets that were compared were obtained at two different times rather than side by side. Consequently, there was some question about the conclusions to be drawn from the IRF6635 data.

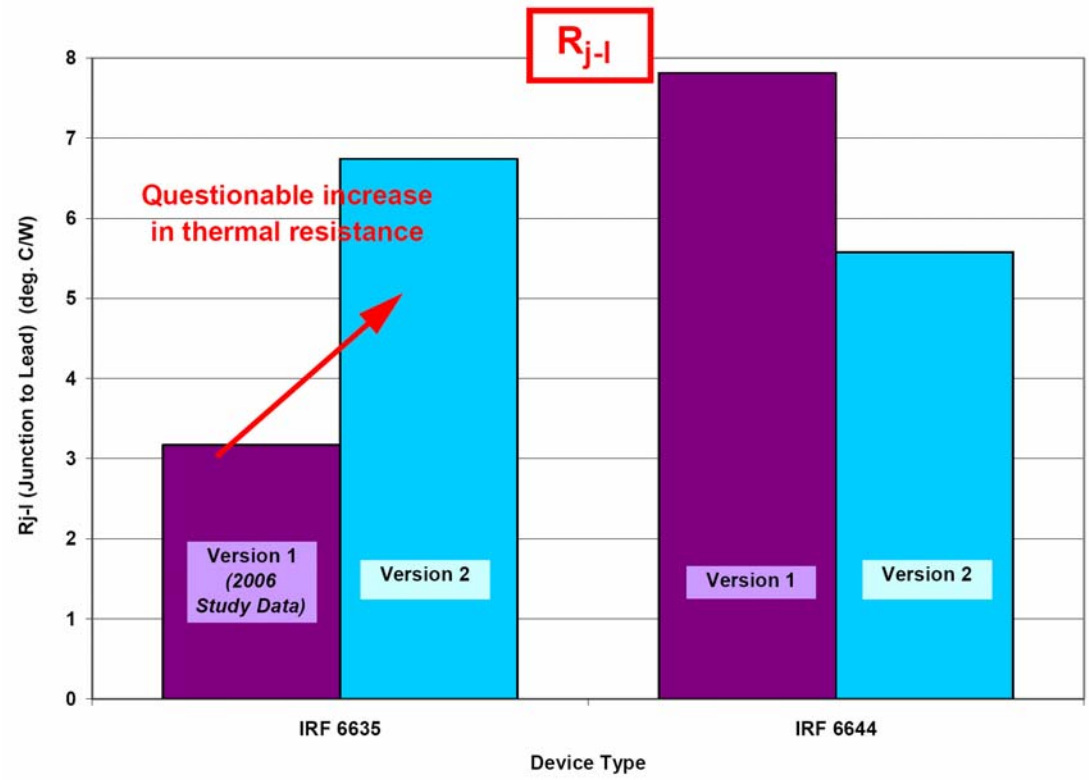


Figure 7. DirectFET Version 1 versus Version 2: Comparison of Thermal Resistance, Junction-to-Lead (Rj-l)

In order to resolve the ambiguity in the resistance data, the resistance measurements on the IRF6635 Version 1 and 2 were repeated. The same Version 1 parts used in the 2006 study were tested alongside the Version 2 parts used in the present study. The parts were tested without heat sinks mounted on them. The revised data for IRF6635 are graphed alongside the IRF6644 data in Figure 8.

The new data for the IRF6635 show that there is no statistical difference between Versions 1 and 2 of this device. The differences observed between the 2006 Version 1 data and the Version 2 data can be attributed to the relative placement of the measurement thermocouple on the drain lead. The drain lead of the DirectFET is very large and offers many places to mount the thermocouple. The junction-to-lead thermal resistance measurement is extremely sensitive to the positioning of the thermocouple. Slight differences in the positioning of the thermocouple can lead to sizable differences in the measured resistance. Consequently, it is reasonable to conclude that unless there are order of magnitude differences between the sets of resistance measurements, the devices can be considered to be equivalent.

Based on this observation, one then concludes that the Versions 1 and 2 of both devices have equivalent thermal resistances. Additionally, one may also reasonably conclude that the IRF6635 and IRF6644 exhibit the same thermal performance.

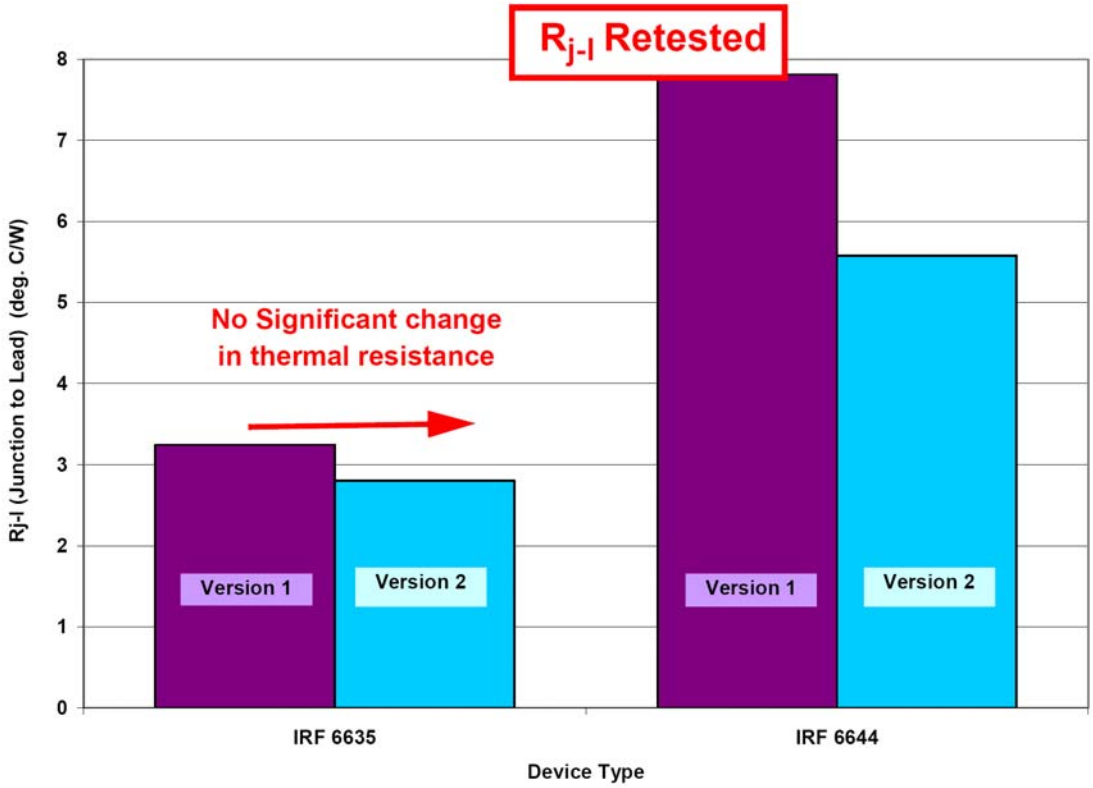


Figure 8. DirectFET Version 1 versus Version 2: Retested IRF6635 Version 1 & 2, Junction-to-Lead (Rj-l)

2.2.2.2 The Effect of Heat Sink

The effect of a finned heat sink on both types of thermal resistances is plotted in Figure 9 and Figure 10. In viewing the plots, one should consider only the change in thermal resistance of with and without heat sink of a particular version (e.g., compare IRF6635 Version 1 with and without heat sink). Also note that the observation regarding the positioning of thermocouple in Rj-l measurements discussed in Section 2.2.2.1.2 is not applicable here, since one is comparing the same parts with and without heat sinks. The thermocouple was not relocated between measurements.

With the exception of the Rj-l of the IRF6635, the heat sink reduced the thermal resistance on average by approximately 15%. The reduction, however, of the Rj-l on the IRF6635 was by 28%. This is observed on both Versions 1 and 2 of this device. The reason for this difference is unknown.

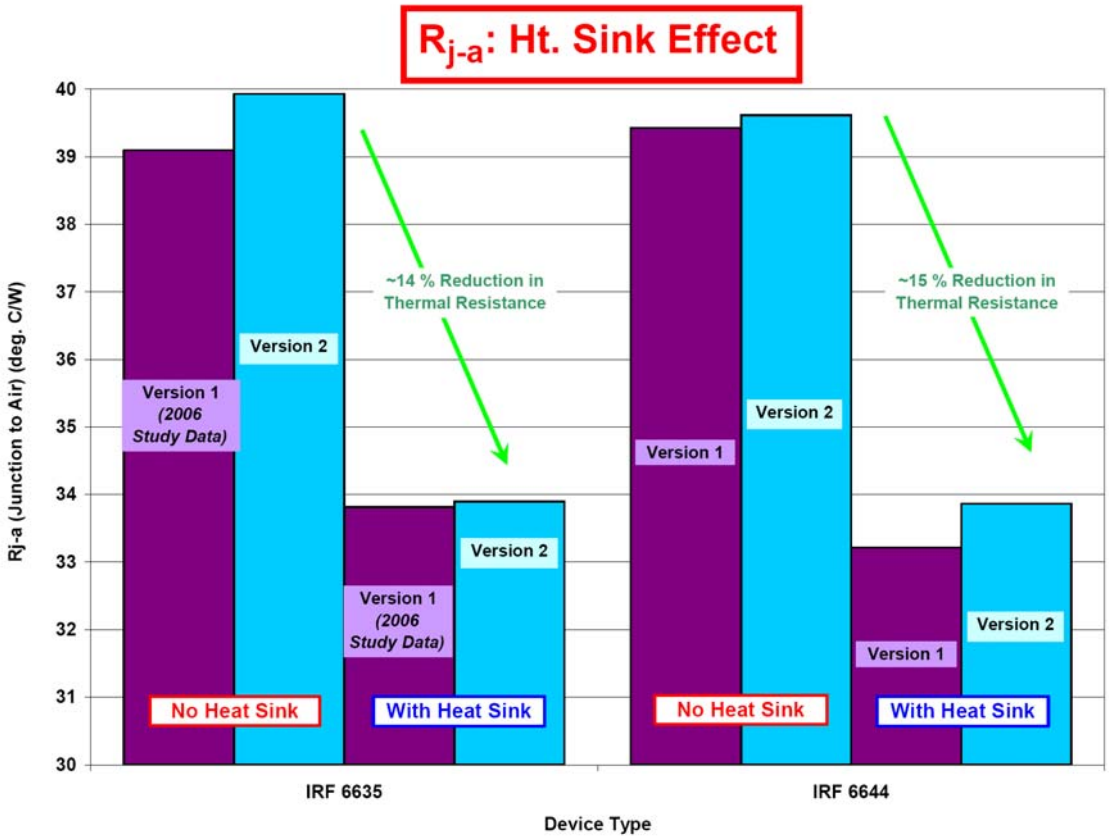


Figure 9. Effect of Heat Sink on Thermal Resistance, Junction-to-Air (Rj-a)

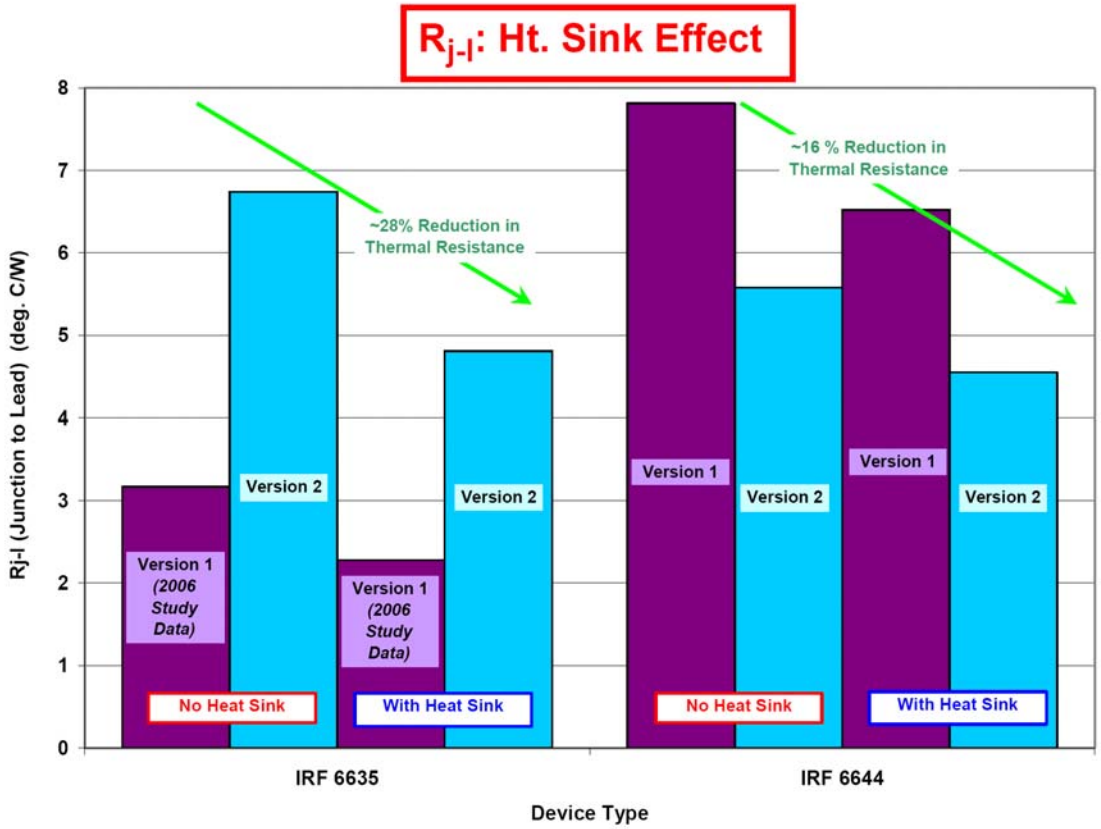


Figure 10. Effect of Heat Sink on Thermal Resistance, Junction-to-Lead (Rj-l)

3.0 High Reliability Evaluation of DirectFET Devices

3.1 Experimental

3.1.1 Electrical and Temperature Cycle Testing

3.1.1.1 Test Assemblies

The assemblies used for these tests are the same ones described in Section 2.1.1.1. Out of the 25 units of each device type tested, 5 units were randomly selected and set aside as control units.

3.1.1.1.1 Control Units

The control units were always electrically tested at the same time as the test assemblies. In this way, it was possible to determine whether a shift in measured parameter values of the test assemblies was real or simply due to drift in the Field-Effect Transistor (FET) Tester. There was significant instrument drift over the course of testing, up to 2 percent drift in the RdsOn measurements.

3.1.1.2 Analysis of Electrical Test Data

All assemblies were electrically tested along with control units before and after the high temperature bake and temperature cycling. The percent shift in each measured device parameter was calculated. Likewise, the percent shift in each measured parameter of the control samples was also computed. The mean percent shift of each control parameter value (ΔP_{Ref}) was then subtracted from the parameter value (ΔP_{Meas}) of each test sample to yield the "true" shift (ΔP_{True}).

$$\Delta P_{True} = \Delta P_{Meas} - \overline{\Delta P}_{Ref}$$

Henceforth, the ΔP_{True} values are referred to as "normalized" delta parameter values and are expressed as percentages taken relative to their initial values.

3.1.1.3 Temperature Cycle Testing

The test assemblies were subjected to a 24-hour bake at 150°C followed by temperature cycling, 100 cycles from -65°C to +150°C. The temperature cycling was performed in accordance with MIL-STD-883, Method 1010, Test Condition C, using a Ransco Temperature Cycle chamber. Assemblies were electrically tested before and after temperature cycling.

3.1.2 Moisture Resistance (Temperature-Humidity-Bias) Testing

3.1.2.1 Test Assemblies

The test assemblies were again the same ones as described in Section 2.1.1.1. Only IRF6635 Version 1 and Version 2 units were subjected to the moisture resistance testing. The IRF6644 devices were not subjected to these tests because this is a test of the package design rather than of the device itself. The differences between the IRF6635 and IRF6644 were not significant enough to warrant testing both devices.

A test board was fabricated (see Figure 11) to apply the constant voltage bias throughout the moisture testing.

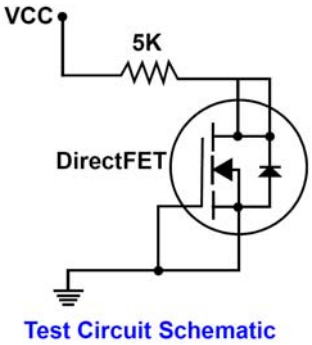
(a) (b) 

Figure 11. (a) Moisture Resistance Test Board and Test Assemblies, and (b) Test Circuit Schematic

3.1.2.2 Temperature-Humidity-Bias Testing

The temperature-humidity-bias (THB) testing was performed by DPA Components, International (Simi Valley, California) using a Trio-Tech humidity chamber. Chamber test conditions were set to 85°C and 1 atm pressure with 85 percent relative humidity. The test board bias was set to 80 percent of device voltage rating or 24V for the IRF6635 devices. The total duration of this test was to be 1000 hours.

The test chamber used for these tests was not a true THB test chamber (DPA's THB chamber was being repaired), but rather a "pressure cooker" chamber normally used for highly accelerated stress testing (HAST). Consequently, it lacked the proper controls to eliminate condensation. In order to prevent moisture condensation on test devices in this chamber, the test chamber was first brought to thermal equilibrium before raising the moisture level to 80 percent. Once relative humidity and temperature had both stabilized, the voltage bias was applied to the assemblies. This procedure was performed in reverse order when removing the assemblies from the test chamber.

Throughout the THB testing, the current output from the test board was monitored. A high current reading (several mA) would constitute a failure. Assemblies were removed from the chamber and electrically tested at Stellar Microelectronics, Inc. using the FET Tester approximately every 250 hours.

3.2 Results and Discussion

3.2.1 Temperature Cycle Testing

The true percent shift (delta) values for each parameter are listed in Table 6 along with their standard deviations. The mean leakage currents were not included in the table (although they were measured) because these exhibited very large standard deviations and were, in spite of this, orders of magnitude smaller than their respective specification limits.

With the exception of the RdsOn values, the change in parameter values were largely insignificant. The shift in RdsOn values was negative for all devices and was most pronounced with Version 2 of each device. The reason for this is not clear. None of the tested devices failed electrical test.

Table 6. Temperature Cycle Testing: Electrical Test Results, Delta Calculations

Measurement*	IRF6635†		IRF6644†	
	Version 1	Version 2	Version 1	Version 2
% Delta Max. RdsOn 1‡ (mOhm)	-0.37 ± 0.85	-3.1 ± 1.8	0.50 ± 0.26	-1.5 ± 0.76
% Delta Max. RdsOn 2‡ (mOhm)	-0.51 ± 0.65	-1.8 ± 1.2	*Not Applicable*	
% Delta Max. Vgs(th) (Volt)	-0.28 ± 0.37	-0.28 ± 0.38	-0.51 ± 0.010	-0.34 ± 0.25
% Delta Min. BVdss (Volt)	0.035 ± 0.092	0.071 ± 0.11	-0.005 ± 0.21	0.061 ± 0.082
% Delta Max. Vdsp (Volt)	-0.18 ± 0.23	-0.29 ± 0.24	-0.41 ± 0.88	-0.22 ± 0.22

* = The mean value of each parameter measured with the control samples is subtracted from the mean values of the tested samples. This is to correct for drift in the FET Tester.

† = Sample quantities for these tests were 20 each.

‡ = A constant of 1.02 mOhm representing the resistance contribution from the circuit board and solder joints, was subtracted from all RdsOn measurements for all IRF6644 devices. A similar constant of 0.8 mOhm was subtracted from all RdsOn measurements for all IRF6635 devices.

3.2.2 Moisture Resistance Testing

The parts completed 255 hours of testing, passed electrical testing at that time, and were returned to the chamber. However, after 325 hours, device failures started to occur—the current output that had previously been 0.0 A jumped to 8 mA. The testing continued up to the 633-hour mark during which the current gradually rose to 29 mA. The parts were removed from the chamber and electrically tested. Four out of five of the IRF6635 Version 1 devices failed electrical testing, while two out of five of the IRF6635 Version 2 devices failed.

The failures of the IRF6635 Version 1 were caused by silver migration and possibly by the presence of residual flux contamination. The electrical failures in all four cases were excessive leakage current (drain to source and gate to source leakage currents) and a low breakdown voltage. Figure 12 shows two of the failed IRF6635 Version 1 parts that were disassembled. Both parts show evidence of significant silver migration from the underlying silver epoxy. The silver particles appear as dull gray or black (from oxidation) on the surface of the die, printed wiring board (PWB), and the can (drain lead). These particles form conductive pathways between the drain and source pads and the gate and source pads that would lead to current leakage failures.

The same excessive leakage currents and low breakdown voltages were also observed with the two failed IRF6635 Version 2 assemblies. Figure 13 shows the two units dissassembled. Again, there is clear evidence of silver migration on the die, PWB and can surfaces.

These failures do not constitute true THB failures, since they were due to moisture condensation on the assemblies. The test chamber did not have proper built-in controls to prevent moisture condensation as would be required of a THB test chamber. The test would have to be repeated using a proper THB test chamber to obtain meaningful results.

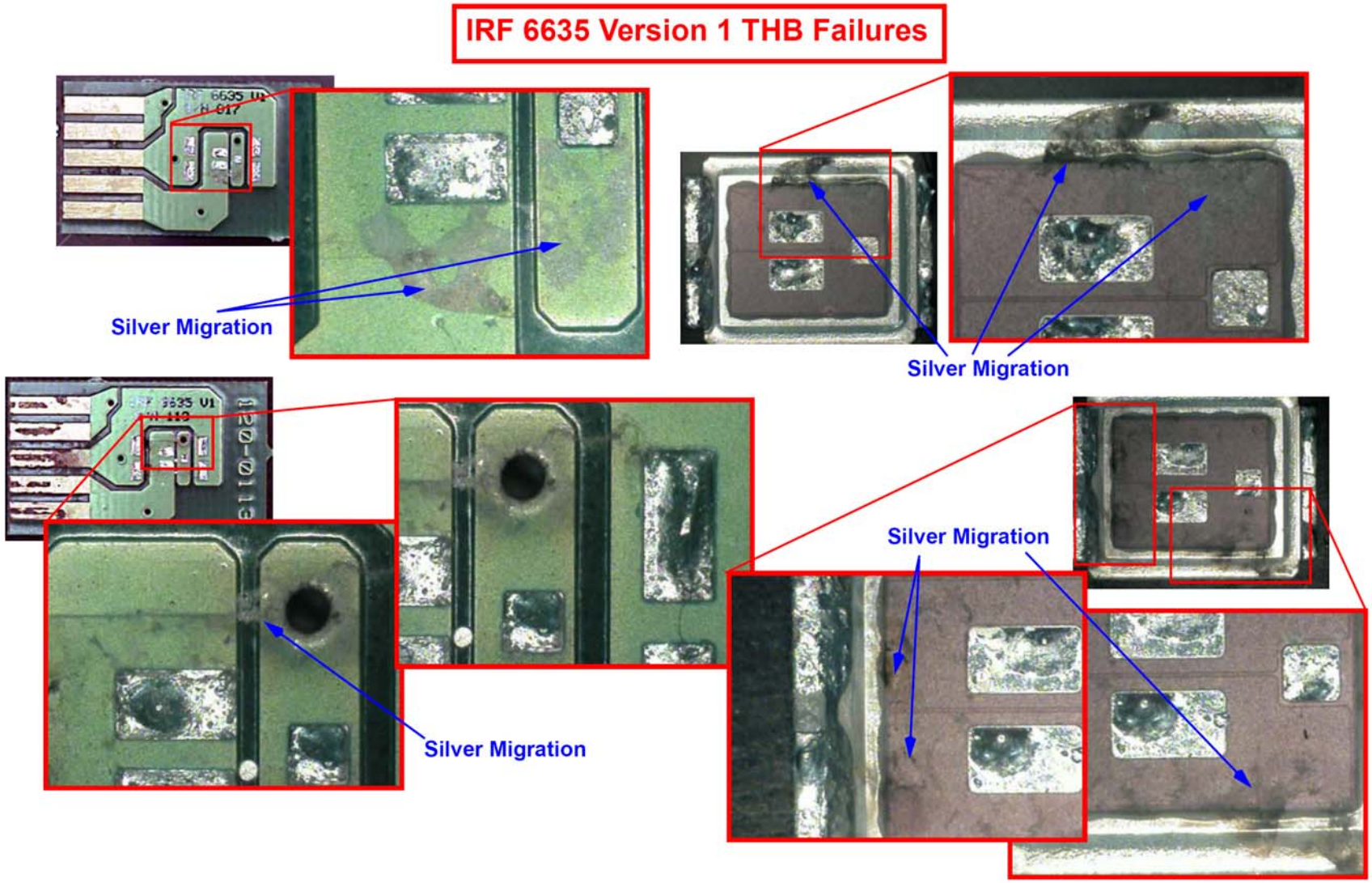


Figure 12. Temperature-Humidity-Bias Testing: Failed IRF6635 Version 1 Test Units Disassembled

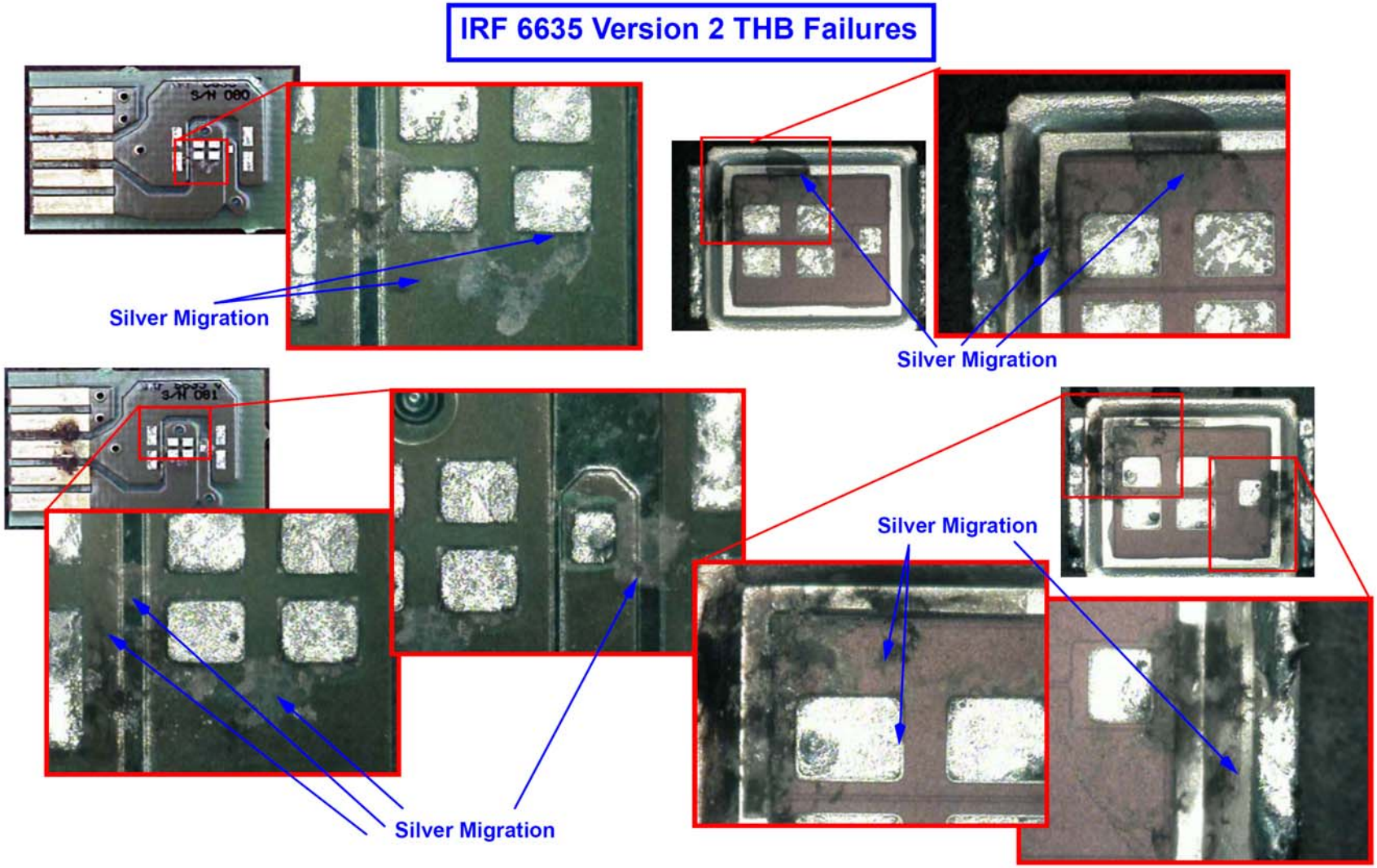


Figure 13. Temperature-Humidity-Bias Testing: Failed IRF6635 Version 2 Test Units Disassembled

Nevertheless, although these results would be unacceptable for terrestrial high reliability assemblies, the performance of the devices for space applications was more than adequate. Space level assemblies will only be exposed to moisture while in assembly and storage during spacecraft fabrication, in transit to the launch site and just prior to launch in the launch vehicle. However, the humidity throughout the fabrication process is carefully controlled and in all cases the parts remain largely unbiased. Consequently, the moisture resistance requirement is far lower than is required for terrestrial applications.

Electromigration and Its Prevention

Silver migration is a common problem with silver-filled epoxies. Silver particles are driven from the epoxy in the presence of a continuous or variable applied voltage, coupled with heat and humidity. In the present instance, the drain lead was positively biased so that it acted as an anode, imparting a positive charge to the silver particles on the surface of the epoxy. These dissolved in the layer of moisture formed on the device surfaces and migrated through this medium driven by the voltage potential to the drain and gate leads, which were both grounded. The rate of electromigration was accelerated by the high humidity and elevated temperature.

This problem can largely be eliminated by using an underfill or conformal coat material. Provided the bonding surfaces are clean and free of residual flux, the underfill or conformal coat create a barrier between the drain and source that effectively prevents electromigration. Parylene conformal coatings and epoxy underfills would provide the best level of protection. Silicone and polyurethane conformal coatings would also provide good protection, though these have a lower resistance to moisture diffusion than Parylene and lower adhesion than the epoxy underfills. Using an epoxy underfill would also have the added benefit (to be discussed in the next section) of improving DirectFET mechanical reliability by dissipating coefficient-of-thermal-expansion (CTE) mismatch stresses.

4.0 Deep Space Thermal Environment and Alternate Solders Evaluation

4.1 Experimental

4.1.1 Test Assemblies Fabrication

4.1.1.1 Assemblies with Lead-Tin Eutectic Solder Alloy

The lead-tin eutectic solder alloy assemblies were the same ones used for the high reliability testing in Section 3.0. No new or additional parts were created for this phase of testing.

4.1.1.2 Assemblies with Indium Solder Alloys

The test assemblies were of the same construction as those described in Section 2.1.1.1.1 except that the indium solder alloys were used in place of the lead-tin eutectic.

4.1.1.2.1 Assembly Materials Issues

The indium alloy solder pastes, Sn77.2:In20:Ag2.8 and Pb60:In40 alloys, were obtained from Indium Corporation (Utica, New York) and were supplied with a no-clean type flux (NC-SMQ flux).

With the exception of the IRF6635 Version 1, all the other devices had source and gate pads pre-tinned with SAC305 alloy (see Section 2.1.1.1.1). Consequently, the source and gate solder joints were not pure indium solder alloy; the SAC305 bumps melted during the solder reflow and combined with the alloy of the solder paste resulting in a mixed composition alloy. The exact composition of these mixed alloy joints was not verified.

The precise effect of the dilution of the paste alloy by the SAC305 is unknown. The large volume of tin in SAC305 reduces the proportion of lead and indium in the solder joint. This effect could make the joints less ductile and more prone to fatigue fracture. However, the presence of other components, copper and silver, could also significantly affect the mechanical properties of the solder joints in some unknown manner.

4.1.1.2.2 Assembly Processes Issues

Solder reflow profiles were developed by Stellar Microelectronics, Inc. (Stellar) using a Research International MicroFlow 7 zone nitrogen atmosphere furnace. The reflow profiles that were actually used were only approximations of the optimum profiles recommended by Indium Corporation. The limited number of heating zones and the extremely low starting zone temperatures were nearly impossible to achieve with this furnace.

Stellar observed a substantial void formation in the gate and source flip chip joints of the IRF6635 Version 1 when attempting to solder with the Sn77.2:In20:Ag2.8 alloy. The IRF6635 Version 1 devices did not have pre-tinned solder pads. By adjusting the reflow profile, the voiding was reduced but not eliminated. There were no difficulties soldering the IRF6635 Version 2 or both versions of IRF6644 with this alloy.

It is thought that the voids were caused by flux entrapment, as well as by a less than optimal solder reflow profile. It is believed that the presence of the SAC305 standoffs made it easier for the flux to escape during reflow by increasing the gap between die pads and by reducing the distance the flux had to travel through the solder. This effect is roughly illustrated in Figure 14. Adding SAC305 bumps to the IRF6635 could have improved the solder joint quality. However, it was too difficult for Stellar to bump individual devices and, consequently, it was not done.

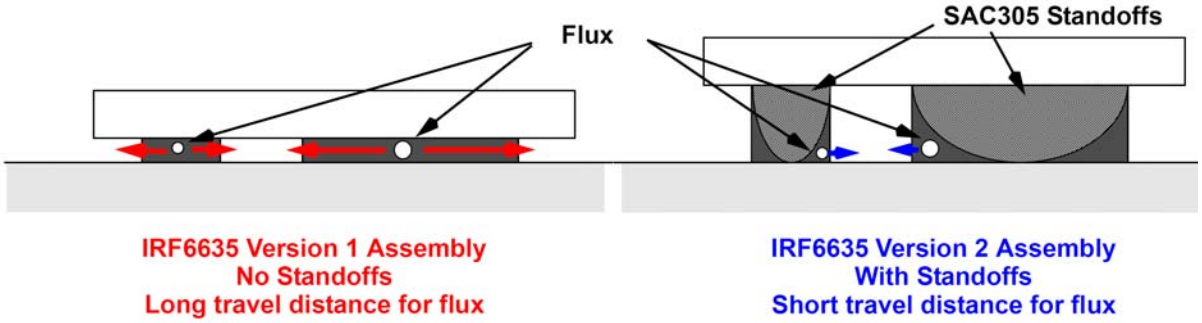


Figure 14. Effect of SAC305 Standoffs on Flux Mobility

Similar problems were experienced with the 60Pb:40In solder alloy in assembling the IRF6635 Version 1. However, in this case, Stellar was unable to reduce the voiding to an acceptable level (less than 25 percent of solderable pad area). Consequently, no IRF6635 Version 1 devices with 60Pb:40In were submitted for testing. Fortunately, with the other devices, the voiding was low enough to be acceptable. Again, it is believed that the presence or absence of standoffs was a factor along with a less than optimal solder reflow profile. The printed wiring board (PWB) solder pad platings may also have been a factor.

4.1.1.3 Matrix of Test Assemblies

Table 7 lists all the electrical test assemblies that were fabricated for this test. The lead-tin eutectic samples were actually the same ones that were used in Section 3.1.1 temperature cycling. With the indium-based solders, quantities of 10 test parts, rather than 20, were used for each device because Stellar only had a limited quantity of Version 2 devices.

Table 7. Matrix of Sample Parts

Test Devices	Solder Alloy	Sample Quantity
IRF6635 Version 1	Sn63:Pb37 Control*	5
	Sn63:Pb37*	20
	Sn77.2:In20:Ag2.8	10
IRF6635 Version 2	Sn63:Pb37 Control*	5
	Sn63:Pb37*	20
	Sn77.2:In20:Ag2.8	10
	Pb60:In40	10
IRF6644 Version 1	Sn63:Pb37 Control*	5
	Sn63:Pb37*	20
	Sn77.2:In20:Ag2.8	10
	Pb60:In40	10

Test Devices	Solder Alloy	Sample Quantity
IRF6644 Version 2	Sn63:Pb37 Control*	5
	Sn63:Pb37*	20
	Sn77.2:In20:Ag2.8	10
	Pb60:In40	10

* = Lead-tin samples were the same ones used in Section 3.1.1 temperature cycle testing.

4.1.2 Extreme Temperature Cycle Testing

The sequence of tests that were performed are detailed in Table 8. Prior to beginning the extreme temperature cycling tests, the indium alloy soldered parts were subjected to the same initial heat soak and temperature cycle testing (100 cycles, -65°C to +150°C) as the lead-tin parts.

The extreme temperature cycle testing was performed using a Sigma Systems M18-C4 Temperature Chamber capable of cycling between -180°C and +150°C. For these tests, the chamber was programmed to ramp between upper and lower set points at a rate of 5°C/min. The dwell at the upper set point temperature was set to 45 minutes while the dwell at the lower set point temperature was set to 10 minutes. The objective of the temperature cycle testing was to subject the parts to conditions that more closely resemble real-world cycling, yet while doing it in a reasonable period of time. The relatively low ramp rate and long dwell at the elevated temperatures would subject the solder joints to low cycle fatigue and creep. In contrast, the rapid rate temperature cycling that is prescribed in MIL-STD-883 subjects the assemblies to high cycle fatigue, which is in some ways less damaging as the assembly materials do not have time to come to full equilibrium, minimizing creep.

The test samples were electrically tested every 25 cycles as described in Section 2.1.1. The same control units used in Section 3.1.1 temperature cycling were used again here.

4.1.2.1 Test Instrument Drift

There was significant measurement drift in the Field-Effect Transistor (FET) Tester measurements, which if not corrected would have led to erroneous conclusions. Plots of mean percent Delta RdsOn (i.e., the percent change is RdsOn relative to initial electrical measurement) of the control samples in Figures 15 and 16 show a significant upwards trend from test to test. All measurements were corrected as discussed in Section 3.1.1.2 to remove this contribution from the measured data.

Table 8. Extreme Temperature Cycling Test Sequence

Test Phase	Step #	Test Step/Description
Heat Soak and 100 Cycles -65°C to +150°C Temperature Cycle "Conditioning"	1	Initial Electrical
	2	Heat Soak, 24 hour @ 150°C
	3	Temperature Cycle, -65°C to +150°C, 100 Cycles
	4	Interim Electrical
100 Cycles -120°C to +115°C Mars Environment Temperature Cycle	5	Temperature Cycle (Mars Environment), -120°C to +115°C, 25 Cycles
	6	Interim Electrical
	7	Temperature Cycle (Mars Environment), -120°C to +115°C, 25 Cycles
	8	Interim Electrical
	9	Temperature Cycle (Mars Environment), -120°C to +115°C, 25 Cycles
	10	Interim Electrical
	11	Temperature Cycle (Mars Environment), -120°C to +115°C, 25 Cycles
	12	Interim Electrical
100 Cycles -180°C to +85°C Deep Space Environment Temperature Cycle	13	Temperature Cycle (Deep Space Environment), -180°C to +85°C, 25 Cycles
	14	Interim Electrical
	15	Temperature Cycle (Deep Space Environment), -180°C to +85°C, 25 Cycles
	16	Interim Electrical
	17	Temperature Cycle (Deep Space Environment), -180°C to +85°C, 25 Cycles
	18	Interim Electrical
	19	Temperature Cycle (Deep Space Environment), -180°C to +85°C, 25 Cycles
	20	Final Electrical

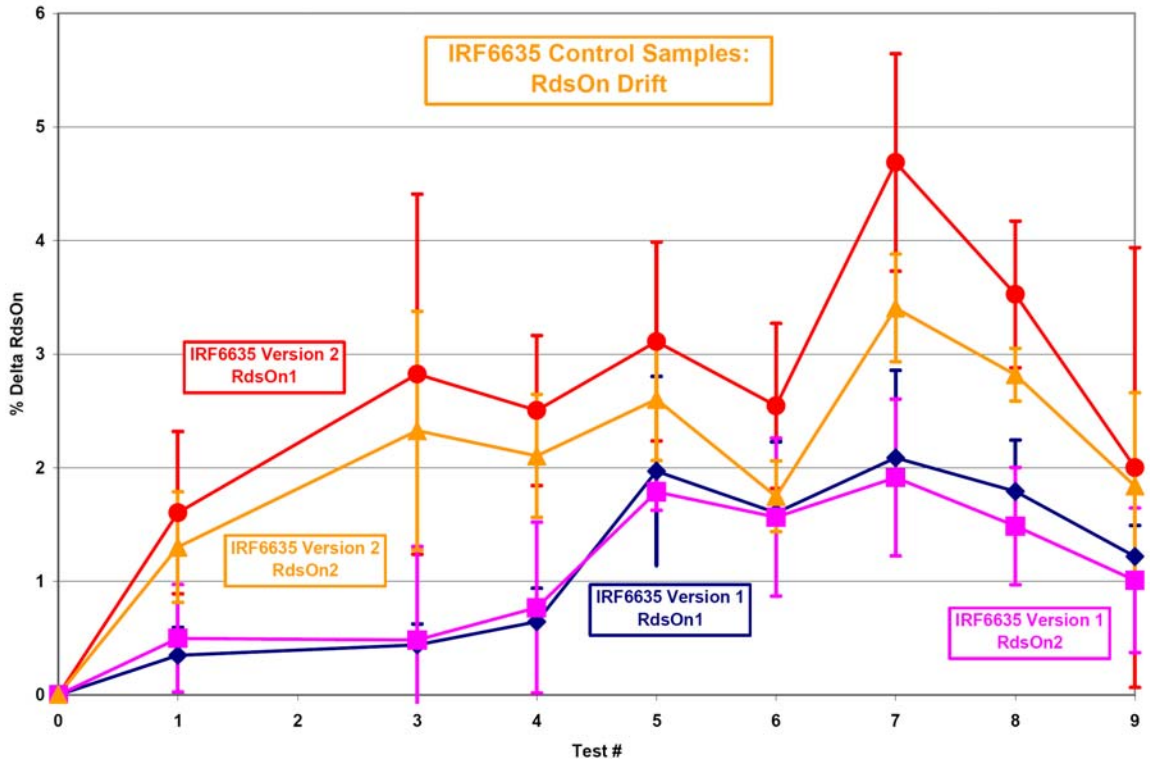


Figure 15. IRF6635 Control Samples: RdsOn Drift

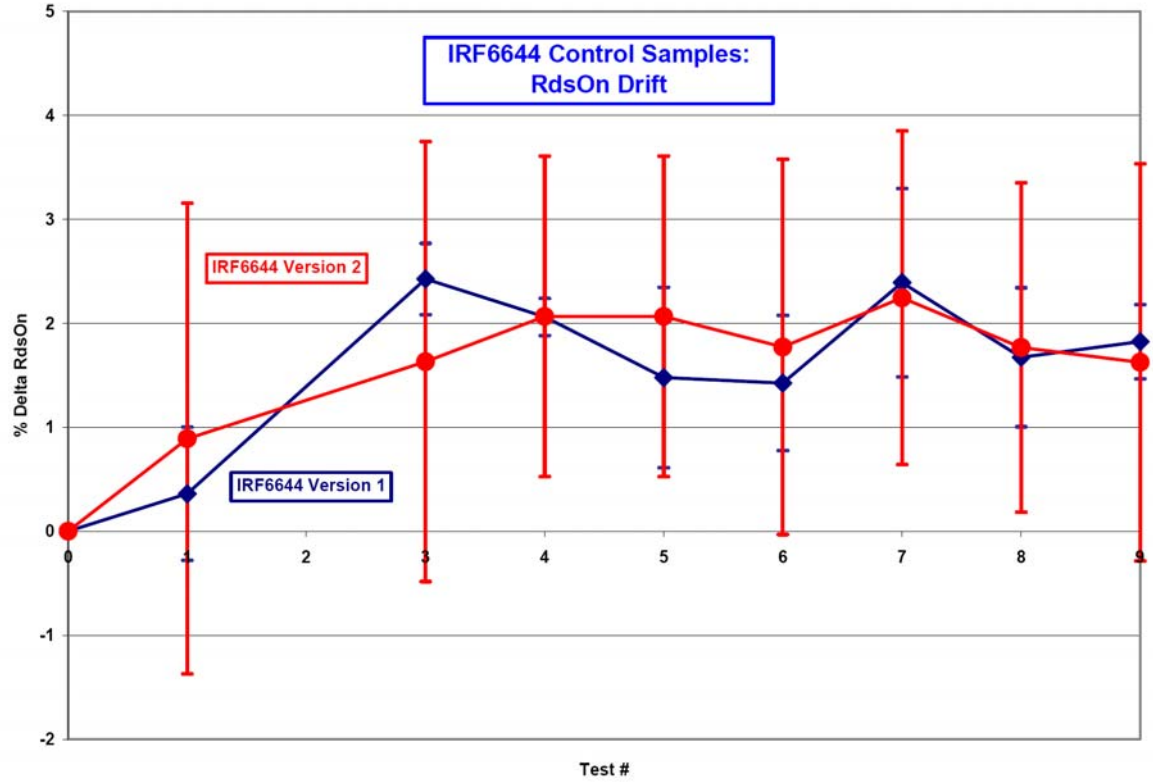


Figure 16. IRF6644 Control Samples: RdsOn Drift

4.1.3 Cross-Sectional and SEM Analysis

At the completion of all the temperature cycling, a sampling of assemblies were sent for cross-sectional and scanning electron microscope (SEM) analysis to Photometrics (Huntington Beach, California). One assembly was selected at random from each group of parts for a total of 15 parts. The parts were cross-sectioned along the cut line indicated by Figure 17. The parts were etched and polished and then inspected under an SEM.

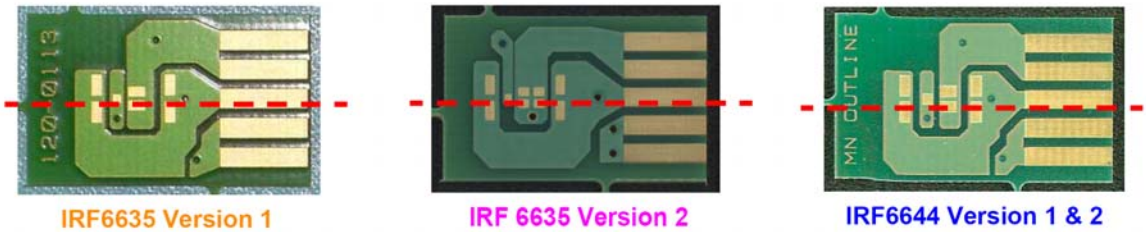


Figure 17. Effect of SAC305 Standoffs on Flux Mobility

4.2 Results and Discussion

4.2.1 Electrical Test Results from Temperature Cycling

4.2.1.1 DirectFET Version 1 versus Version 2: Lead-Tin Assemblies

4.2.1.1.1 Yield Analysis

Table 9 summarizes all the electrical failures that occurred over the course of electrical testing. Most devices survived the first set of extreme temperature cycles (-120°C to +115°C) with the exception of the IRF6635 Version 1, which saw one Igss (reverse gate-to-source leakage) failure. This may be due to device damage.

The -180°C to +85°C temperature cycling precipitated additional failures. The IRF6635 Version 1 experienced a solder joint failure and the IRF6644 Version 2 experienced a complete catastrophic failure, which may be a combination of a device and solder joint failure.

It appears that the SAC305 standoffs may have enhanced the assembly reliability. The smaller solder volume of the IRF6635 Version 1 solder joints meant there was less solder to absorb the thermomechanical stresses leading to a higher failure incidence than other devices. In contrast, the IRF6635 Version 2 devices that had standoffs saw no electrical failures.

By comparison, the structural differences between the two versions of IRF6644 were less significant. Version 2 had a slightly larger solder volume than Version 1. It was then not surprising that they exhibited similar reliability, with one catastrophic failure of an IRF6644 Version 2. This result suggests that additional failures would likely be observed with continued temperature cycling.

Table 9. Cumulative Electrical Failures during Temperature Cycling: Lead-Tin Eutectic

Test Phase	Cycles	IRF6635 Version 1	IRF6635 Version 2	IRF6644 Version 1	IRF6644 Version 2
Heat Soak and 100 Cycles -65°C to +150°C Temperature Cycle "Conditioning"	0	0	0	0	0
	100	0	0	0	0
100 Cycles -120°C to +115°C Mars Environment Temperature Cycle	25	0	0	0	0
	50	1 *(Igss Fail)*	0	0	0
	75	1	0	0	0
	100	1	0	0	0
100 Cycles -180°C to +85°C Deep Space Environment Temperature Cycle	25	1	0	0	0
	50	2 *(RdsOn Fail)*	0	0	0
	75	2	0	0	1 *(Total Failure)*
	100	2	0	0	1

4.2.1.1.2 RdsOn Analysis

Figures 18, 19, and 20 show the mean percent change (percent delta) in RdsOn parameter for IRF6635 and IRF6644 over the course of all temperature cycle testing performed. The delta is calculated with respect to the initial RdsOn measurement of each assembly. The percent delta is said to be "normalized" in these plots because the mean percent delta measured from the corresponding control samples was subtracted from the mean values of the test samples. This ensures that the instrument drift or fluctuations are stripped from the data leaving only the "real" change in the RdsOn. The RdsOn is the only parameter that is plotted here, since it is the only one that was measurably affected by the temperature cycling. Note that data obtained from any of the failed units was omitted from the mean RdsOn calculation and does not appear in these plots.

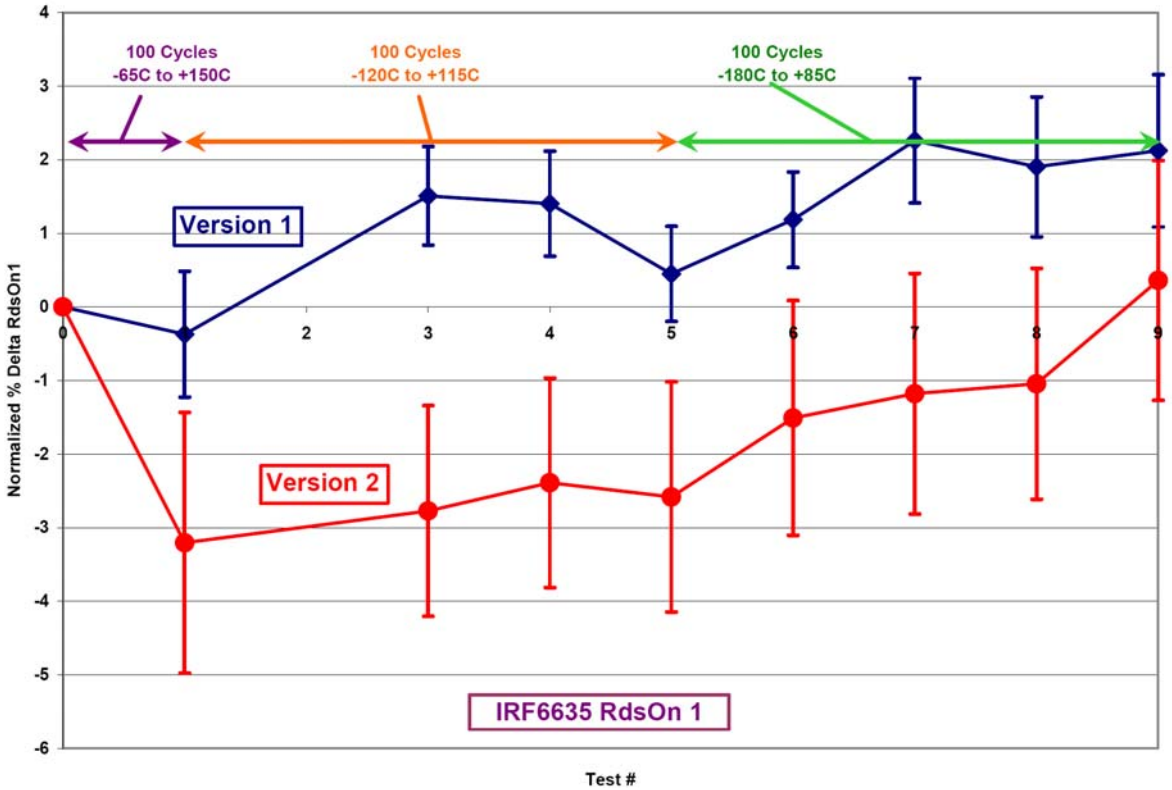


Figure 18. IRF6635 Versions 1 versus 2: Normalized Percent Delta RdsOn1

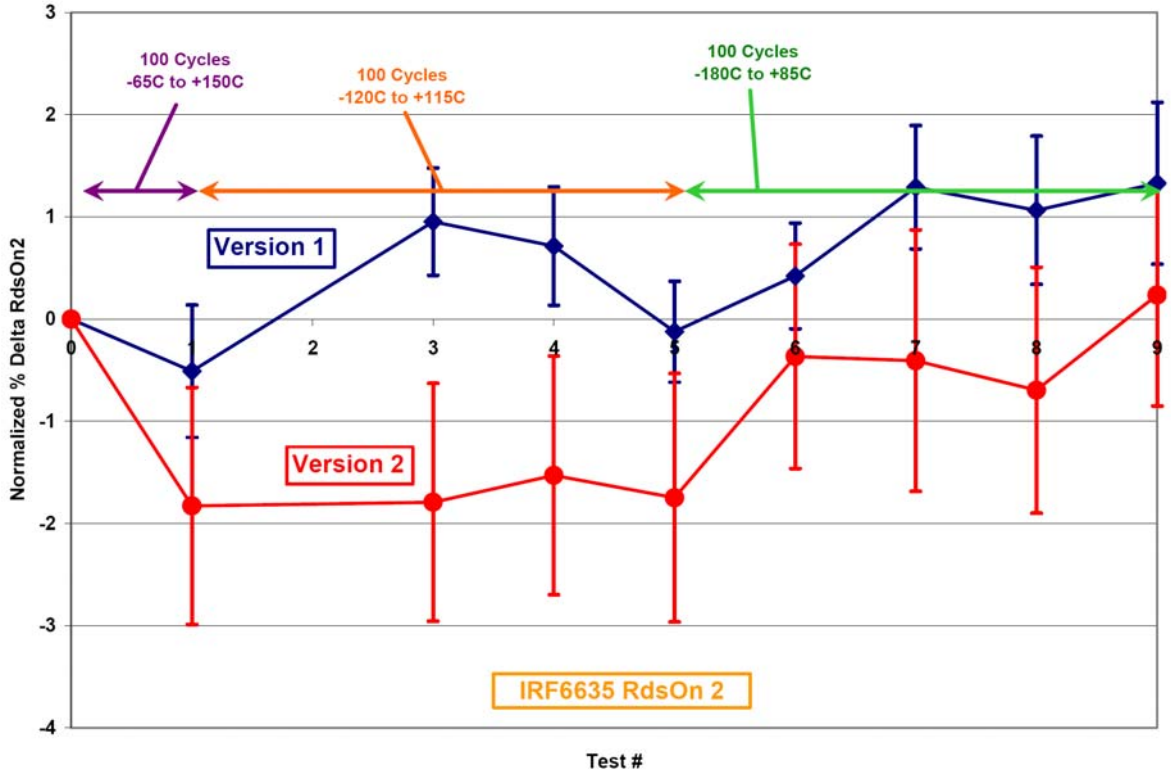


Figure 19. IRF6635 Versions 1 versus 2: Normalized Percent Delta RdsOn2

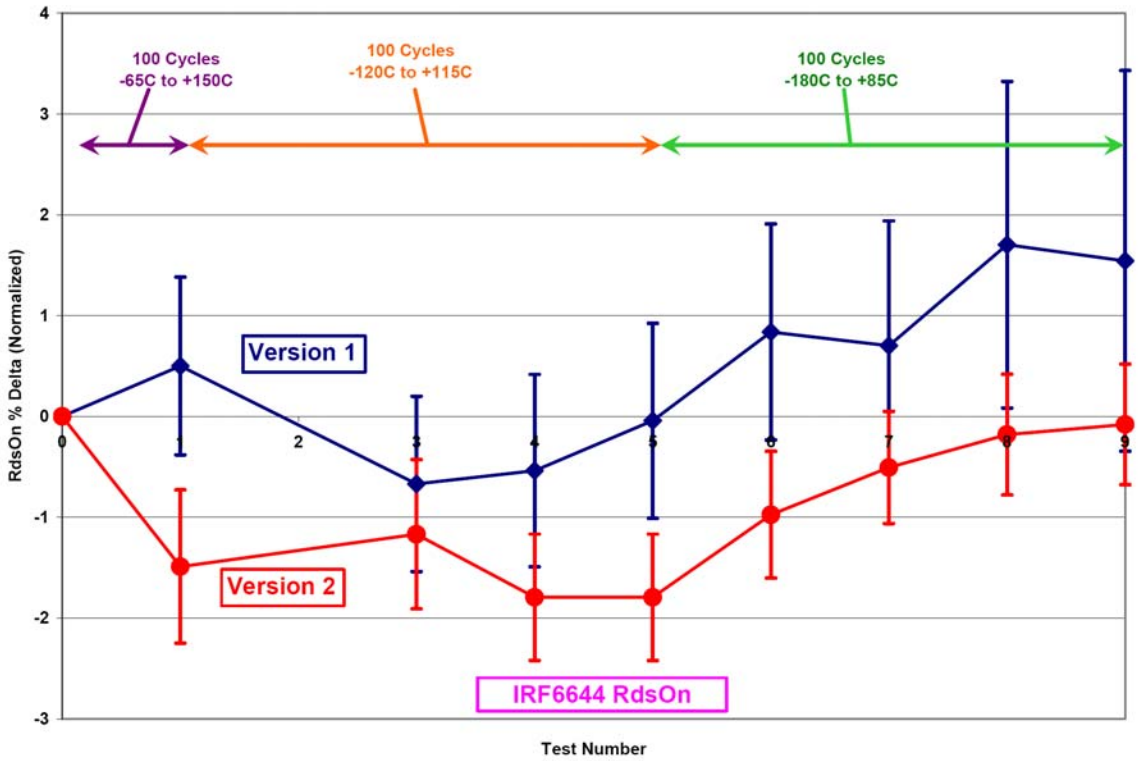


Figure 20. IRF6644 Versions 1 versus 2: Normalized Percent Delta RdsOn

The general observed trend is an initial decrease in on-resistance after the initial 100 cycles of -65°C to +150°C resistance followed by a gradual rise in on-resistance throughout the course of the extreme temperature cycling. The Version 2 devices experienced a larger initial drop in resistance than the Version 1 devices. The cause of the initial drop in resistance is unknown. However, the subsequent rise in resistance was due to the gradual degradation (fatigue) of the solder joints; as the joints fatigue, cracks and voids develop within them that increase solder resistivity.

Both versions of IRF6635 and IRF6644, relative to the RdsOn measured after initial temperature cycling (Test 1), experienced comparable net RdsOn shifts of between 1 and 3 percent over the course of extreme temperature cycle testing. Although these are real measurable shifts, they are still relatively small given the temperature extremes that the assemblies were subjected to. Furthermore, they are small enough that they would probably not even be noticeable in normal applications. For instance, by operating the IRF6635 at the test conditions used for measuring RdsOn1, the device dissipates approximately 1.5 Watts and shifts 3 percent, which equates to only approximately 4.5 mW. Variations in drain current would likely be far more noticeable.

4.2.1.2 DirectFET Assemblies: Lead-tin Eutectic versus Indium Alloy Compositions

4.2.1.2.1 Yield Analysis

Table 10 summarizes all the electrical failures that occurred over the course of electrical testing with all assemblies, including those fabricated with indium alloys. The indium alloy soldered assemblies exhibited similar yields and types of failures to those fabricated with lead-tin eutectic. Remarkably, the units did not begin to fail until late into the third, most extreme regimen of temperature cycling.

Table 10. Cumulative Electrical Failures during Temperature Cycling: All Solder Alloys

Test Phase	Cycles	IRF6635 Version 1		IRF6635 Version 2			IRF6644 Version 1			IRF6644 Version 2		
		Sn63: Pb37	Sn77.2: In20: Ag2.8	Sn63: Pb37	Sn77.2: In20: Ag2.8	Pb60: In40	Sn63: Pb37	Sn77.2: In20: Ag2.8	Pb60: In40	Sn63: Pb37	Sn77.2: In20: Ag2.8	Pb60: In40
Heat Soak and 100 Cycles -65°C to 150°C Temperature Cycle "Conditioning"	0	0	0	0	0	0	0	0	0	0	0	0
	100	0	0	0	0	0	0	0	0	0	0	0
100 Cycles -120°C to +115°C Mars Environment Temperature Cycle	25	0	0	0	0	0	0	0	0	0	0	0
	50	1 (Igss Fail)	0	0	0	0	0	0	0	0	0	0
	75	1	0	0	0	0	0	0	0	0	0	0
	100	1	0	0	0	0	0	0	1 (RdsOn Fail)	0	0	0
100 Cycles -180°C to +85°C Deep Space Environment Temperature Cycle	25	1	0	0	0	0	0	0	1	0	0	0
	50	2 (RdsOn Fail)	0	0	0	0	0	0	1	0	0	0
	75	2	0	0	0	0	0	0	1	1 (Total Failure)	0	0
	100	2	1 (Ids, Bv, Igss)	0	0	0	0	0	1	1	0	0
Total Qty Tested:		20	10	20	10	10	20	10	10	20	10	5*
% Overall Yield:		90	90	100	100	100	100	100	90	95	100	100

* = A total of 10 Pb60:In40 IRF6644 V2 test units were assembled on two different PWB lots. Five units were assembled using one lot fabricated in 06/2006 and five on the other lot fabricated in 08/2007. The assemblies using the older lot of boards exhibited an RdsOn failure at initial electrical. Three of the four remaining functional units failed in the course of temperature cycling. It is believed that the boards contributed to the failures and therefore the data from these five units were omitted from the analysis.

4.2.1.2.2 RdsOn Analysis

The mean percent delta RdsOn values are plotted in Figures 21 through 24. Again the percent delta RdsOn values are "normalized" against the mean percent deltas of the control samples. Only the IRF6635 RdsOn1 is plotted, since the RdsOn2 shows the same general trend.

The indium alloy soldered parts displayed the same trends as the lead-tin assemblies—an initial drop in RdsOn through initial temperature cycling followed by a gradual rise over the course of the extreme temperature cycling. The net increase in RdsOn, relative to Test 1 measurements, was between 1 to 5 percent, which is comparable to the shift observed in lead-tin eutectic assemblies. These are again relatively small changes in resistance.

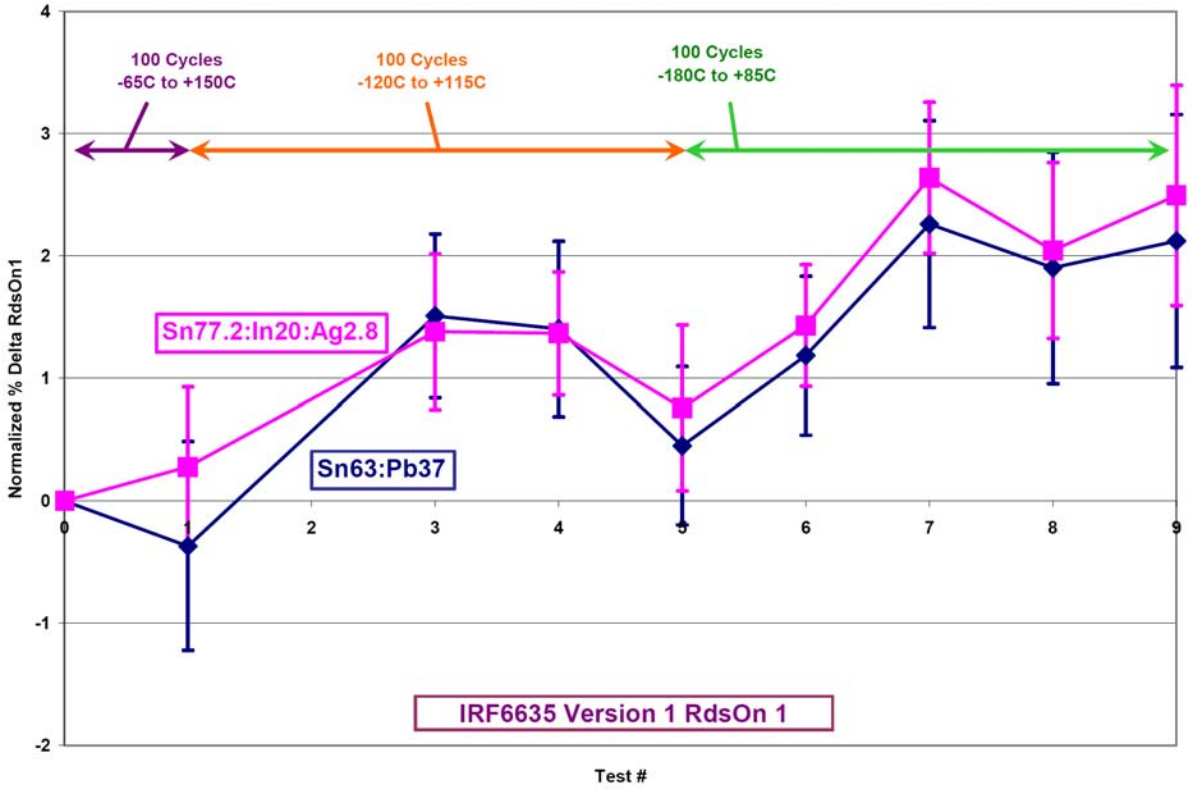


Figure 21. IRF6635 Version 1 Indium Solder Alloys: Normalized Percent Delta RdsOn 1

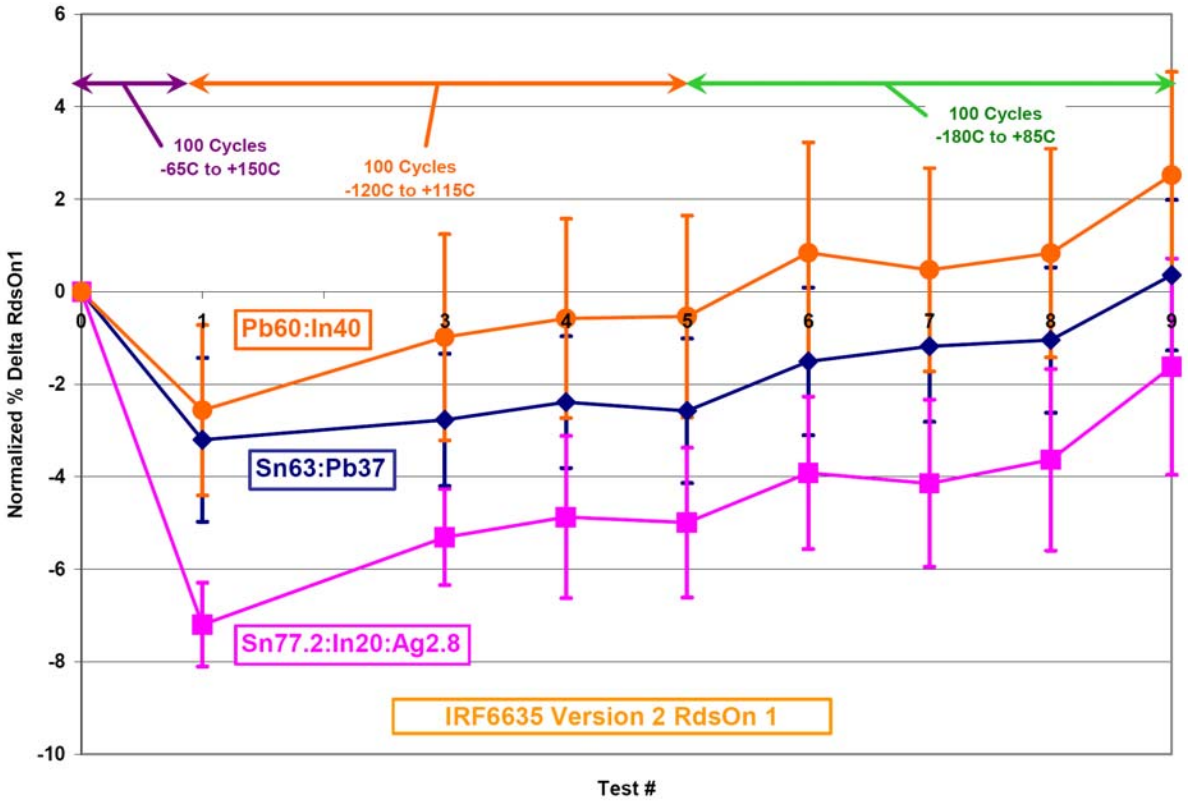


Figure 22. IRF6635 Version 2 Indium Solder Alloys: Normalized Percent Delta RdsOn 1

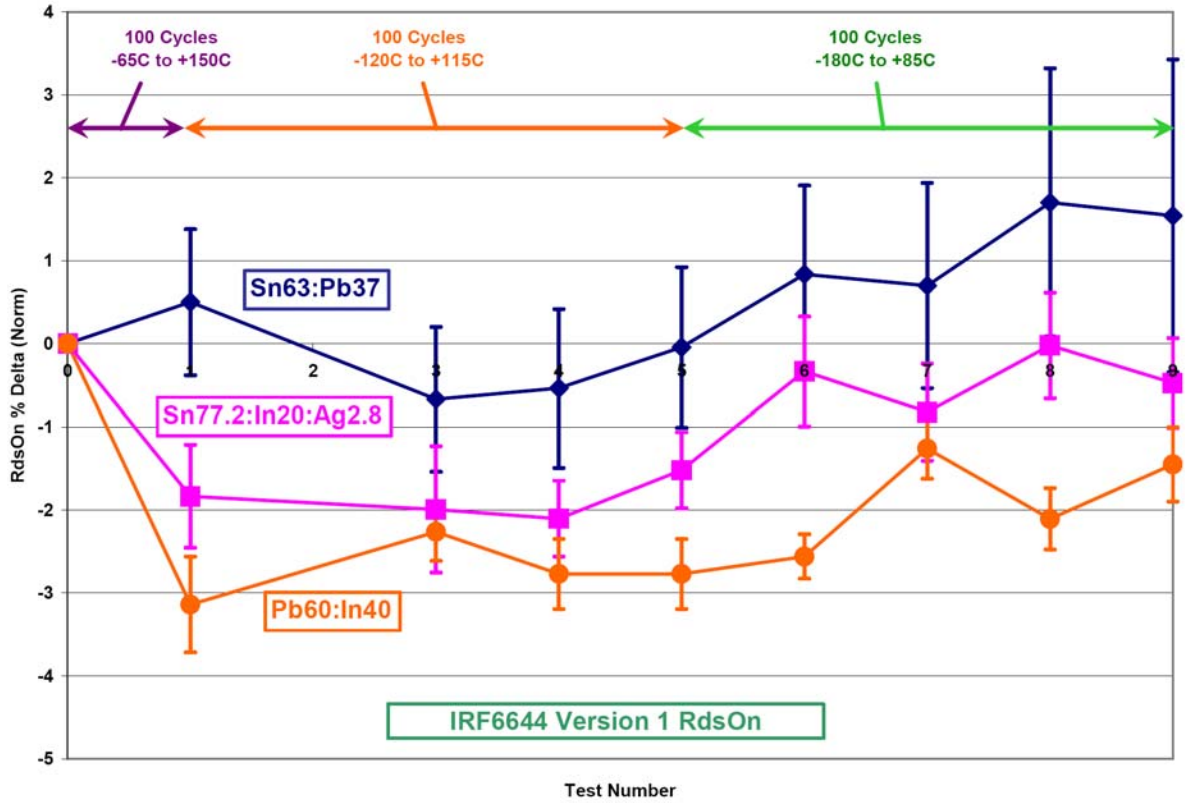


Figure 23. IRF6644 Version 1 Indium Solder Alloys: Normalized Percent Delta RdsOn

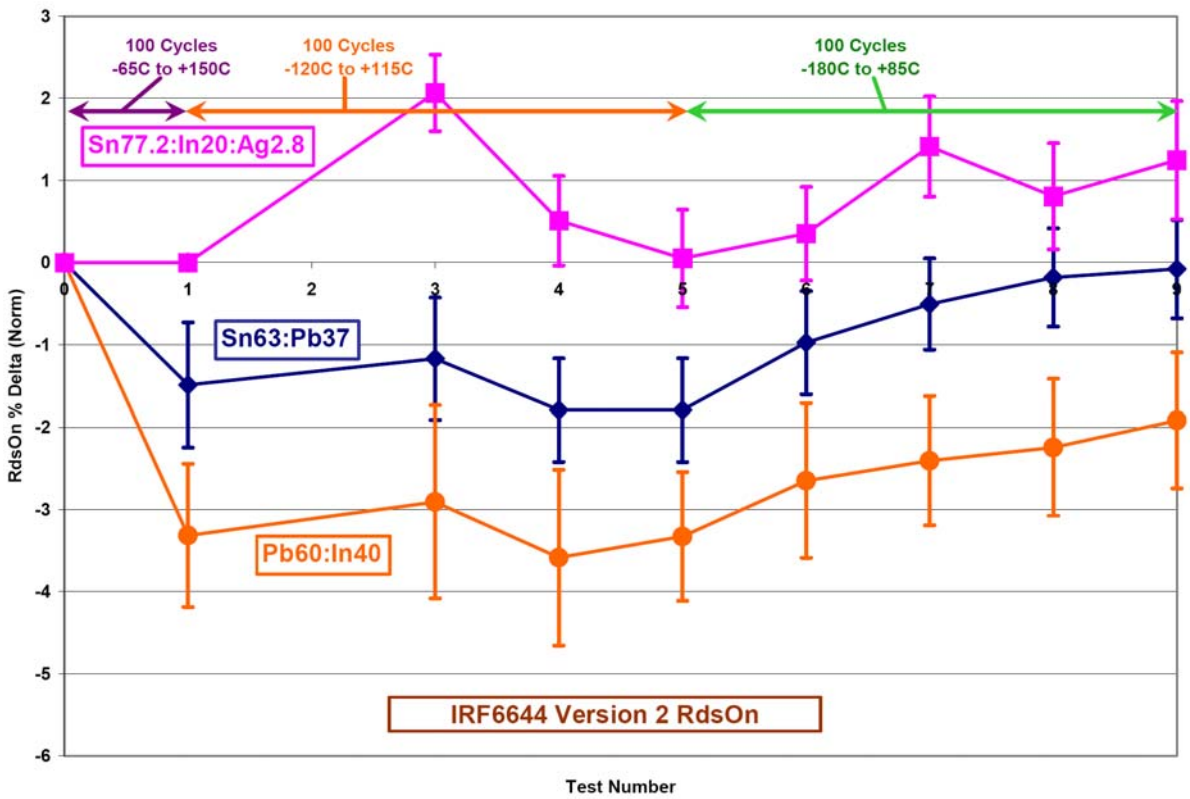


Figure 24. IRF6644 Version 1 Indium Solder Alloys: Normalized Percent Delta RdsOn

4.2.2 Cross-Sectional and SEM Analysis

The cross-sectional analysis provided the most revealing look at the effects of the temperature cycling on the solder joints. The analysis showed that the electrical test data are not necessarily the best indicator of assembly integrity. It also showed that the various solder alloys behaved quite differently under repeated thermo-mechanical stress loading.

4.2.2.1 Lead-Tin Eutectic Soldered Assemblies

The cross-sections of test samples of both versions of IRF6635 and IRF6644 are shown in Figures 25 through 28. In each figure there is also a cross-section of a control sample (not temperature cycled). Both the control and test samples were electrically good units that passed all parameter tests.

The source solder joints on all the temperature cycled devices that were cross-sectioned showed at least some evidence of fatigue cracking. In all cases, the cracks were located near or at the interface between the solder joint and the die pad. Coincidentally, this is not the region of the joint that sees the largest stresses due to the coefficient-of-thermal-expansion (CTE) mismatch between the die and PWB. A typical FR4 laminate has a CTE of between 12 and 16 ppm/°C whereas the silicon has a CTE of only 2.4 ppm/°C. This large mismatch, particularly over the large temperature delta in temperature cycling (265°C in the Deep Space environment cycling) imposes large CTE stresses at the die-to-solder interface. The cyclic loading gradually weakens

the joint at the interface via grain coarsening and crack initiation. The devices eventually fail once the cracks have fully propagated through the joint.

In spite of the presence of cracks in the source solder joint, none of the cross-sectioned units failed electrical testing or displayed any adverse effect on the measured device parameters. For instance, the IRF6644 Version 1 device shows a crack, which appears to traverse the entire length of the source solder joint. Yet, the final RdsOn measurement for this device (10.4 mOhm) was within the specification limits and the percent delta RdsOn was not large (+2.6 percent). Thus, significant deterioration of the solder joint had only minor effects on measured electrical parameters. One can then conclude that electrical monitoring of these devices through environmental testing should not be solely relied upon to determine device or assembly reliability. Destructive physical analysis of samples periodically and randomly selected from the test group must also be performed.

4.2.2.2 Sn77.2:In20:Ag2.8 Soldered Assemblies

Figure 29 depicts the cross-sections of all the assemblies soldered with the Sn77.2:In20:Ag2.8 solder. All cross-sectioned test samples were electrically good units that passed all parameter tests. All samples displayed a distinct interfacial region that was disbonded from either the PWB or the die pads. A large gap between the intermetallic layer of the solder and the PWB or die is clearly visible. The solder formed a thick (3 to 4 microns) and very dense intermetallic with the electroless nickel immersion gold (ENIG) plating (see Figure 30). The intermetallics look like a dense forest of tall, thin crystals. As thick and dense as it was, it was inflexible and may have lifted when it was originally
stressed in temperature cycling.

The separation of the intermetallic layer appears to have had the unintended benefit of stress relieving the solder joint while still maintaining good electrical connection. Examining the electrical test data, there is no evidence of any effect on the device parameters. The RdsOn values were within specification and the percent delta RdsOn was of the same magnitude as compared to the lead-tin eutectic samples. This result underscores the need to evaluate solder joint reliability and integrity by other means than electrical test.

4.2.2.3 Pb60:In40 Soldered Assemblies

Figure 31 depicts the cross-sections of all the assemblies soldered with the Pb60:In40 solder. All cross-sectioned test samples were electrically good units that passed all parameter tests.

All samples displayed substantial voiding. The voids do not have a spherical geometry as might be expected from reflow voids. The outline of the voids are irregular, which suggests that they were formed or deformed by solder creep. The voids were also likely enlarged by the creep of the lead-indium solder. The extensive creeping of the solder would eventually sever the joint leading to an RdsOn failure. Several such failures did occur with the IRF6644 Version 1 and 2 assemblies.

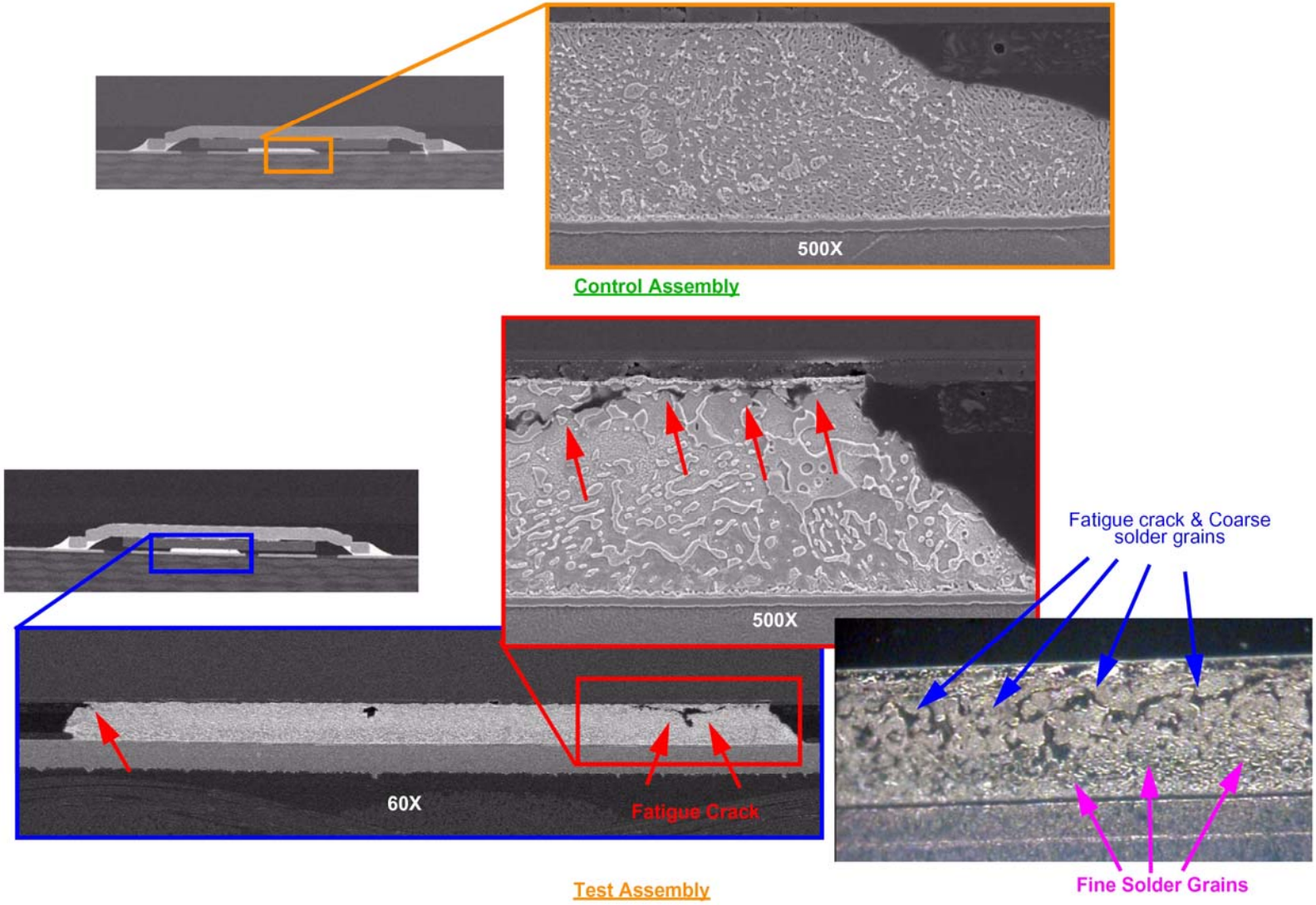


Figure 25. Cross-Sectional Analysis: IRF6635 Version 1 Lead-Tin Eutectic Solder

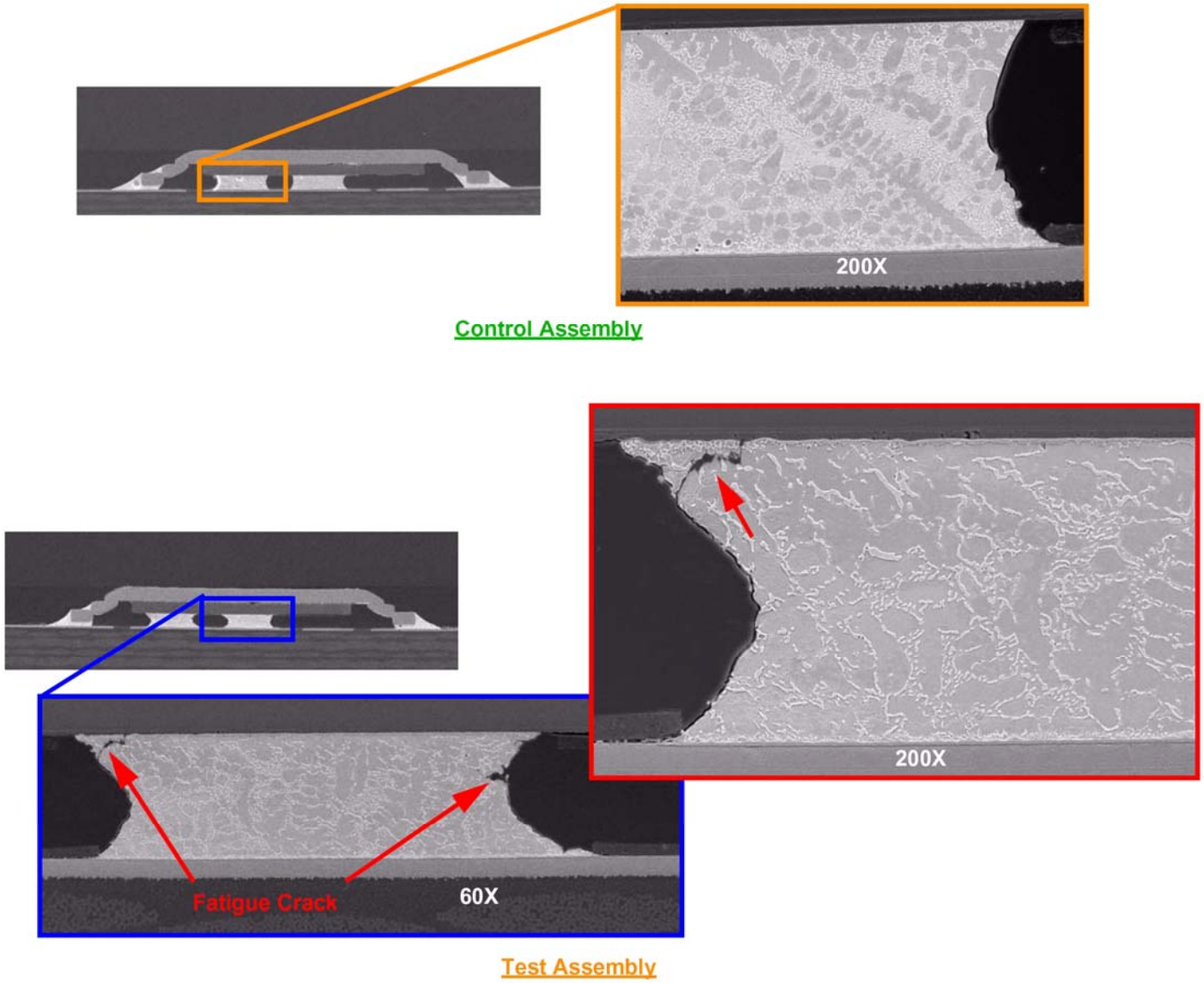


Figure 26. Cross-Sectional Analysis: IRF6635 Version 2 Lead-Tin Eutectic Solder

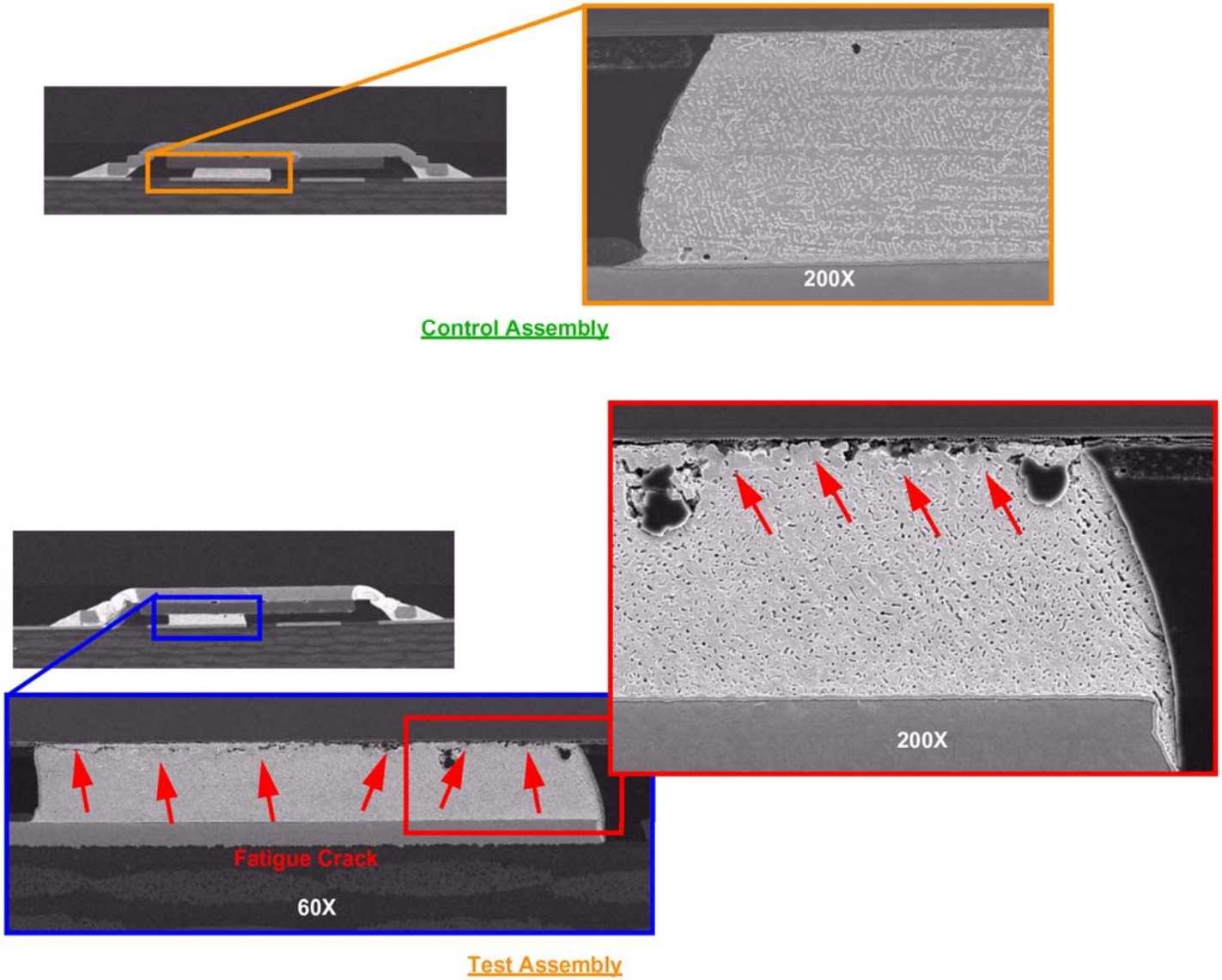


Figure 27. Cross-Sectional Analysis: IRF6644 Version 1 Lead-Tin Eutectic Solder

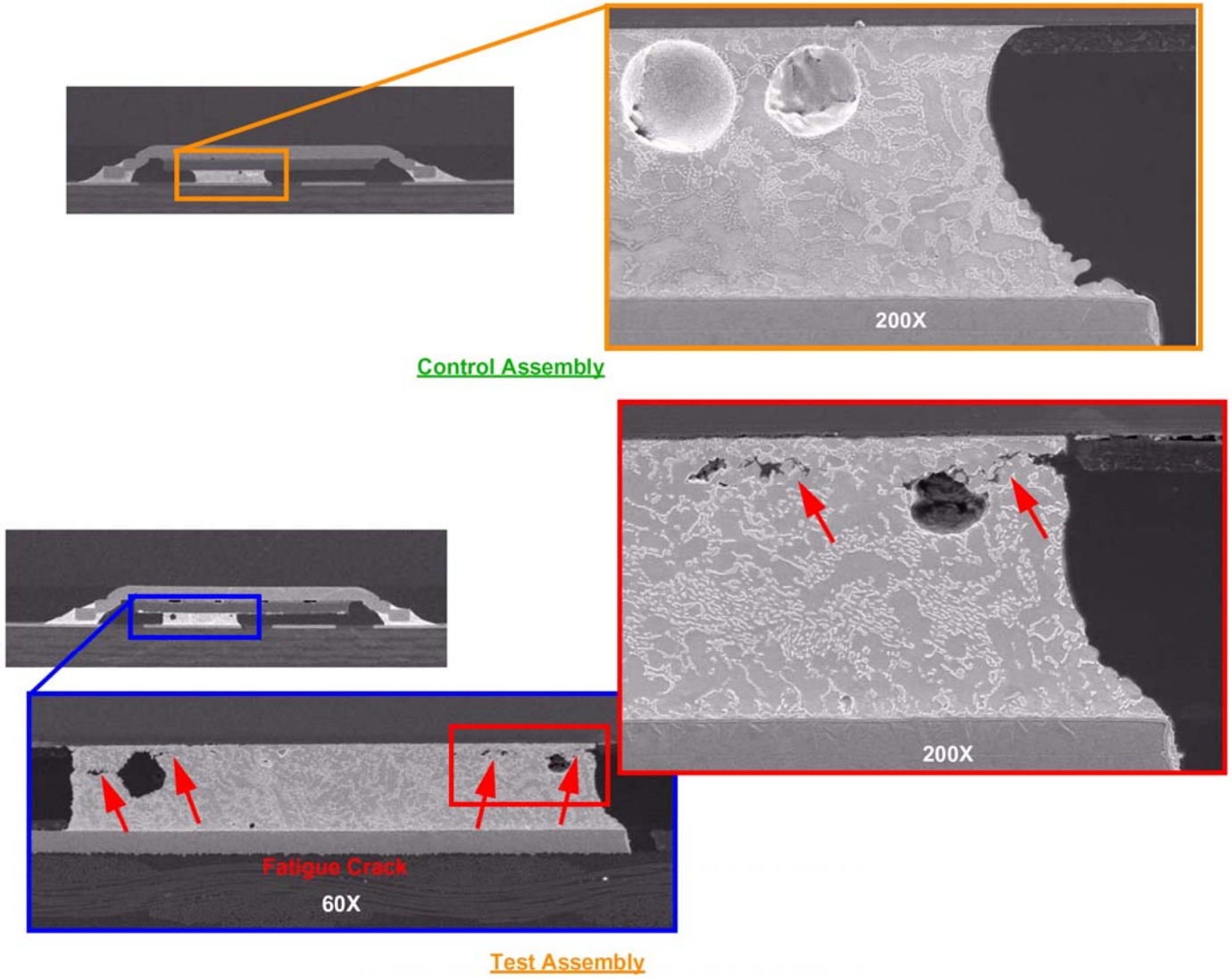


Figure 28. Cross-Sectional Analysis: IRF6644 Version 2 Lead-Tin Eutectic Solder

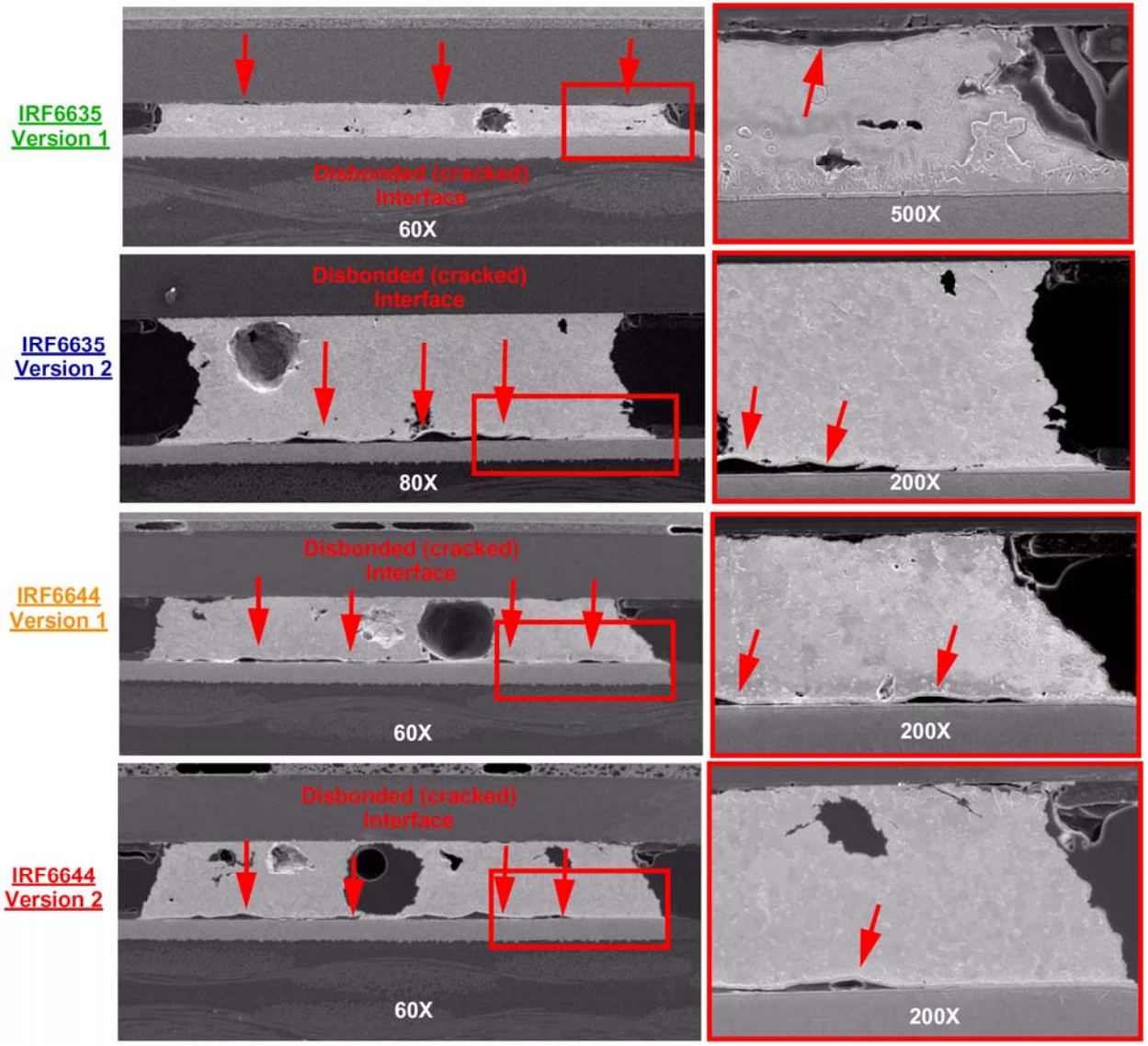


Figure 29. Cross-Sectional Analysis: Sn77.2:In20:Ag2.8 Soldered Assemblies

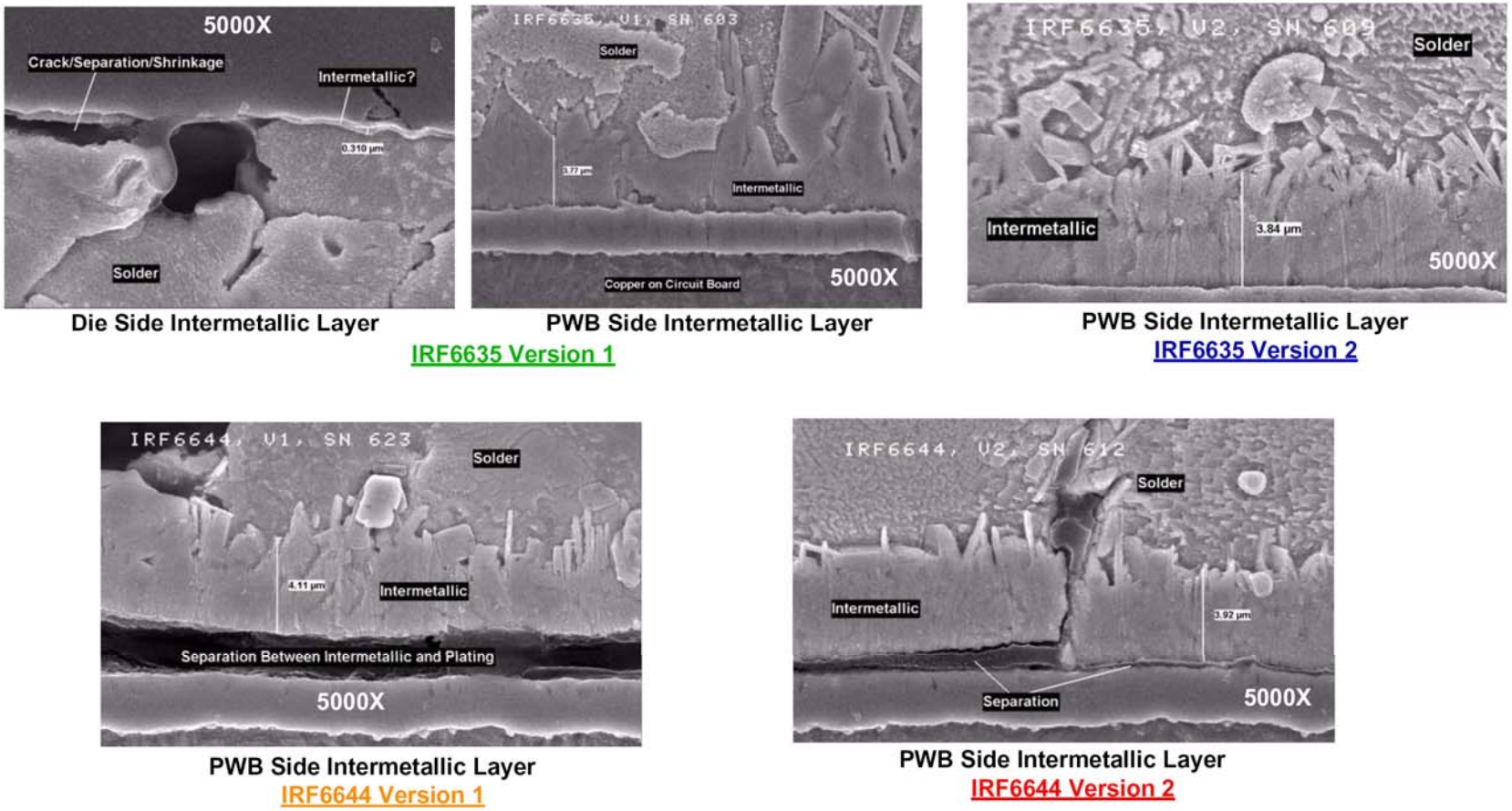


Figure 30. Cross-Sectional Analysis: Sn77.2:In20:Ag2.8 Intermetallics

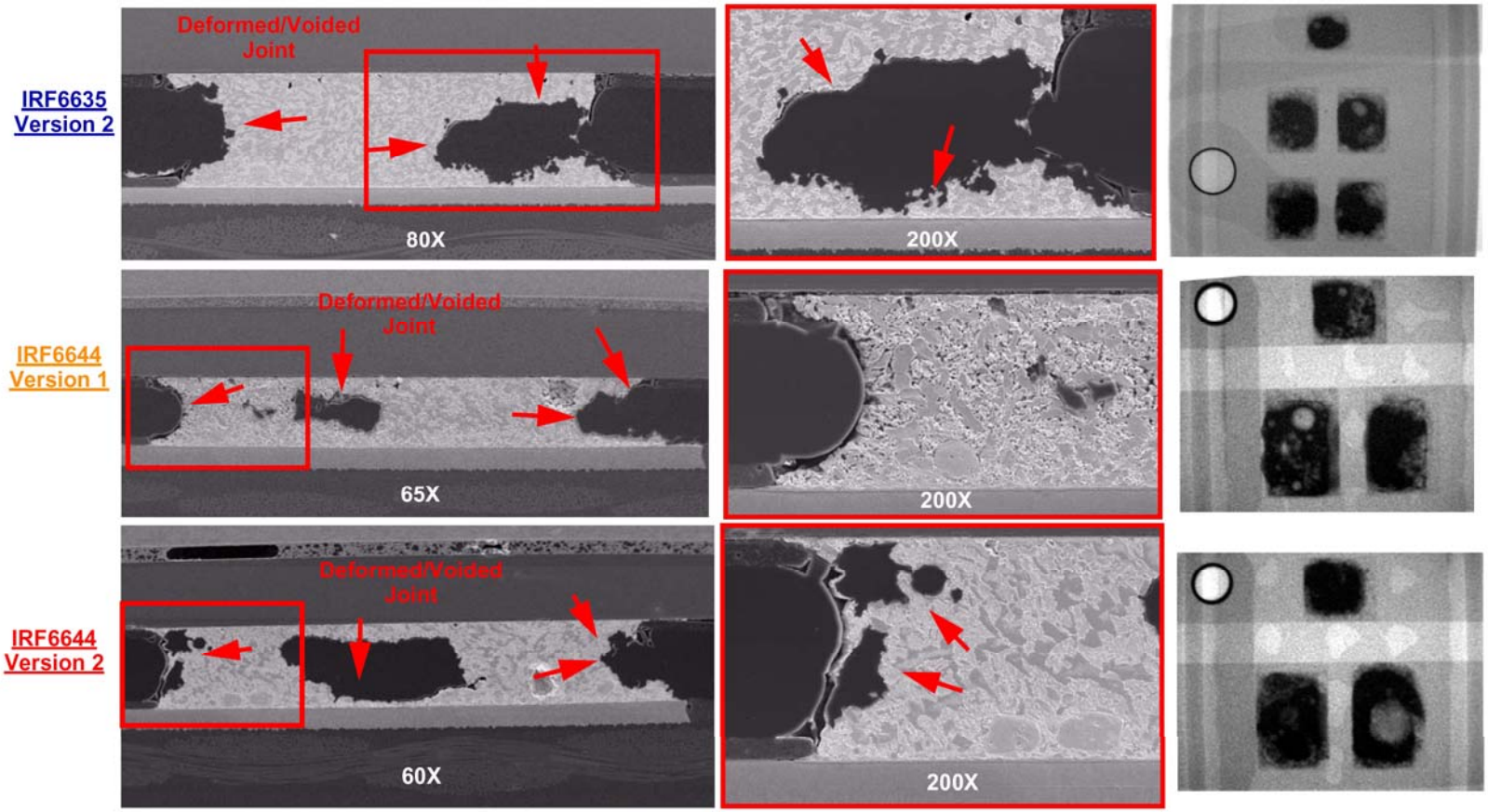


Figure 31. Cross-Sectional Analysis: SEM Micrographs of Pb60:In40 Soldered Assemblies and Top View X-rays

5.0 Summary

5.1 General

5.1.1 Overview

- Stellar Microelectronics, Inc. (Stellar) and the Jet Propulsion Laboratory (JPL) continued a joint study (initially started in 2006) of the International Rectifier (IR) DirectFET metal oxide semiconductor field effect transistor (MOSFET) packaging to evaluate IR's new improved DirectFET package design (Version 2) and to evaluate the suitability of DirectFETs for space-bourne applications.
- The study also evaluated the reliability of the DirectFET devices in simulated Mars (-120°C to +115°C) and Deep Space (-180°C to +85°C) thermal environments.
- Stellar and JPL selected the IRF6635 and IRF6644 DirectFET devices, which were evaluated in the 2006 study, to use in the present study.
- IR supplied the Version 2 IRF6635 and IRF6644 devices for the present study.
- Stellar and JPL evaluated the performance of the two versions of both devices soldered with lead-tin eutectic (Sn63:Pb37), tin-indium-silver (Sn77.2:In20:Ag2.8), and lead-indium (60Pb:In40) solder alloys.

5.1.2 Conclusions

- The Version 2 devices exhibited thermal and electrical characteristics largely identical to the Version 1 devices.
- Both versions of both device types would meet the minimum environmental test requirements for space-bourne, high-reliability assemblies.
- DirectFET devices with built-in standoffs or SAC305 pre-tinned source and gate pads (which acted as standoffs) had the best electrical test yield in Mars and Deep Space thermal environments.
- The three different solders exhibited three different behaviors in response to the cyclic thermomechanical stresses: the lead-tin solder joints fatigue cracked, the tin-indium-silver solder joints separated from the PWB pads, and the lead-indium solder joints creeped.
- None of the solder materials tested performed reliably under the extreme thermal environments even though the electrical test results suggest otherwise.

5.2 Direct FET Version 1 versus Version 2: Thermal & Electrical Performance

- Four sets of electrical test assemblies representing the two versions of both device types were fabricated and electrically tested in accordance with each device specification.
- Four sets of thermal test assemblies were fabricated and the thermal resistances were measured.

5.2.1 Electrical Performance

- With the exception of the RdsOn measurements on IRF6635, there were no statistically significant differences in measured parameters between the two versions of both devices.
- The RdsOn1 and RdsOn2 of IRF6635 Version 2 measured 45 percent and 18 percent lower, respectively, than that of IRF6635 Version 1.
- The difference in RdsOn values may be due to the geometric configuration of the source pads on Version 2 or some other difference internal to the die.

5.2.2 Thermal Performance

- The thermal resistances, Rj-a and Rj-l, of both versions of IRF6635 measured approximately 39.5 W/mK and 3.0 W/mK, respectively.
- The thermal resistance, Rj-a, of both versions of IRF6644 were identical to IRF6635, measuring approximately 39.5 W/mK.
- The thermal resistance, Rj-l, of Versions 1 and 2 of IRF6644 were measured at 7.8 W/mK and 5.6 W/mK, respectively.
- The differences in Rj-l between the two versions of IRF6644 are likely an artifact of the testing. There may have been some slight differences between the position of the measuring thermocouple that altered the measured results.

5.2.2.1 The Effect of a Finned Heat Sink

- Except with the Rj-l of both versions of IRF6635, the addition of a finned heat sink reduced both Rj-a and Rj-l of all devices by approximately 15 percent.
- The Rj-l of both versions of IRF6635 was reduced by approximately 28 percent with the addition of the finned heat sink.
- The reason for the larger reduction in Rj-l on IRF6635 is unknown.

5.3 High Reliability Evaluation of DirectFET Devices

- The four sets of electrical test assemblies were subjected to 100 cycles of -65°C to +150°C temperature cycling.
- One set each of IRF6635 Version 1 and Version 2 were subjected to a 1000-hour temperature humidity bias test.

5.3.1 Temperature Cycle Testing

- All assemblies successfully completed 100 cycles temperature cycling between -65°C and +150°C.
- There were no electrical failures.
- With the exception of the Version 2 RdsOn, there were no statistically significant shifts in electrical parameter deltas.

- The RdsOn parameter on the Version 2 devices of each device type experienced a negative shift of between -1.5 and -3.1 percent.
- The cause of the negative delta in Version 2 RdsOn is unknown.

5.3.2 Temperature-Humidity-Bias Testing

- IRF6635 Versions 1 and 2 experienced current leakage failures after 255 hours of temperature-humidity-bias (THB) testing.
- Electromigration of the silver flakes from the epoxy die attach material was the cause of the electrical failures.
- The electromigration occurred as a result of moisture condensation on the assemblies during the test.
- Moisture condensation occurred because the test chamber lacked adequate controls to prevent it.
- Test failures are not true THB failures and, consequently, these test results are inconclusive.

5.4 Deep Space Thermal Environment and Alternate Solders Evaluation

- Several sets of electrical test assemblies representing both versions of both devices were fabricated using three different solder alloys: lead-tin eutectic (Sn63:Pb37), tin-indium-silver (Sn77.2:In20:Ag2.8), and lead-indium (Pb60:In40).
- All test assemblies were subjected to the following temperature cycling sequence: 100 cycles of -65°C to +150°C followed by 100 cycles of -120°C to +115°C (Mars thermal environment) followed finally by 100 cycles -180°C to +85°C (Deep Space thermal environment).
- Test assemblies were electrically tested every 25 cycles.
- A sampling of electrically good test assemblies was cross-sectioned at the completion of all temperature cycles.

5.4.1 Lead-Tin Eutectic (Sn63:Pb37) Soldered Assemblies

5.4.1.1 Electrical Test Results

5.4.1.1.1 Test Yield

- IRF6635 Version 2 and IRF6644 Version 1 assemblies successfully passed all temperature cycling tests.
- The IRF6644 Version 2 assemblies passed all temperature cycling with only one failure (or 90 percent yield), which occurred around 75 cycles in the Deep Space thermal environment.
- IRF6635 Version 1 had the lowest yield (with the first failures).

5.4.1.1.2 Electrical Performance

- Percent delta RdsOn generally trended downwards by up to -3 percent after the initial 100 cycles of -65°C to +150°C.
- The cause of the negative shift is unknown.
- After the initial negative shift in percent delta RdsOn, this parameter trended upwards over the remainder of testing.
- The Version 2 assemblies had a nearly zero percent delta RdsOn at the completion of all testing while the Version 1 assemblies registered a 1 percent delta RdsOn.
- The upwards trend in RdsOn reflects the micro structural degradation of the solder joints from cyclic stress loading.

5.4.1.2 Cross-Sectional Analysis Results

- The solder joints appeared to be homogeneous. The SAC305 pre-tinned bumps appeared to have liquefied and combined with the lead-tin eutectic alloy during reflow.
- All source pad solder joints on all devices showed evidence of fatigue.
- Fatigue cracks, initiated at the outer edges of the solder joints, propagated through the joint adjacent to the die-pad-to-solder interface.
- Version 1 source pad solder joints exhibited clear evidence of grain coarsening and fatigue crack propagation through the coarsened grain structure.
- Version 1 devices had fatigue cracks, which seemed to traverse the entire width of the solder joint.
- Version 2 devices displayed a lesser degree of grain coarsening and fatigue crack propagation.

5.4.1.2.1 Conclusions

- Although all the cross-sectioned units passed electrical testing, from a structural standpoint, the assemblies were failures.
- The lead-tin solder did not survive the temperature cycling (though the contribution of the SAC305 may have also affected its performance in some fashion).
- The slightly taller solder joints of Version 2 devices may have added some more fatigue resistance.

5.4.2 Tin-Indium-Silver (Sn77.2:In20:Ag2.8) Soldered Assemblies

5.4.2.1 Electrical Test Results

5.4.2.1.1 Test Yield

- The tin-indium-silver soldered assemblies had the best electrical reliability of all the solders.

- With the exception of IRF6635 Version 1, all assemblies successfully passed all temperature cycling tests.
- One of the IRF6635 Version 1 assemblies failed after 100 cycles in the Deep Space environment.
- The leakage current and breakdown voltage failure appears to have been an internal device failure rather than a solder joint failure.

5.4.2.1.2 Electrical Performance

- The tin-indium-silver assemblies exhibited the same general trends as the lead-tin assemblies—a small initial drop in RdsOn after -65°C to +150°C cycling followed by a steady rise throughout the rest of the temperature cycling.
- The IRF6635 Version 1 assemblies had the largest shift, +2.5 percent, in delta RdsOn at the completion of all testing.
- All other devices had shifts of 0 to 1 percent in delta RdsOn at the completion of all testing.
- The upwards trend in RdsOn reflects the structural degradation of the solder joints from cyclic stress loading.

5.4.2.2 Cross-Sectional Analysis Results

- The solder joints appeared to be homogeneous. The SAC305 pre-tinned bumps appeared to have liquefied and combined with the tin-indium-silver alloy during reflow.
- No fatigue cracks or grain coarsening were observed on any devices.
- All the source pad solder joints on both versions of both devices were disbonded from either the PWB or the die pads.
- The disbonding occurred at the pad to intermetallic interface.
- The intermetallic layer in all samples was thick and dense.
- The large thermomechanical stresses during temperature cycling may have caused the interface to fail between the pad and the thick and relatively inflexible intermetallics.

5.4.2.2.1 Conclusions

- Although all the cross-sectioned units passed electrical testing, from a structural standpoint, the assemblies were failures.
- The tin-indium-silver solder “stress relieved” the joints by de-bonding from the solder pads, allowing the devices to pass temperature cycling and electrical testing.
- The tin-indium-silver solder did not survive the temperature cycling (though the contribution of the SAC305 may have also affected its performance in some fashion).

5.4.3 Lead-Indium (Pb60:In40) Soldered Assemblies

5.4.3.1 Electrical Test Results

5.4.3.1.1 Test Yield

- The lead-indium soldered assemblies had yields comparable to the other two solders.
- With the exception of IRF6644 Version 1, all assemblies successfully passed all temperature cycling tests.
- One of the IRF6644 Version 1 assemblies failed RdsOn after 50 cycles in the Mars environment.

5.4.3.1.2 Electrical Performance

- The lead-indium assemblies exhibited the same general trends as the lead-tin assemblies: a small initial drop in RdsOn after -65°C to +150°C cycling followed by a steady rise throughout the rest of the temperature cycling.
- The percent delta RdsOn at the completion of all testing ranged from -2 percent (IRF6644) to +2 percent (IRF6635).
- The upwards trend in RdsOn reflects the microstructural degradation of the solder joints from cyclic stress loading.

5.4.4 Cross-Sectional Analysis Results

- The solder joints appeared to be homogeneous: the SAC305 pre-tinned bumps appeared to have liquefied and combined with the tin-indium-silver alloy during reflow.
- Large voids were evident in the source pad joints of all the test devices.
- The voids had irregular, odd-shaped outlines rather than smooth spherical outlines and surfaces.
- The size and shape of the voids were likely the result of solder creep.

5.4.4.1 Conclusions

- Although all the cross-sectioned units passed electrical testing, from a structural standpoint, the assemblies were failures.
- The lead-indium solder did not survive the temperature cycling (though the contribution of the SAC305 may have also affected its performance in some fashion).

5.5 Recommendations

- DirectFET devices that will be exposed to high humidity levels should be underfilled or conformal coated to prevent silver electromigration.
- The extreme temperature cycling tests should be repeated with DirectFET devices that are either not pre-tinned or have the tinning removed.

- The use of encapsulant underfills should be evaluated as a means to improve DirectFET reliability in extreme thermal environments.
- For extreme thermal environments, DirectFET devices should be assembled onto substrates that are more closely coefficient-of-thermal-expansion (CTE) matched to the die.
- For extreme thermal environments, lower CTE materials than copper should be considered for the DirectFET can (drain lead).

6.0 References

[1] Burmeister, Martin and Amin Mottiwala. 2006. *IR DirectFET Performance Evaluation*. NEPP 07-1280.

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14. ABSTRACT

In 2007, International Rectifier (IR) introduced a new version of its DirectFET metal oxide semiconductor field effect transistor (MOSFET) packaging. The new version (referred to as “Version 2”) enhances device moisture resistance, makes surface mount (SMT) assembly of these devices to printed wiring boards (PWBs) more repeatable, and subsequent assembly inspection simpler. In the present study, the National Aeronautics Space Administration (NASA) Jet Propulsion Laboratory (JPL), in collaboration with Stellar Microelectronics (Stellar), continued an evaluation of the DirectFET that they started together in 2006. The present study focused on comparing the two versions of the DirectFET and examining the suitability of the DirectFET devices for space applications. This study evaluated both versions of two DirectFET packaged devices that had both been shown in the 2006 study to have the best electrical and thermal properties: the IRF6635 and IRF6644.

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Block 1	NOTE: NASA uses month and year (February 2003) on the covers and title pages of its documents. However, this OMB form is coded for block 1 to accept data in the following format: day, month, and year (ex.: day (23), month (02), year (2003) or 23-02-2003, which means February 23, 2003. For this block, use the actual date of publication (on the cover and title page) and add 01 for the day. Example is March 2003 on the cover and title page, and 01-03-03 for block 1.
Block 2:	Technical Paper, Technical Memorandum, etc.
Block 3:	Optional for NASA
Block 4:	Insert title and subtitle (if applicable)
Block 5a:	Complete if have the information
b:	Complete if have the information
c:	Optional for NASA
d:	Optional for NASA; if have a cooperative agreement number, insert it here
e:	Optional for NASA
f:	Required. Use funding number (WU, RTOP, or UPN)
Block 6:	Complete (ex.: Smith, John J. and Brown, William R.)
Block 7:	NASA Center (ex.: NASA Langley Research Center) City, State, Zip code (ex.: Hampton, Virginia 23681-2199) You can also enter contractor's or grantee's organization name here, below your NASA center, if they are the performing organization for your center
Block 8:	Center tracking number (ex.: L-17689)
Block 9:	National Aeronautics and Space Administration Washington, DC 20546-0001
Block 10:	NASA
Block 11:	ex.: NASA/TM-2003-123456
Block 12:	ex.: Unclassified – Unlimited Subject Category http://www.sti.nasa.gov/subjcat.pdf Availability: NASA CASI (301) 621-0390 Distribution: (Standard or Nonstandard) If restricted/limited, also put restriction/limitation on cover and title page
Block 13:	(ex.: Smith and Brown, Langley Research Center. An electronic version can be found at http:// _____ , etc.)
Block 14:	Self-explanatory
Block 15:	Use terms from the NASA Thesaurus http://www.sti.nasa.gov/thesfrm1.htm, Subject Division and Categories Fact Sheet http://www.sti.nasa.gov/subjcat.pdf, or Machine-Aided Indexing tool http://www.sti.nasa.gov/nasaonly/webmai/
Block 16a,b,c:	Complete all three
Block 17:	UU (unclassified/unlimited) or SAR (same as report)
Block 18:	Self-explanatory
Block 19a:	STI Help Desk at email: help@sti.nasa.gov
Block 19b:	STI Help Desk at: (301) 621-0390